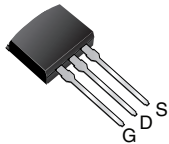


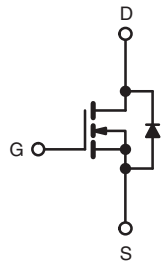
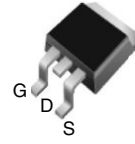
## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	400	
$R_{DS(on)}$ (Max.) ( $\Omega$ )	$V_{GS} = 10$ V	1.0
$Q_g$ (Max.) (nC)	22	
$Q_{gs}$ (nC)	5.8	
$Q_{gd}$ (nC)	9.3	
Configuration	Single	

I<sup>2</sup>PAK (TO-262)



D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{oss}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both US Line Input Only)

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF730AS-GE3	SiHF730ASTRL-GE3 <sup>a</sup>	SiHF730ASTRR-GE3 <sup>a</sup>	SiHF730AL-GE3
Lead (Pb)-free	IRF730ASPbF	IRF730ASTRLPbF <sup>a</sup>	IRF730ASTRRPbF <sup>a</sup>	IRF730ALPbF
	SiHF730AS-E3	SiHF730ASTL-E3 <sup>a</sup>	SiHF730ASTR-E3 <sup>a</sup>	SiHF730AL-E3

**Note**

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	400	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	5.5	A
		$T_C = 100$ °C	3.5	
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$	22		
Linear Derating Factor		0.6	W/°C	
Single Pulse Avalanche Energy <sup>b, e</sup>	$E_{AS}$	290	mJ	
Avalanche Current <sup>a</sup>	$I_{AR}$	5.5	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	7.4	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	74	W
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>		$dV/dt$	4.6	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>

**Notes**


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 19$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5.5$  A (see fig. 12).
- $I_{SD} \leq 5.5$  A,  $dI/dt \leq 90$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- Uses IRF730A, SiHF730A data and test conditions.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

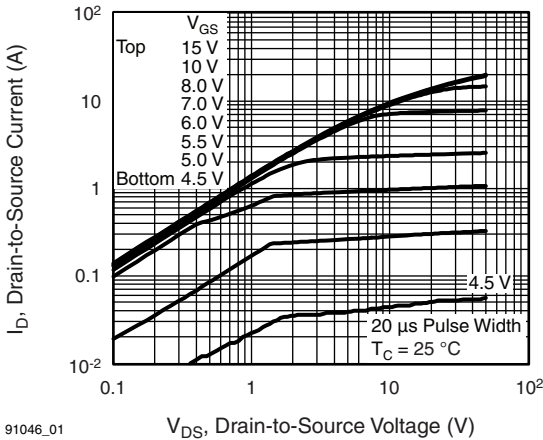
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	400	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.5	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 3.3\text{ A}^b$	-	-	1.0	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3.3\text{ A}^d$	3.1	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>d</sup>	-	600	-	pF	
Output Capacitance	$C_{oss}$		-	103	-		
Reverse Transfer Capacitance	$C_{rss}$		-	4.0	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	890	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 320\text{ V}, f = 1.0\text{ MHz}$	-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3.5\text{ A}, V_{DS} = 320\text{ V}$ , see fig. 6 and 13 <sup>b, d</sup>	-	-	22	nC
Gate-Source Charge	$Q_{gs}$			-	-	5.8	
Gate-Drain Charge	$Q_{gd}$			-	-	9.3	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 3.5\text{ A}, R_g = 12\text{ }\Omega, R_D = 57\text{ }\Omega$ , see fig. 10 <sup>b, d</sup>	-	10	-	ns	
Rise Time	$t_r$		-	22	-		
Turn-Off Delay Time	$t_{d(off)}$		-	20	-		
Fall Time	$t_f$		-	16	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.5	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	22		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.5\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b, d$	-	370	550	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.6	2.4	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .
- Uses IRF730A, SiHF730A data and test conditions.

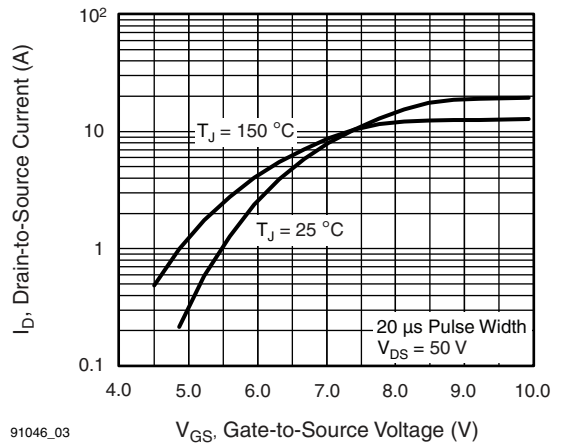


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



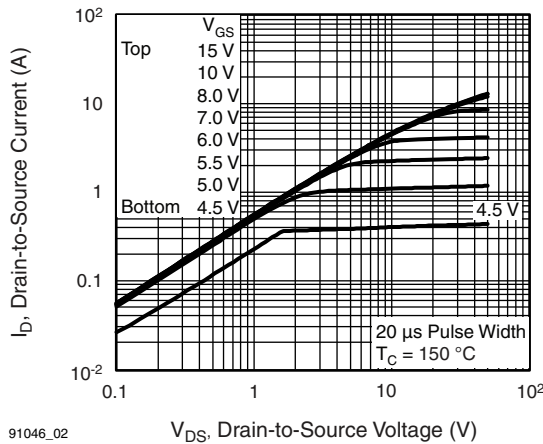
91046\_01

**Fig. 1 - Typical Output Characteristics**



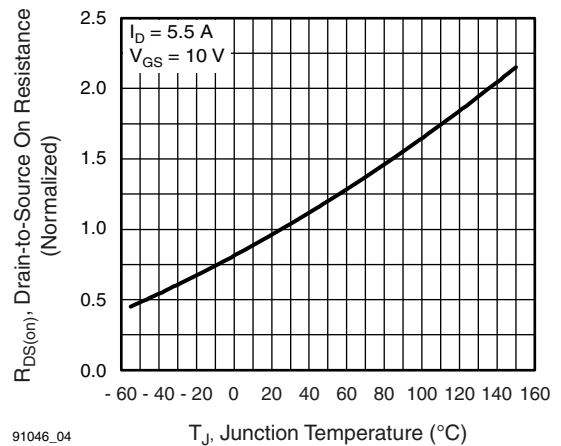
91046\_03

**Fig. 3 - Typical Transfer Characteristics**



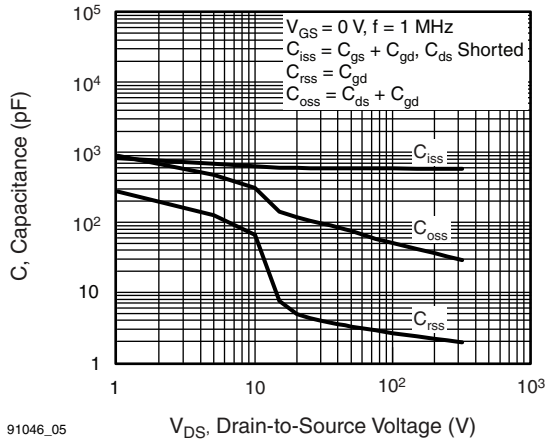
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**Fig. 2 - Typical Output Characteristics**

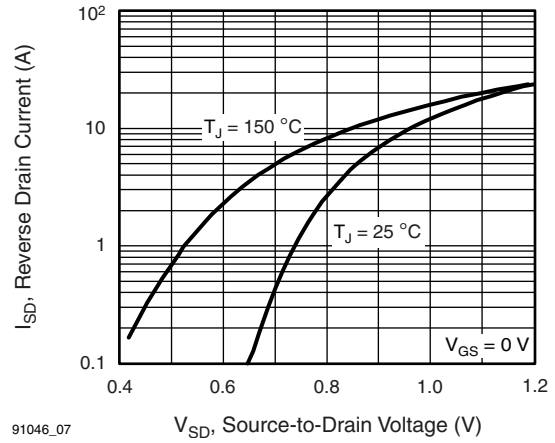


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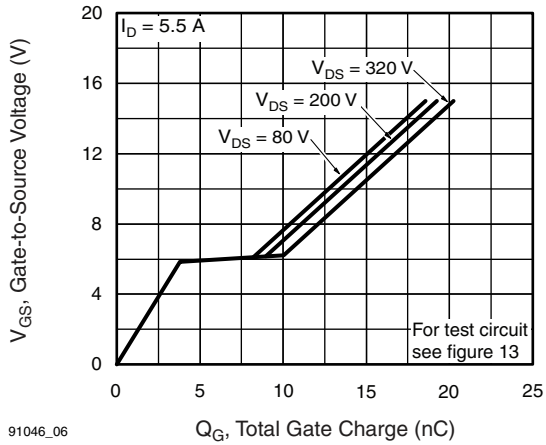
**Fig. 4 - Normalized On-Resistance vs. Temperature**



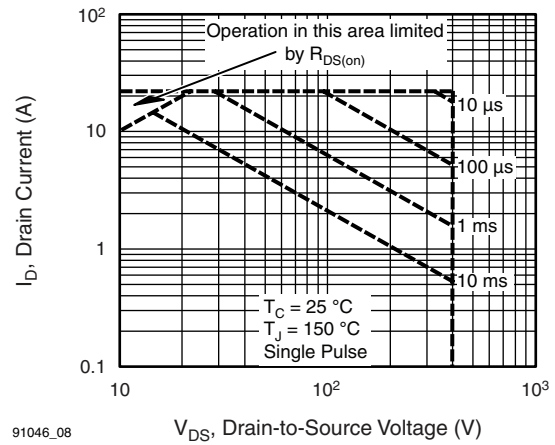
91046\_05  
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



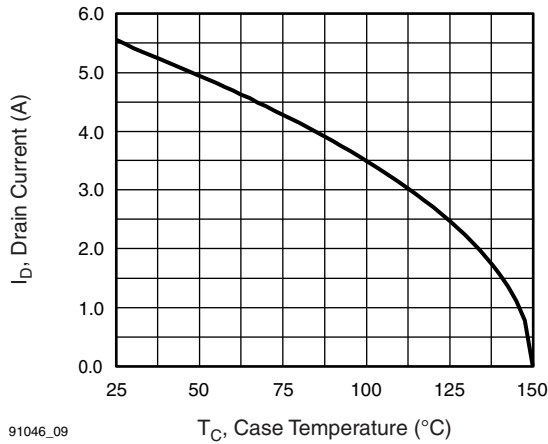
91046\_07  
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



91046\_06  
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

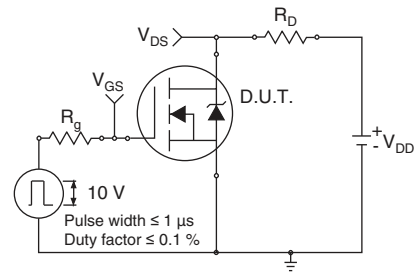


91046\_08  
**Fig. 8 - Maximum Safe Operating Area**

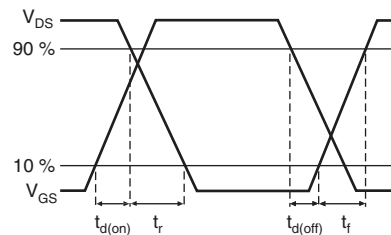


91046\_09

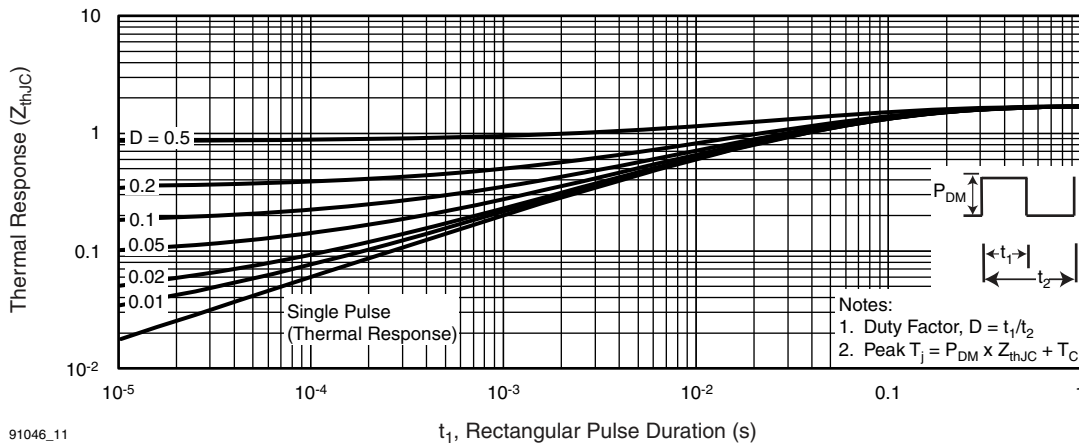
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**

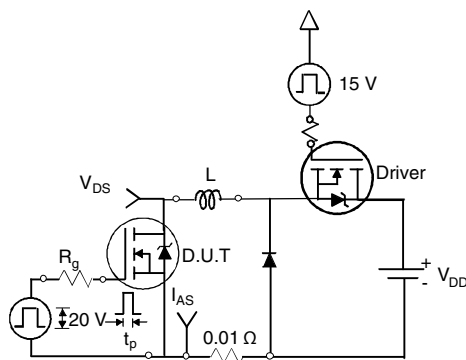


**Fig. 10b - Switching Time Waveforms**

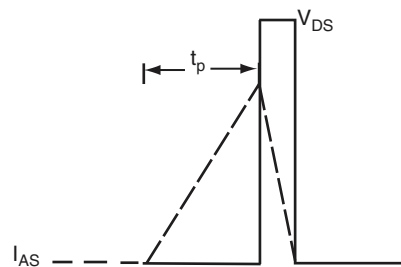


91046\_11

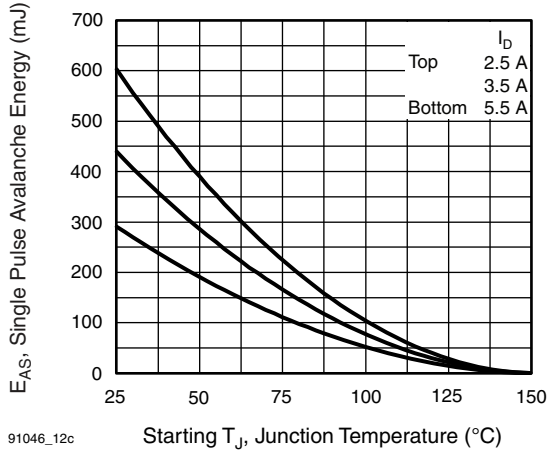
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**

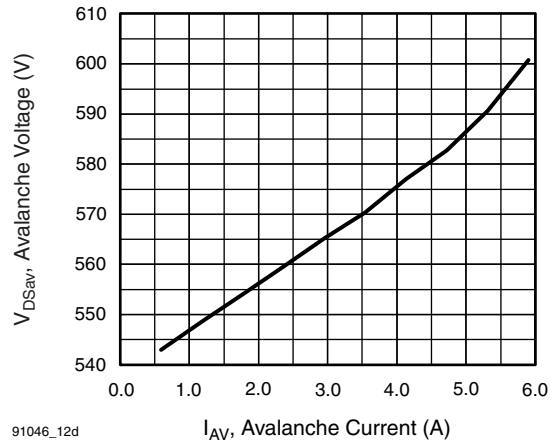


**Fig. 12b - Unclamped Inductive Waveforms**



91046\_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current



91046\_12d

Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

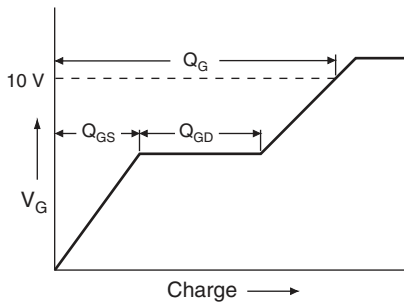


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

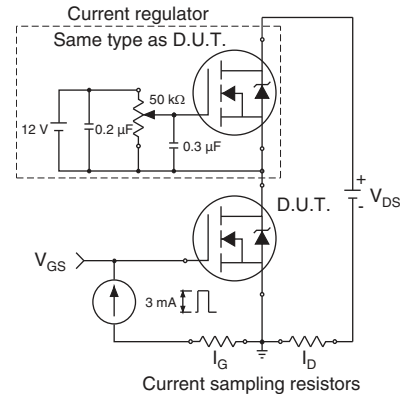
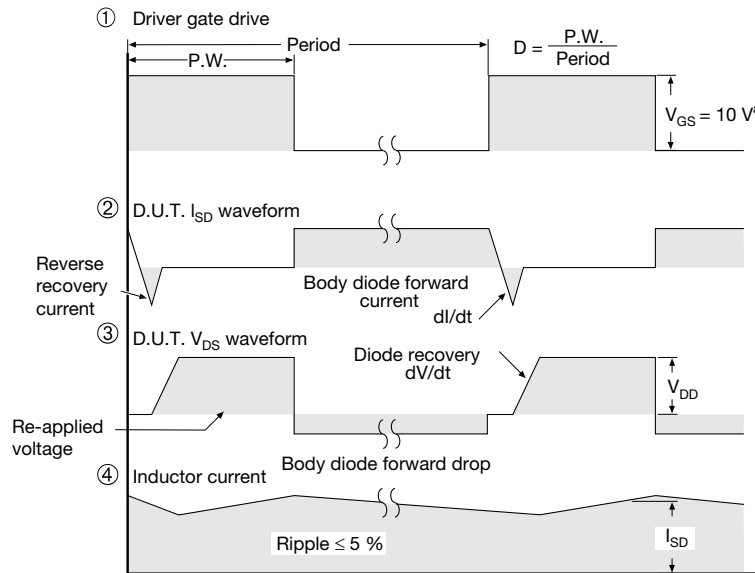
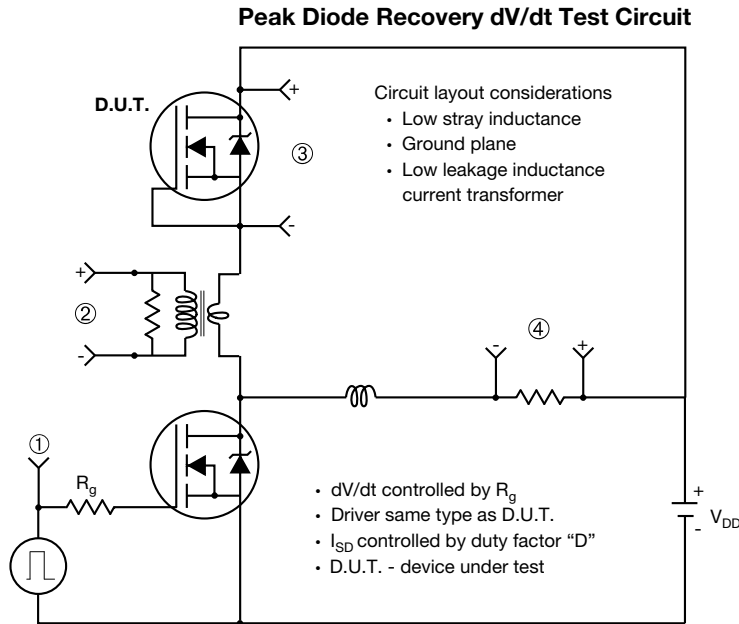


Fig. 13b - Gate Charge Test Circuit



**Note**

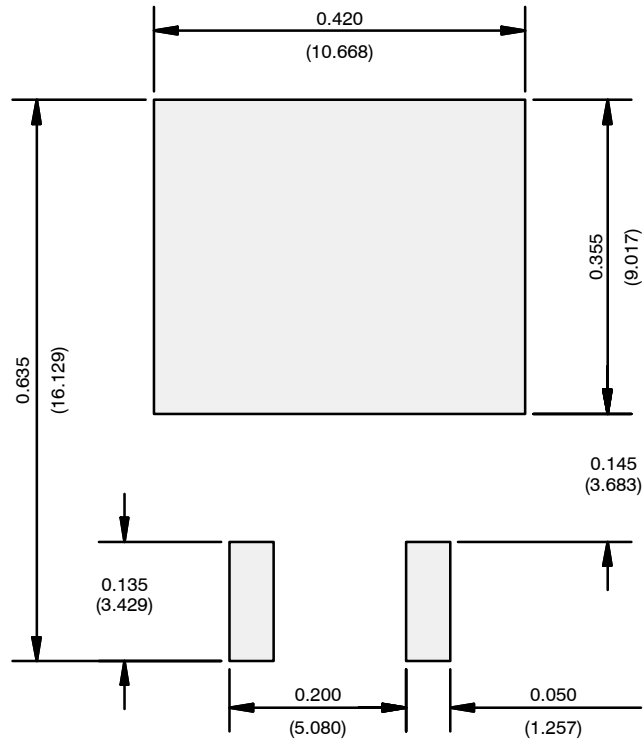
a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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