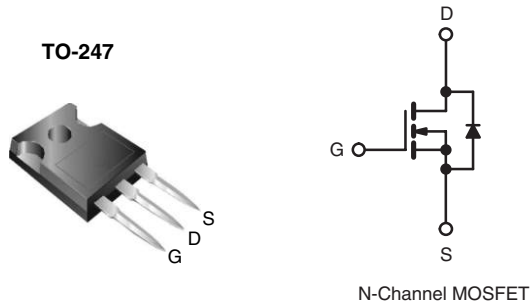


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.18
Q_g (Max.) (nC)	180
Q_{gs} (nC)	56
Q_{gd} (nC)	86
Configuration	Single



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

APPLICATIONS

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive


ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP27N60KPbF
	SiHFP27N60K-E3
SnPb	IRFP27N60K
	SiHFP27N60K

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	600	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current ^a	I_{DM}	110		
Linear Derating Factor		4.0	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b	E_{AS}	530	mJ	
Repetitive Avalanche Current ^a	I_{AR}	27	A	
Repetitive Avalanche Energy ^a	E_{AR}	50	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	500	W
Peak Diode Recovery dV/dt^c		dV/dt	13	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 - Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.4\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 27\text{ A}$, $dV/dt = 13\text{ V/ns}$ (see fig. 12).
 - $I_{SD} \leq 27\text{ A}$, $dI/dt \leq 390\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
 - 1.6 mm from case.
- * Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.29	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	640	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}^b$	-	0.18	0.22	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 16\text{ A}$		14	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$		-	4660	-	pF
Output Capacitance	C_{oss}	$V_{DS} = 25\text{ V}$		-	460	-	
Reverse Transfer Capacitance	C_{riss}	$f = 1.0\text{ MHz}$, see fig. 5		-	41	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	5490	-	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	120	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	250	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 27\text{ A}, V_{DS} = 480\text{ V}$ see fig. 6 and 13 ^b	-	-	180	nC
Gate-Source Charge	Q_{gs}			-	-	56	
Gate-Drain Charge	Q_{gd}			-	-	86	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 27\text{ A}$ $R_G = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}$, see fig. 10 ^b		-	27	-	ns
Rise Time	t_r			-	110	-	
Turn-Off Delay Time	$t_{d(off)}$			-	43	-	
Fall Time	t_f			-	38	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	27	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	110	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 27\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 27\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	620	920	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	11	16	μC
Reverse Recovery Current	I_{RRM}			-	36	53	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

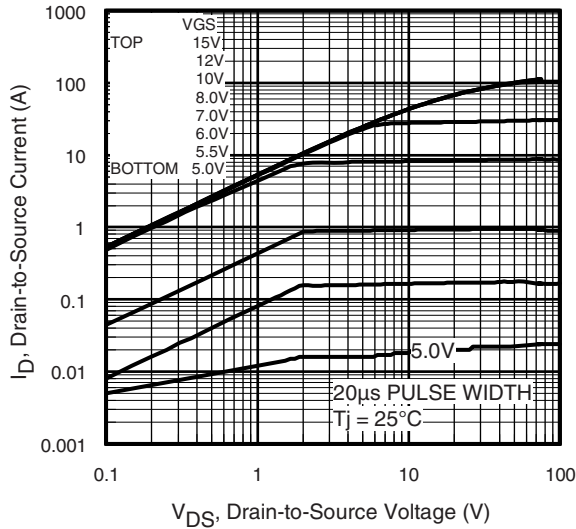


Fig. 1 - Typical Output Characteristics

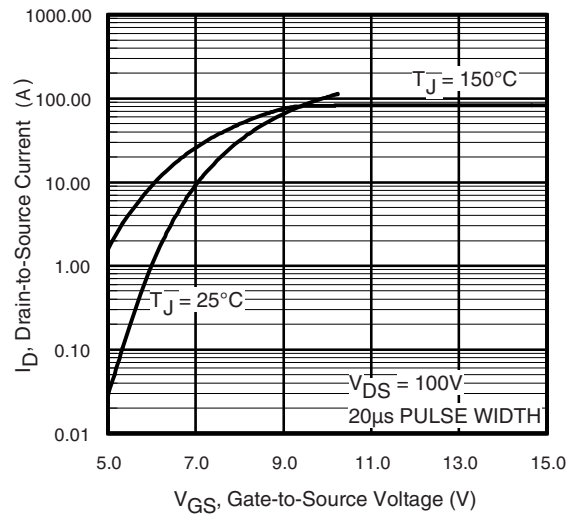


Fig. 3 - Typical Transfer Characteristics

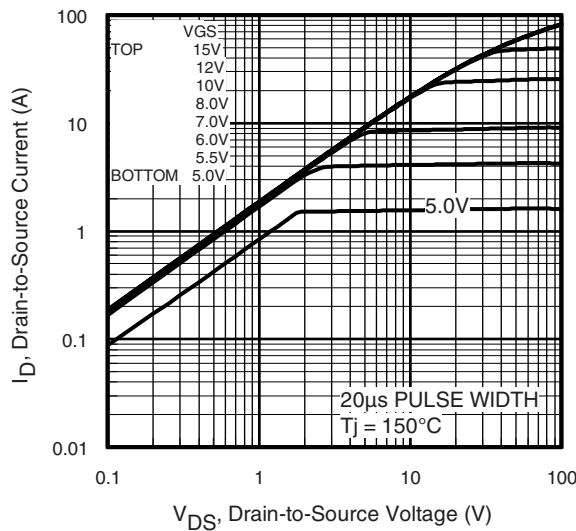


Fig. 2 - Typical Output Characteristics

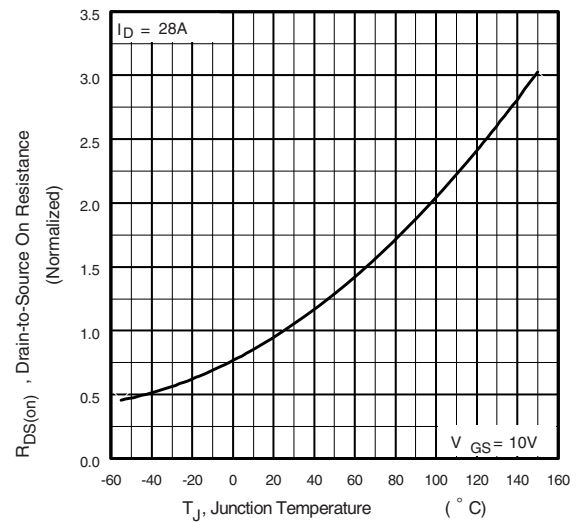


Fig. 4 - Normalized On-Resistance vs. Temperature

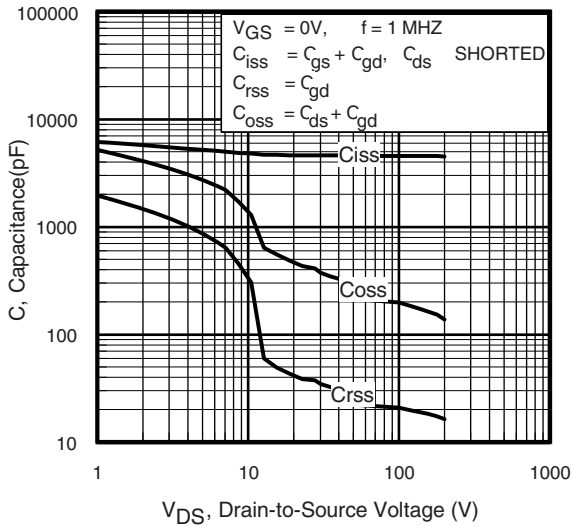


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

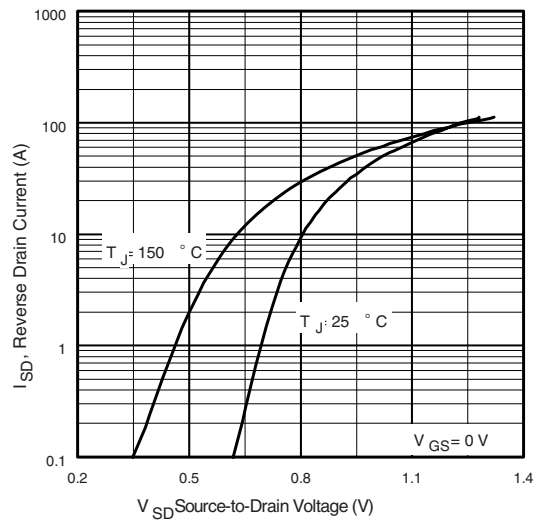


Fig. 7 - Typical Source-Drain Diode Forward Voltage

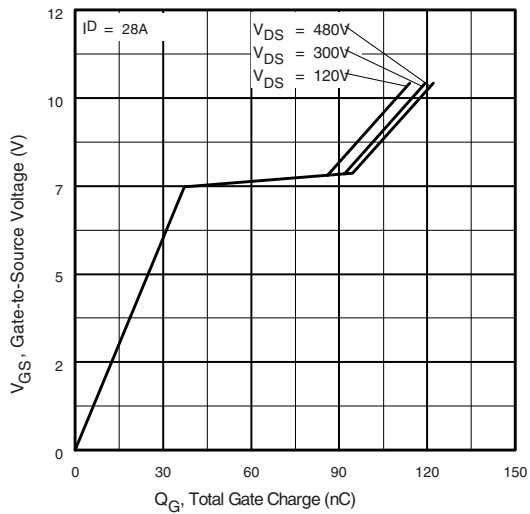


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

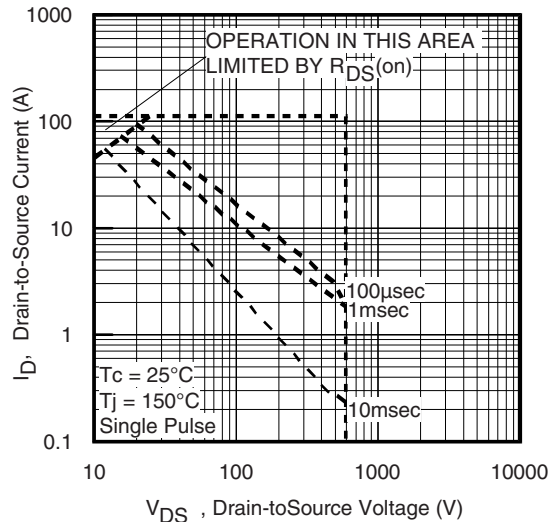


Fig. 8 - Maximum Safe Operating Area

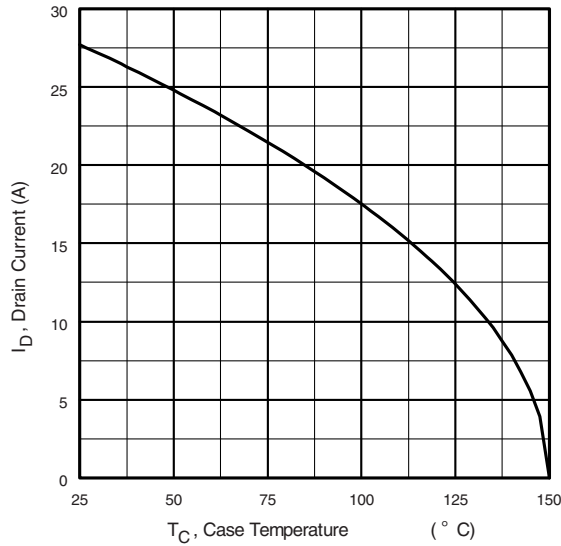


Fig. 9 - Maximum Drain Current vs. Case Temperature

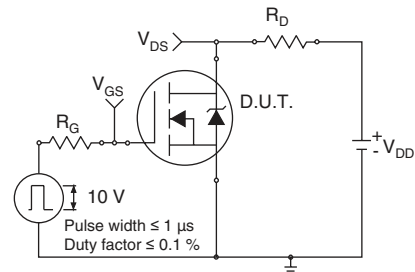


Fig. 10a - Switching Time Test Circuit

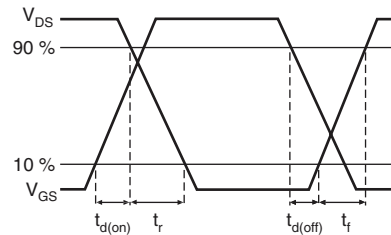


Fig. 10b - Switching Time Waveforms

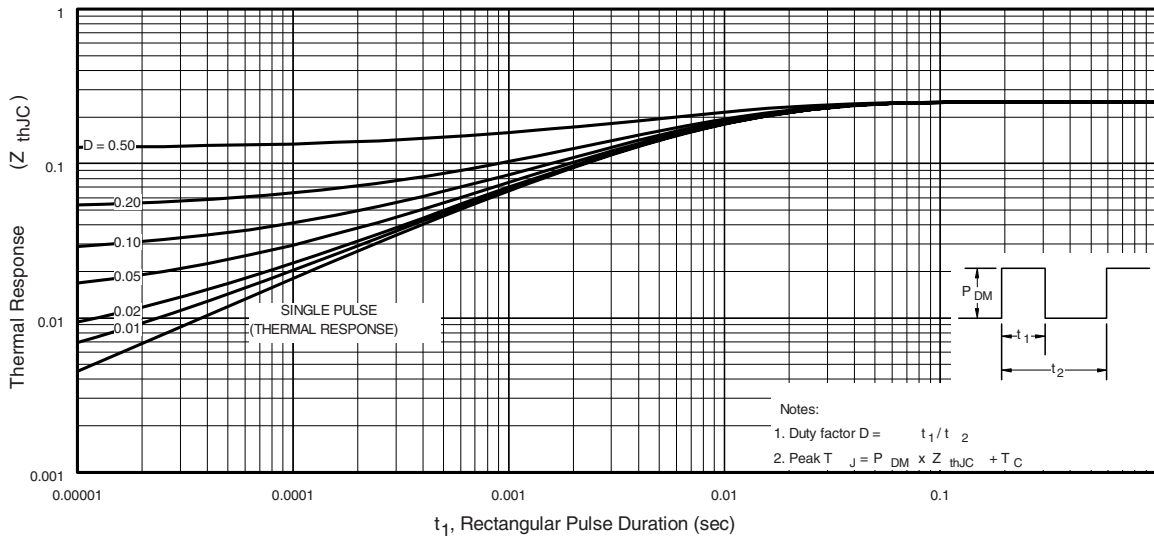


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

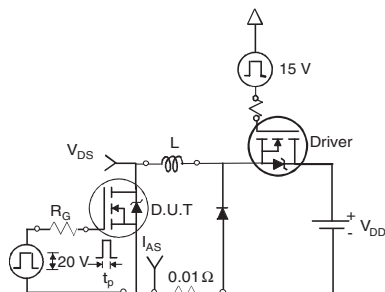


Fig. 12a - Unclamped Inductive Test Circuit

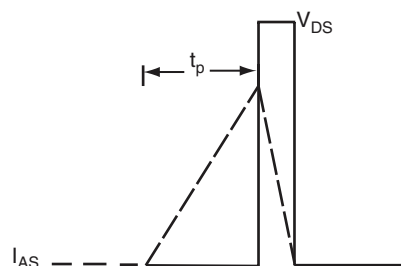


Fig. 12b - Unclamped Inductive Waveforms

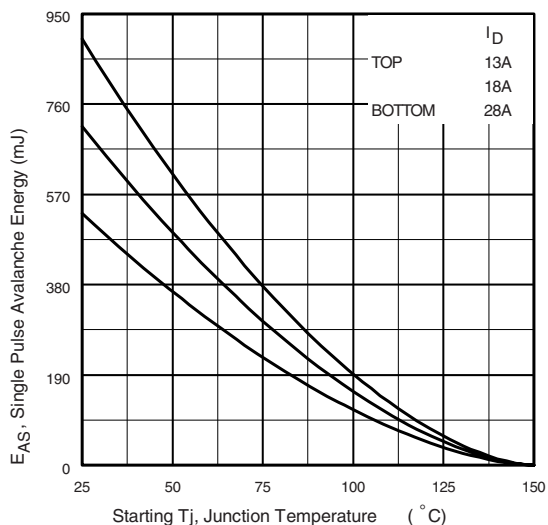


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

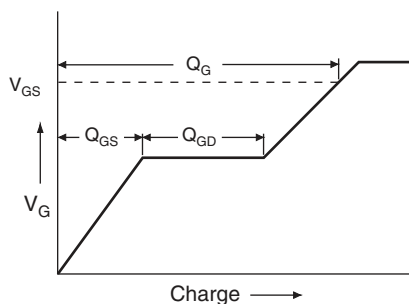


Fig. 13a - Basic Gate Charge Waveform

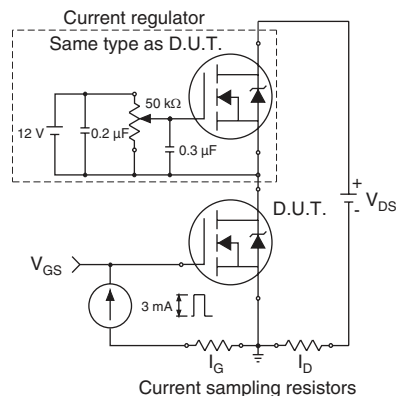
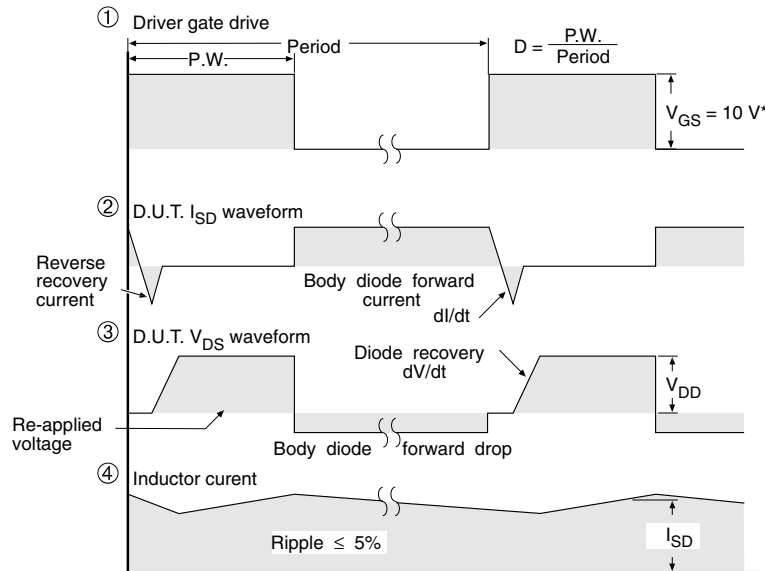
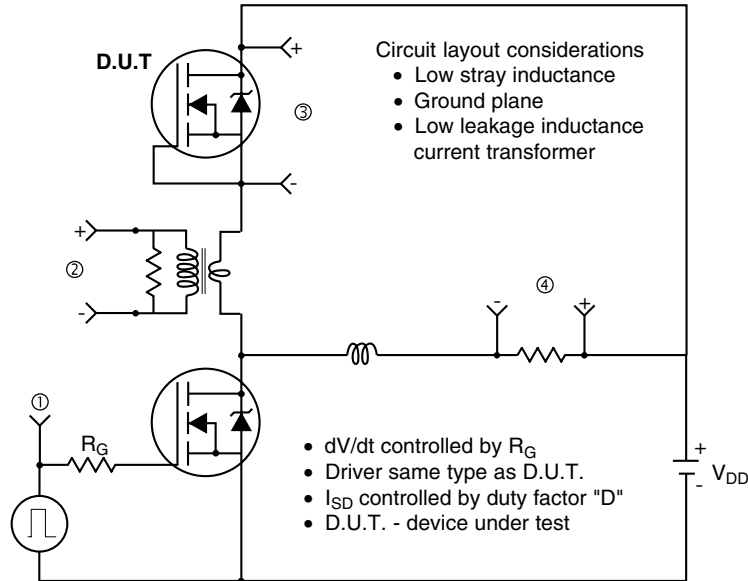


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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