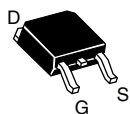
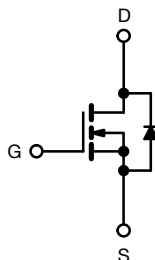
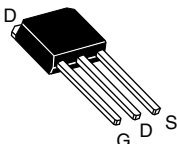




Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	3.0
Q_g max. (nC)	17	
Q_{gs} (nC)	4.3	
Q_{gd} (nC)	8.5	
Configuration	Single	

DPAK
(TO-252)IPAK
(TO-251)

N-Channel MOSFET

FEATURES

- Low gate Charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR420A-GE3	SiHFR420ATR-GE3 ^a	SiHFR420ATRL-GE3	SiHFU420A-GE3
Lead (Pb)-free	IRFR420APbF	IRFR420ATRPbF ^a	IRFR420ATRLPbF	IRFU420APbF

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	3.3	A
		T _C = 100 °C		2.1	
Pulsed Drain Current ^a			I _{DM}	10	
Linear Derating Factor				0.67	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	140	mJ
Repetitive Avalanche Current ^a			I _{AR}	2.5	A
Repetitive Avalanche Energy ^a			E _{AR}	5.0	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	83	W
Peak Diode Recovery dV/dt ^c			dV/dt	3.4	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s			300	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 45\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.5\text{ A}$ (see fig. 12).
c. $I_{SD} \leq 2.5\text{ A}$, $dI/dt \leq 270\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
d. 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.5	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.60	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.5	V	
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA	
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.5 A ^b	-	-	3.0	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.5 A		1.4	-	-	S	
Dynamic								
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	340	-	pF	
Output Capacitance	C _{oss}			-	53	-		
Reverse Transfer Capacitance	C _{rss}			-	2.7	-		
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	490	-	pF	
Effective Output Capacitance	C _{oss} eff.		V _{DS} = 400 V, f = 1.0 MHz	-	15	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	V _{DS} = 0 V to 400 V ^c	-	28	-	nC	
Gate-Source Charge	Q _{gs}		I _D = 2.5 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	17		
Gate-Drain Charge	Q _{gd}		-	-	-	4.3		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 2.5 A, R _g = 21 Ω, R _D = 97 Ω, see fig. 10 ^b		-	-	8.1	ns	
Rise Time	t _r			-	-	12		-
Turn-Off Delay Time	t _{d(off)}			-	-	16		-
Fall Time	t _f			-	-	13		-
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.3	A	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	10		
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 2.5 A, V _{GS} = 0 V ^b		-	-	1.6	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 2.5 A, dI/dt = 100 A/μs ^b		-	330	500	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			-	760	1140	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

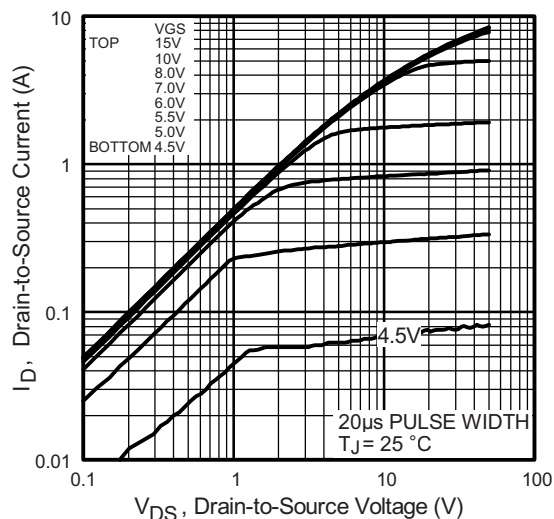


Fig. 1 - Typical Output Characteristics

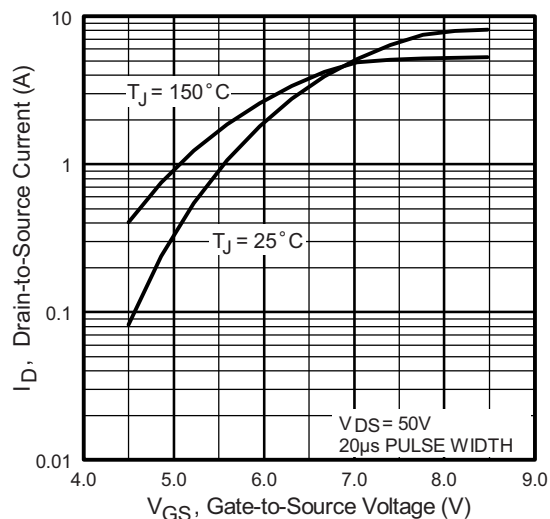


Fig. 3 - Typical Transfer Characteristics

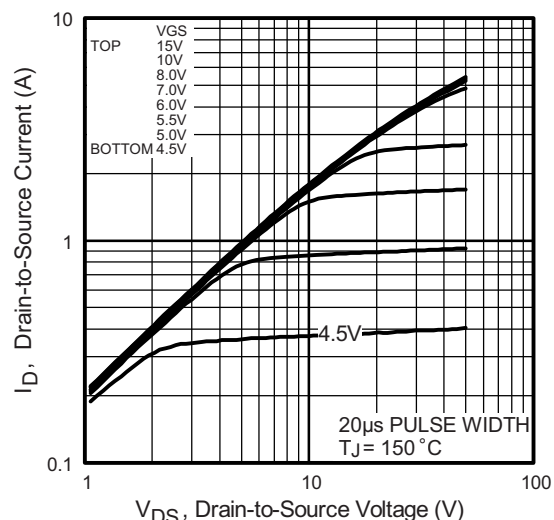


Fig. 2 - Typical Output Characteristics

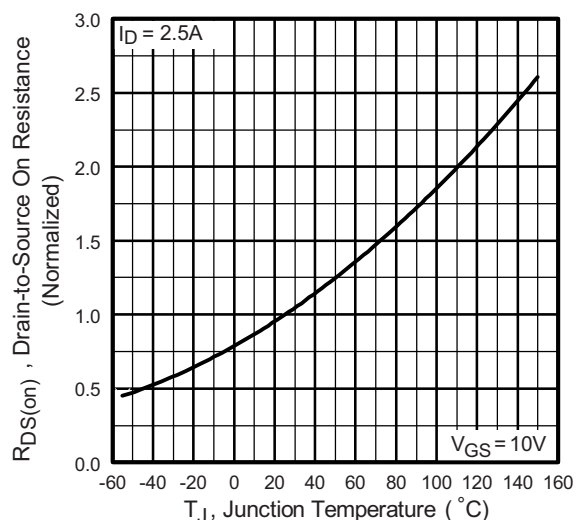
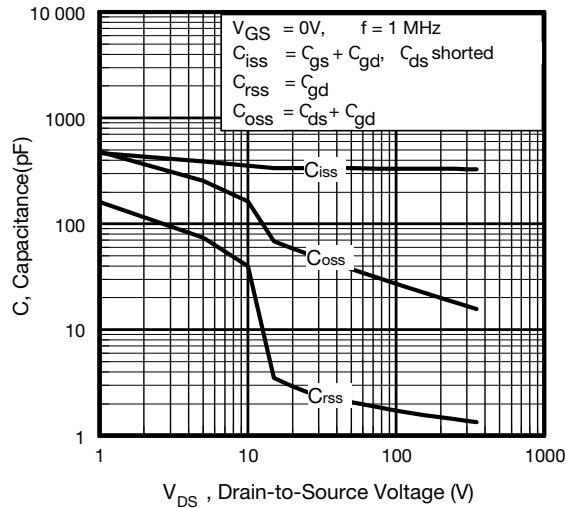
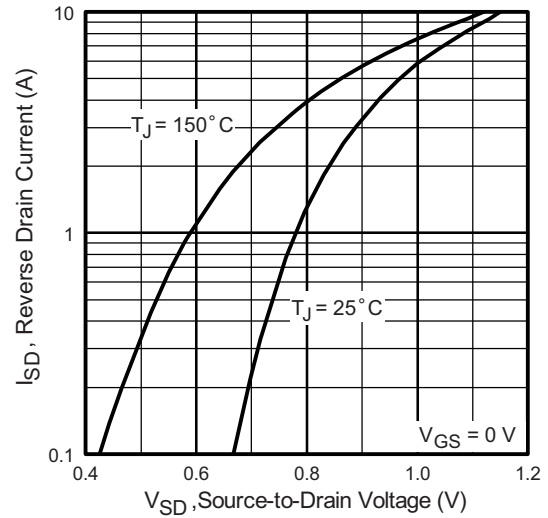
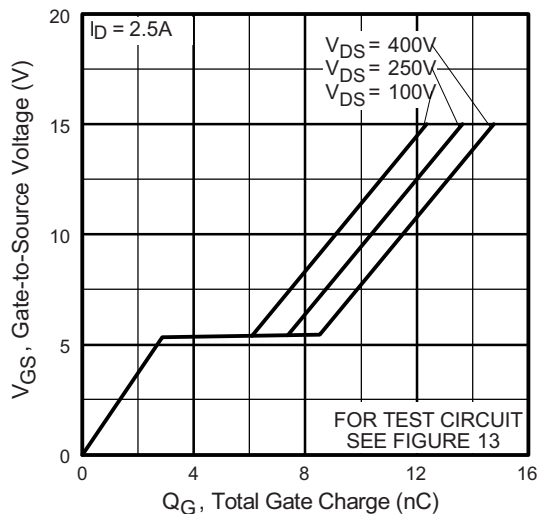
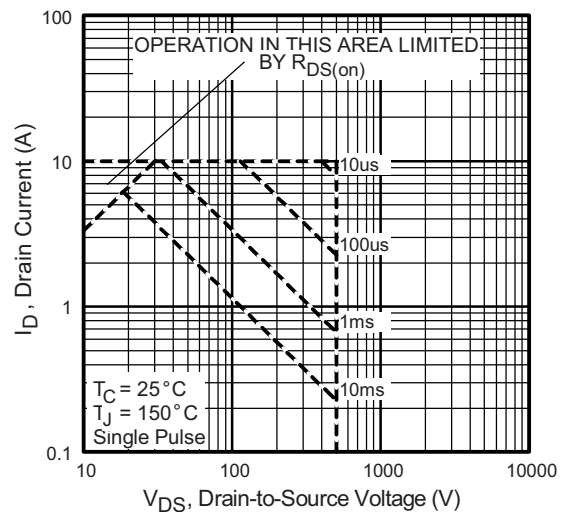


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

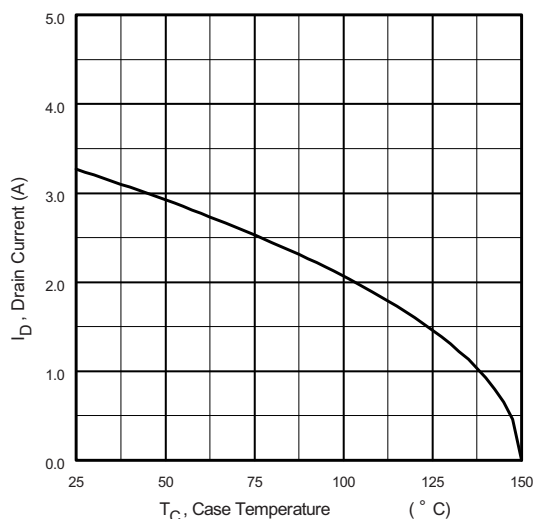


Fig. 9 - Maximum Drain Current vs. Case Temperature

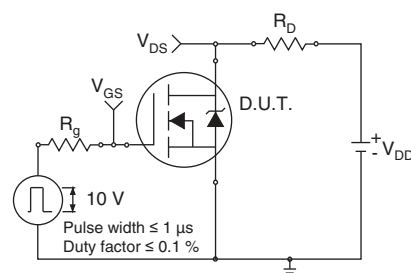


Fig. 10a - Switching Time Test Circuit

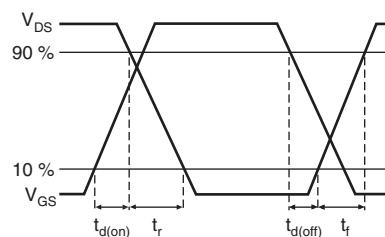


Fig. 10b - Switching Time Waveforms

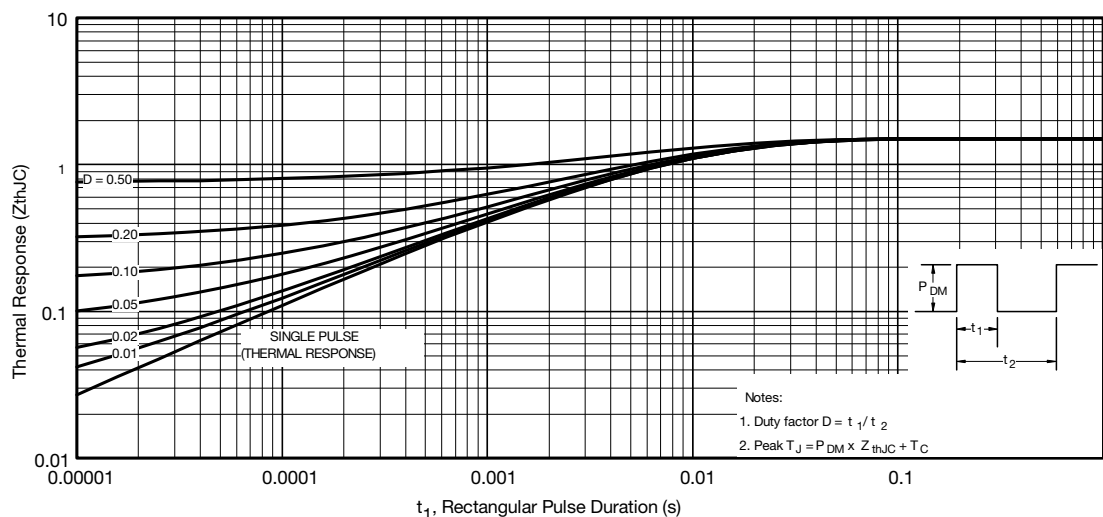


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

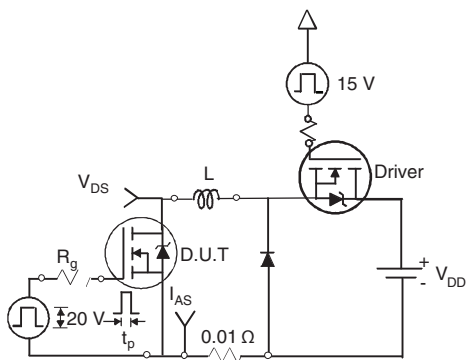


Fig. 12a - Unclamped Inductive Test Circuit

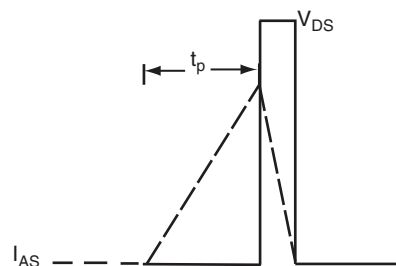
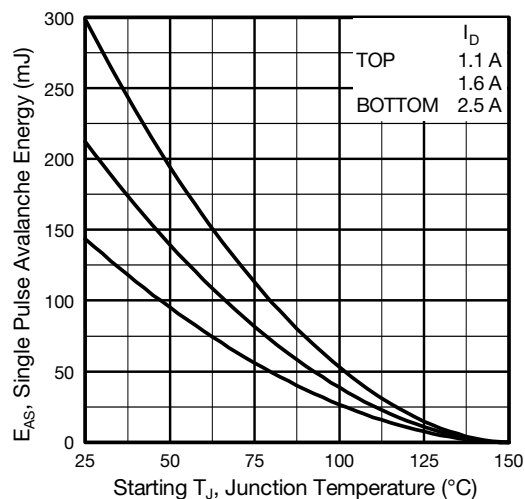
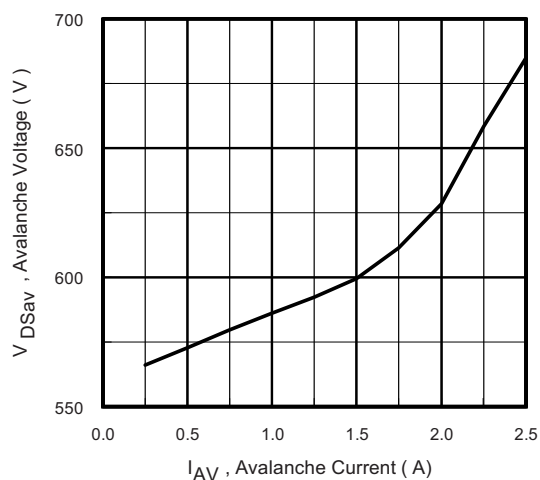
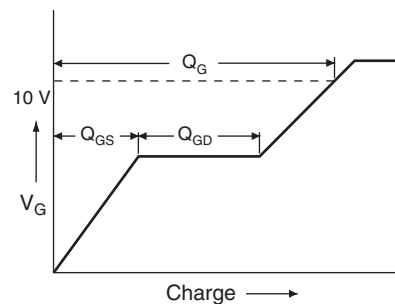
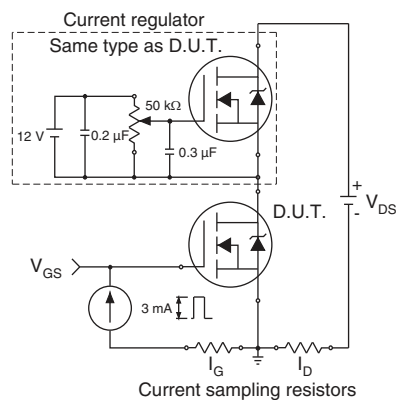
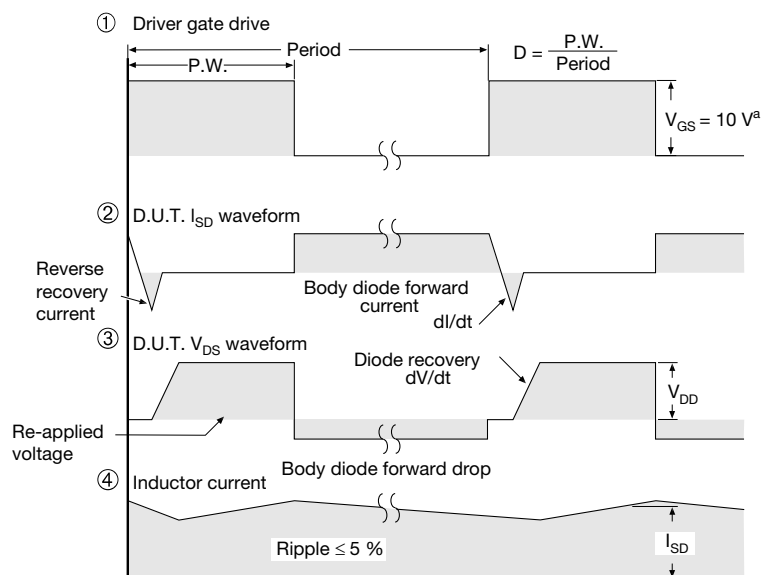
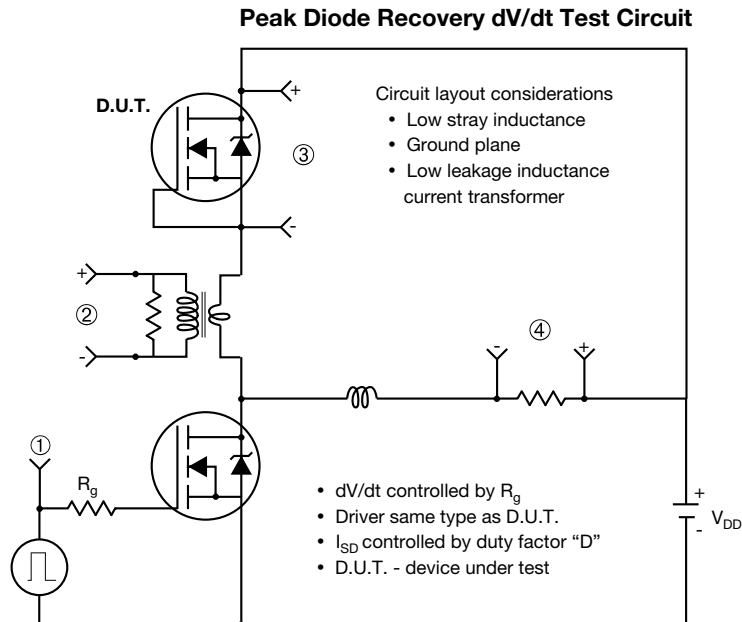


Fig. 12b - Unclamped Inductive Waveforms


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 12d - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit



Note

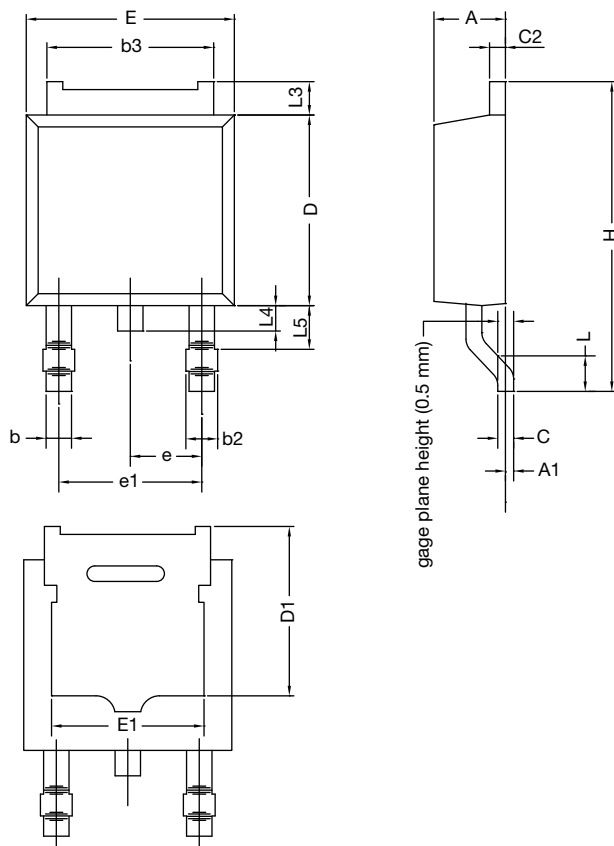
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-252AA Case Outline

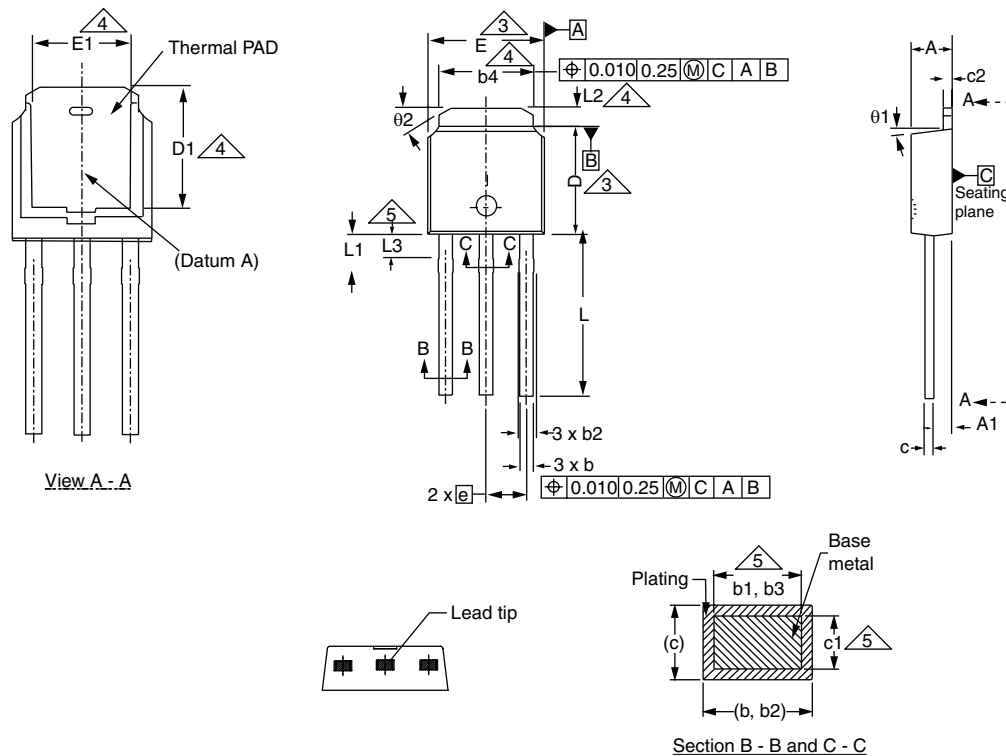


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

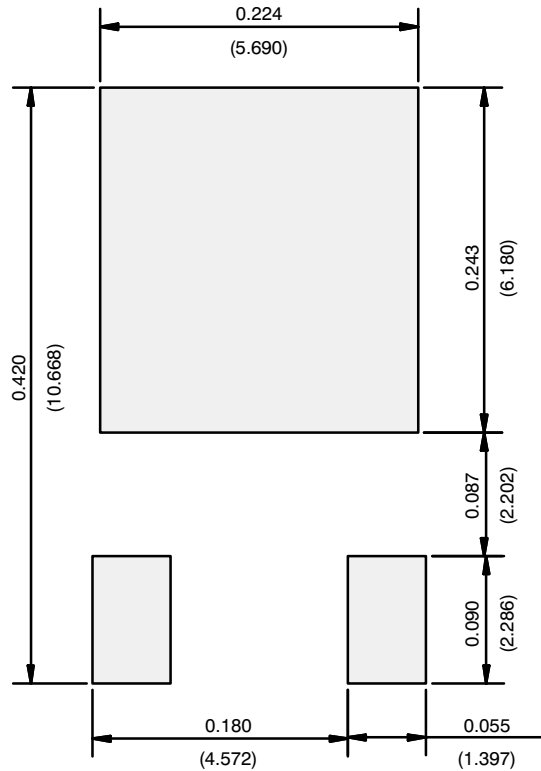
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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