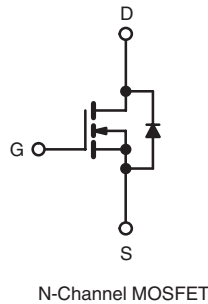
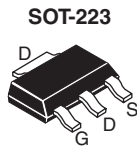


Power MOSFET

| PRODUCT SUMMARY | | |
|---------------------------|------------------|------|
| V_{DS} (V) | 100 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 5.0$ V | 0.54 |
| Q_g (Max.) (nC) | 6.1 | |
| Q_{gs} (nC) | 2.6 | |
| Q_{gd} (nC) | 3.3 | |
| Configuration | Single | |



FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

| ORDERING INFORMATION | | |
|----------------------|-------------|---------------------------|
| Package | SOT-223 | SOT-223 |
| Lead (Pb)-free | IRLL110PbF | IRLL110TRPbF ^a |
| | SiHLL110-E3 | SiHLL110T-E3 ^a |
| SnPb | IRLL110 | IRLL110TR ^a |
| | SiHLL110 | SiHLL110T ^a |

Note

- a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted | | | | |
|--|-------------------|-------|------------------|------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V_{DS} | | 100 | V |
| Gate-Source Voltage | V_{GS} | | ± 10 | |
| Continuous Drain Current | V_{GS} at 5.0 V | I_D | $T_C = 25$ °C | 1.5 |
| | | | $T_C = 100$ °C | 0.93 |
| Pulsed Drain Current ^a | I_{DM} | | 12 | A |
| Linear Derating Factor | | | 0.025 | |
| Linear Derating Factor (PCB Mount) ^e | | | 0.017 | |
| Single Pulse Avalanche Energy ^b | E_{AS} | | 50 | mJ |
| Repetitive Avalanche Current ^a | I_{AR} | | 1.5 | A |
| Repetitive Avalanche Energy ^a | E_{AR} | | 0.31 | mJ |
| Maximum Power Dissipation | $T_C = 25$ °C | | 3.1 | W |
| | $T_A = 25$ °C | | | |
| Maximum Power Dissipation (PCB Mount) ^e | | | 2.0 | |
| Peak Diode Recovery dV/dt ^c | dV/dt | | 5.5 | V/ns |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | 300 ^d | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 25$ mH, $R_G = 25$ Ω , $I_{AS} = 1.5$ A (see fig. 12).
 c. $I_{SD} \leq 5.6$ A, $di/dt \leq 75$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
 d. 1.6 mm from case.
 e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|--|------------|------|------|------|
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | 60 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 40 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|--|---------------------|---|---|------|-----------|---------------|----|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 100 | - | - | V | |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C , $I_D = 1\text{ mA}$ | - | 0.12 | - | V/°C | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 1.0 | - | 2.0 | V | |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 10\text{ V}$ | - | - | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | 25 | μA | |
| | | $V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$ | - | - | 250 | | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 5.0\text{ V}$ | - | - | 0.54 | Ω | |
| | | $V_{GS} = 4.0\text{ V}$ | - | - | 0.76 | | |
| Forward Transconductance | g_{fs} | $V_{DS} = 25\text{ V}$, $I_D = 0.90\text{ A}$ | 0.57 | - | - | S | |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | - | 250 | - | pF | |
| Output Capacitance | C_{oss} | | - | 80 | - | | |
| Reverse Transfer Capacitance | C_{rss} | | - | 15 | - | | |
| Total Gate Charge | Q_g | $V_{GS} = 5.0\text{ V}$ | $I_D = 5.6\text{ A}$, $V_{DS} = 80\text{ V}$, see fig. 6 and 13 ^b | - | - | 6.1 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 2.6 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 3.3 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}$, $I_D = 5.6\text{ A}$, $R_G = 12\text{ }\Omega$, $R_D = 8.4\text{ }\Omega$ | - | 9.3 | - | ns | |
| Rise Time | t_r | | - | 47 | - | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 16 | - | | |
| Fall Time | t_f | | - | 18 | - | | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | - | 4.0 | - | nH | |
| Internal Source Inductance | L_S | | - | 6.0 | - | | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode | - | - | 1.5 | A | |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 12 | | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ °C}$, $I_S = 1.5\text{ A}$, $V_{GS} = 0\text{ V}$ ^b | - | - | 2.5 | V | |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ °C}$, $I_F = 5.6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$ ^b | - | 110 | 130 | ns | |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 0.50 | 0.65 | μC | |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

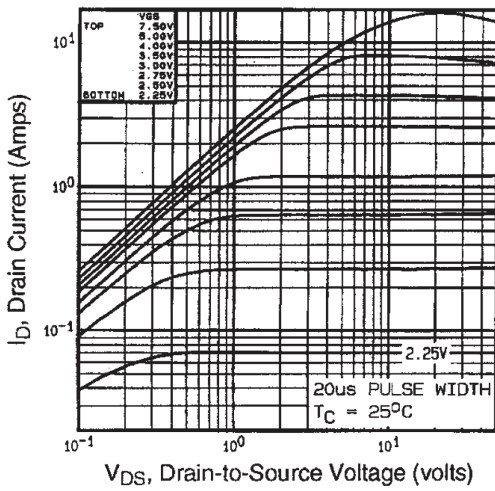


Fig. 1 - Typical Output Characteristics

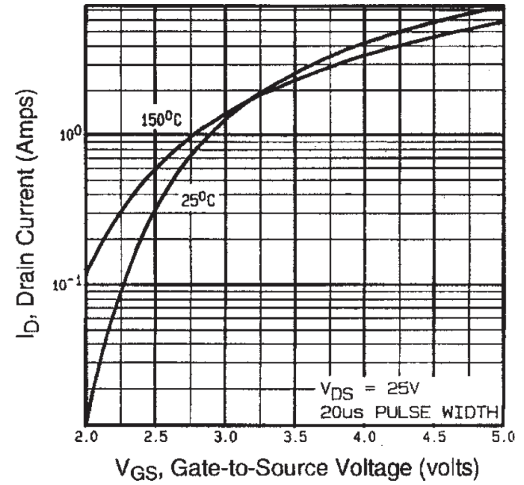


Fig. 3 - Typical Transfer Characteristics

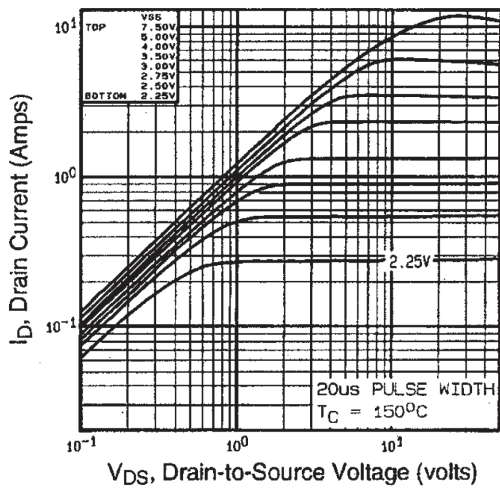


Fig. 2 - Typical Output Characteristics

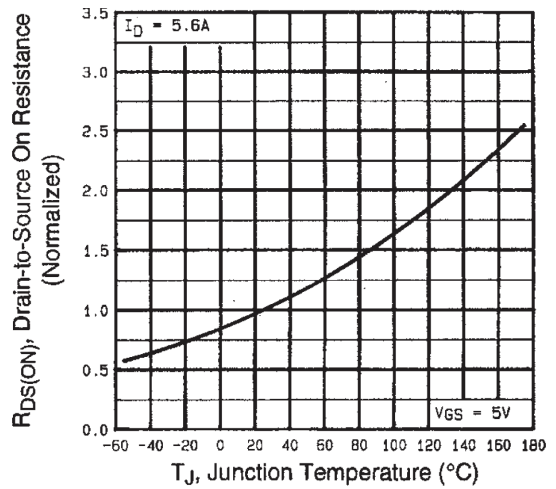


Fig. 4 - Normalized On-Resistance vs. Temperature

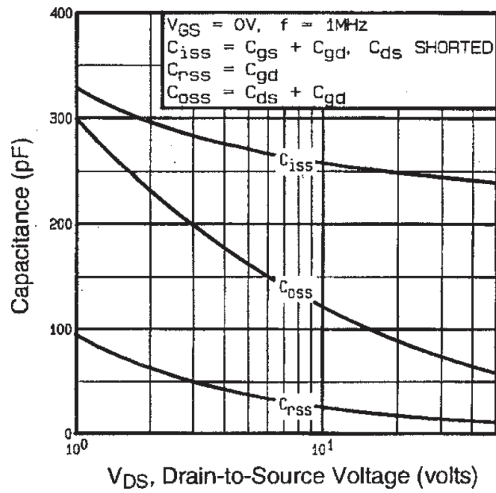


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

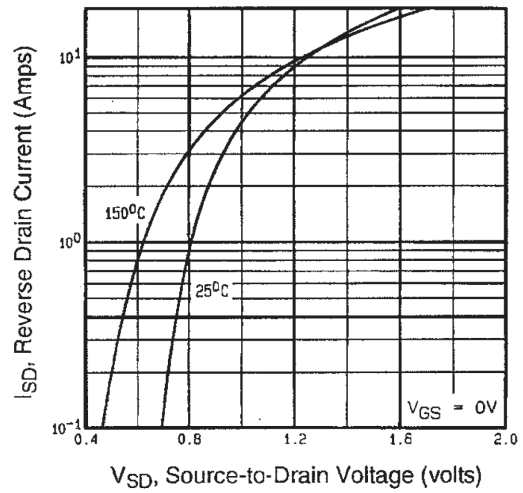


Fig. 7 - Typical Source-Drain Diode Forward Voltage

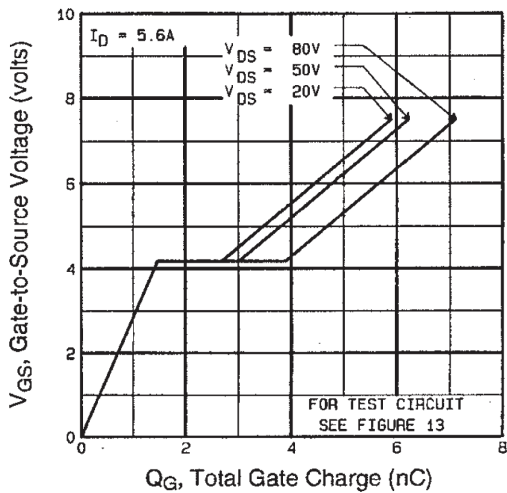


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

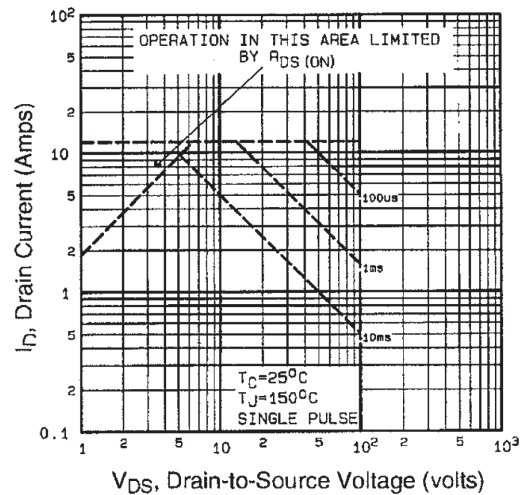


Fig. 8 - Maximum Safe Operating Area

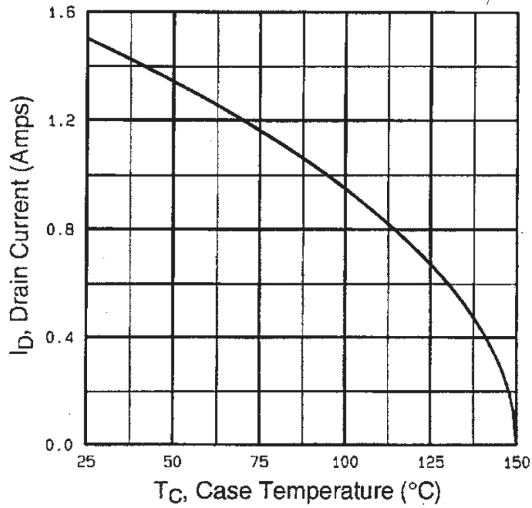


Fig. 9 - Maximum Drain Current vs. Case Temperature

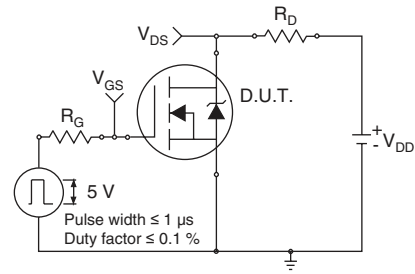


Fig. 10a - Switching Time Test Circuit

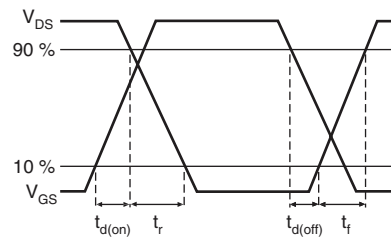


Fig. 10b - Switching Time Waveforms

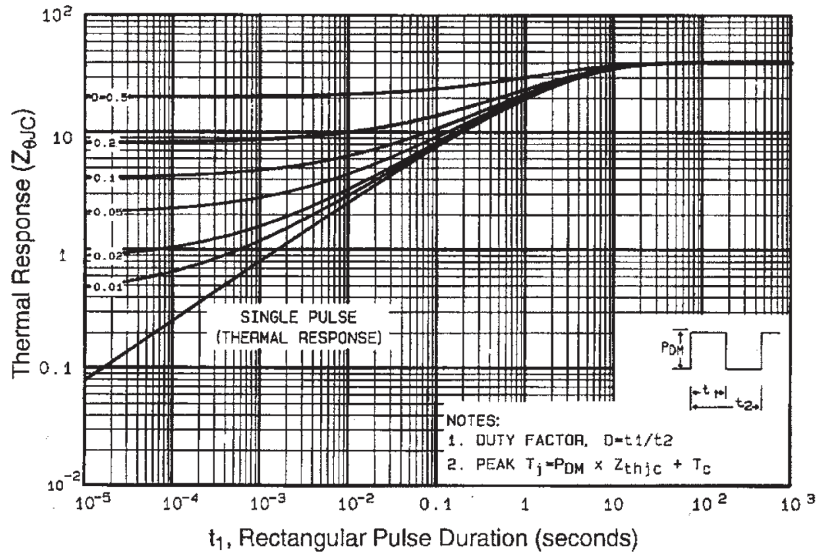


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

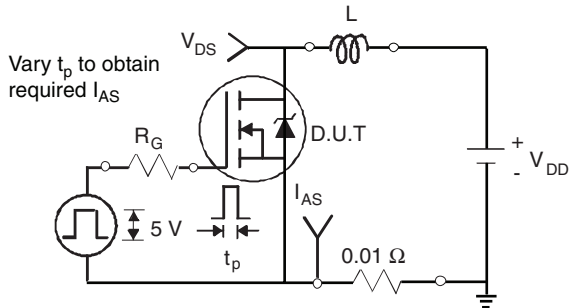


Fig. 12a - Unclamped Inductive Test Circuit

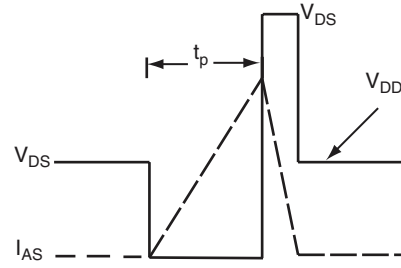


Fig. 12b - Unclamped Inductive Waveforms

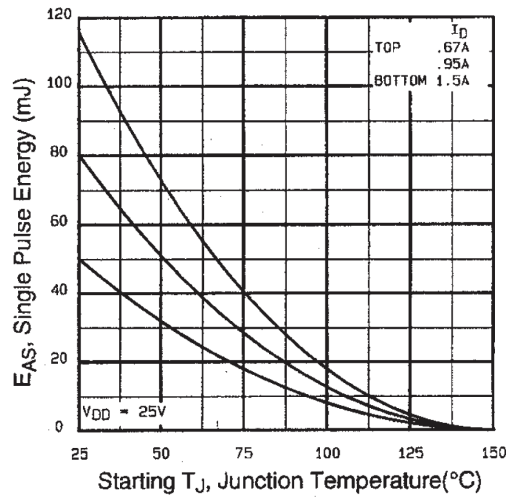


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

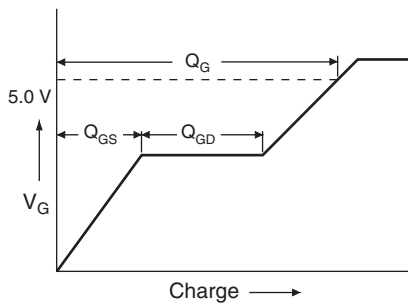


Fig. 13a - Basic Gate Charge Waveform

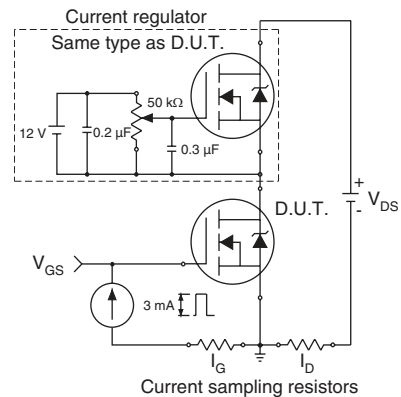
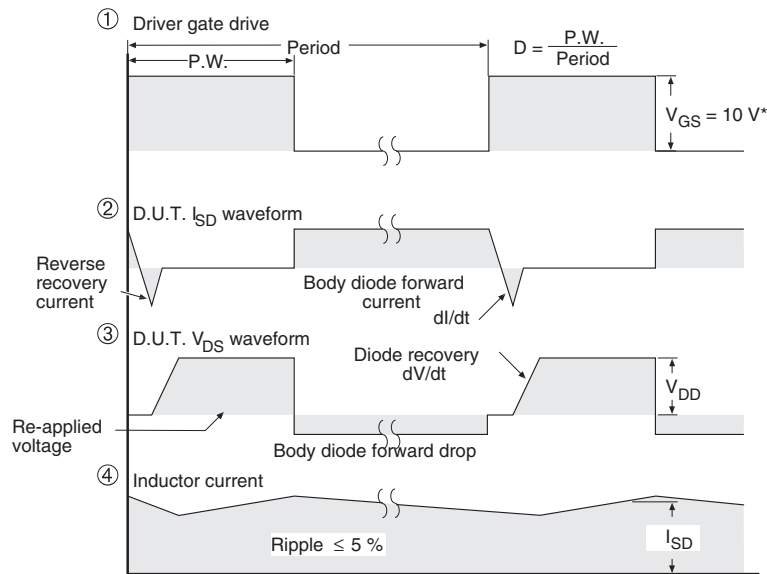
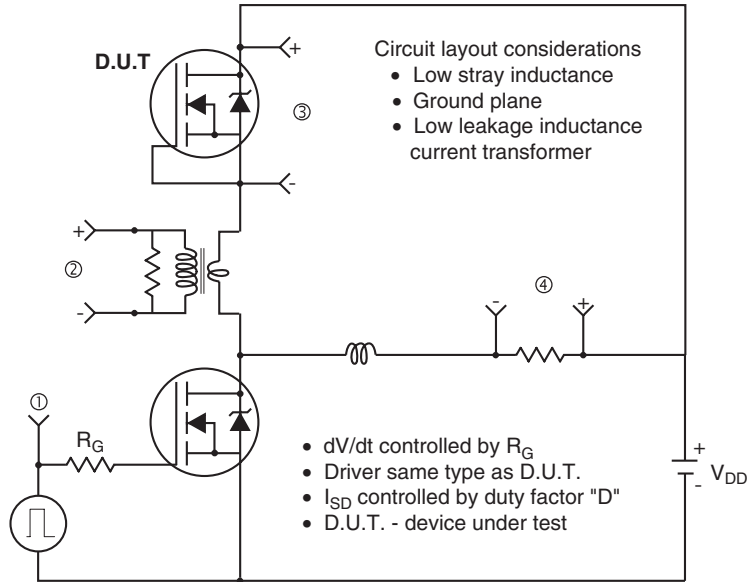


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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