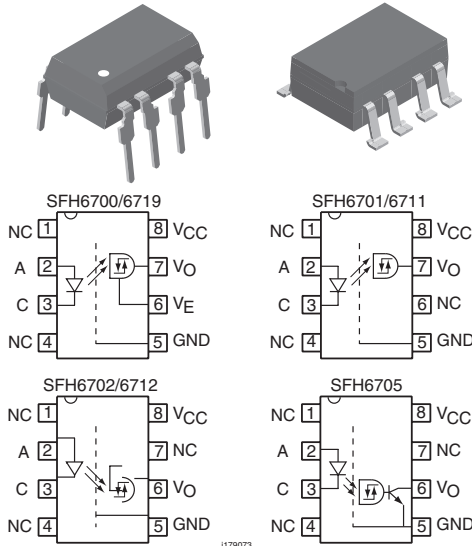


High Speed Optocoupler, 5 MBd, 1 kV/ μ s dV/dt



DESCRIPTION

The SFH67xx high speed optocoupler series consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector. The detector incorporates a Schmitt-Trigger stage for improved noise immunity. Using the enable input, the output can be switched to the high ohmic state, which is necessary for data bus applications. A Faraday shield provides a common mode transient immunity of 1000 V/ μ at $V_{CM} = 50$ V for SFH6700/01/02/05 and 2500 V/ μ at $V_{CM} = 400$ V for SFH6711/12/19. The SFH67xx uses an industry standard DIP-8 package. With standard lead bending, creepage distance and clearance of ≥ 7.0 mm with lead bending options 6, 7, and 9 ≥ 8 mm are achieved.

FEATURES

- Data rate 5.0 MBits/s (2.5 MBit/s over temperature)
- Buffer
- Isolation test voltage, 5300 V_{RMS} for 1.0 s
- TTL, LSTTL and CMOS compatible
- Internal shield for very high common mode transient immunity
- Wide supply voltage range (4.5 to 15 V)
- Low input current (1.6 mA to 5 mA)
- Three state output (SFH6700/19)
- Totem pole output (SFH6701/02/11/12)
- Open collector output (SFH6705)
- Lead (Pb)-free component
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC


**RoHS
COMPLIANT**

APPLICATIONS

- Industrial control
- Replace pulse transformers
- Routine logic interfacing
- Motion/power control
- High speed line receiver
- Microprocessor system interfaces
- Computer peripheral interfaces

AGENCY APPROVALS

- UL1577, file no. E52744 system code H or J, double protection
- DIN EN 60747-5-2 (VDE 0884)/DIN EN 60747-5-5 pending available with option 1

ORDER INFORMATION

PART	REMARKS
SFH6700	Three state output, DIP-8
SFH6701	Totem pole output, DIP-8
SFH6702	Totem pole output, DIP-8
SFH6705	Open collector output, DIP-8
SFH6711	Totem pole output, DIP-8
SFH6712	Totem pole output, DIP-8
SFH6719	Three state output, DIP-8
SFH6700-X009	Three state output, SMD-8 (option 9)
SFH6701-X006	Totem pole output, DIP-8 400 mil (option 6)
SFH6701-X007	Totem pole output, SMD-8 (option 7)
SFH6701-X009	Totem pole output, SMD-8 (option 9)
SFH6705-X006	Open collector output, DIP-8 400 mil (option 6)
SFH6705-X007	Open collector output, SMD-8 (option 7)
SFH6711-X007	Totem pole output, SMD-8 (option 7)

Note

For additional information on the available options refer to option information.

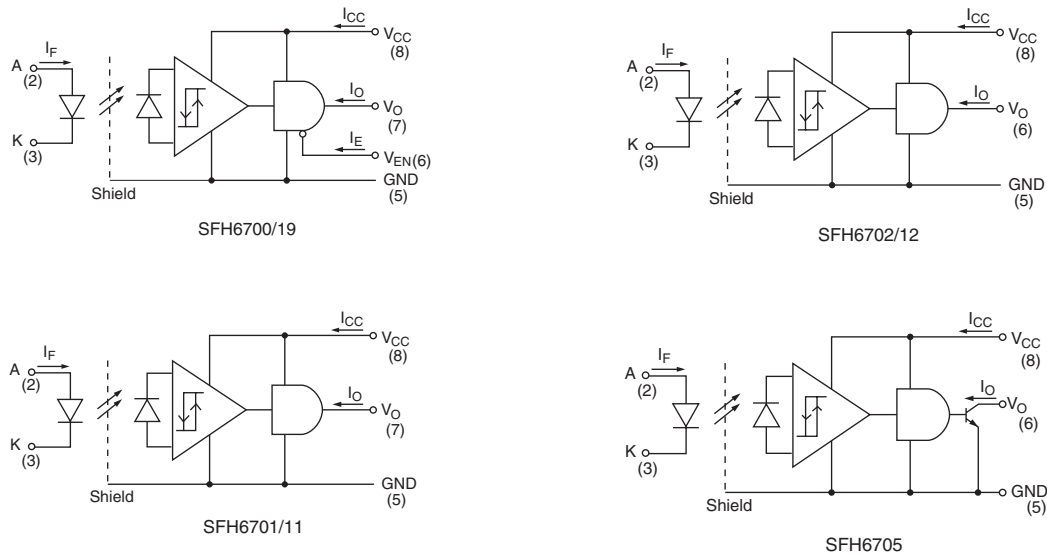
TRUTH TABLE (Positive Logic)			
PARTS	IR DIODE	ENABLE	OUTPUT
SFH6700	on	H	Z
	off	H	Z
SFH6719	on	L	H
	off	L	L
SFH6701	on		H
	off		L
SFH6702	on		H
	off		L
SFH6705	on		H
	off		L
SFH6711	on		H
	off		L
SFH6712	on		H
	off		L

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
INPUT				
Reverse voltage		V_R	3.0	V
DC forward current		I_F	10	mA
Surge forward current	$t \leq 1.0 \mu\text{s}$	I_{FSM}	1.0	A
Power dissipation		P_{diss}	20	mW
OUTPUT				
Supply voltage		V_{CC}	- 0.5 to + 15	V
Three state enable voltage (SFH6700/19 only)		V_{EN}	- 0.5 to + 15	V
Output voltage		V_O	- 0.5 to + 15	V
Average output current		I_O	25	mA
Power dissipation		P_{diss}	100	mW
COUPLER				
Storage temperature range		T_{stg}	- 55 to + 125	$^{\circ}\text{C}$
Ambient temperature range		T_{amb}	+ 85	$^{\circ}\text{C}$
Lead soldering temperature	$t = 10 \text{ s}$	T_{sld}	260	$^{\circ}\text{C}$
Isolation test voltage		V_{ISO}	5300	V_{RMS}
Pollution degree			2.0	
Creepage distance and clearance	Standard lead bending		7.0	mm
	Options 6, 7, 9		8.0	mm
Comparative tracking index per DIN IEC 112/VDE 0303, part 1			175	
Isolation resistance	$V_{IO} = 500 \text{ V}, T_{amb} = 25 \text{ }^{\circ}\text{C}$	R_{IO}	10^{12}	Ω
	$V_{IO} = 500 \text{ V}, T_{amb} = 100 \text{ }^{\circ}\text{C}$	R_{IO}	10^{11}	Ω

Note

$T_{amb} = 25 \text{ }^{\circ}\text{C}$, unless otherwise specified.

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.



isfh6700_01

Fig. 1 - Schematics

RECOMMENDED OPERATING CONDITIONS (1)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage			V_{CC}	4.5		15	V
Enable voltage high		SFH6700	V_{EH}	2.0		15	V
		SFH6719	V_{EH}	2.0		15	V
Enable voltage low		SFH6700	V_{EL}	0		0.8	V
		SFH6719	V_{EL}	0		0.8	V
Forward input current			I_{Fon}	1.6 (2)		5.0	mA
			I_{Foff}			0.1	mA
Operating temperature			T_{amb}	- 40		85	°C
Output pull-up resistor		SFH6705	R_L	350		4	kΩ
Fan output	$R_L = 1.0\text{ k}\Omega$	SFH6705	N			16	LS TTL loads

Notes

(1) A 0.1 μF bypass capacitor connected between pins 5 and 8 must be used.

(2) We recommended using a 2.2 mA to permit at least 20 % CTR degradation guard band.

ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Forward voltage	$I_F = 5.0 \text{ mA}$	V_F		1.6	1.75	V
	$I_F = 5.0 \text{ mA}$	V_F			1.8	V
Input current hysteresis	$V_{CC} = 5.0 \text{ V}, I_{HYS} = I_{Fon} - I_{Foff}$	I_{HYS}		0.1		mA
Reverse current	$V_R = 3.0 \text{ V}$	I_R		0.5	10	μ A
Capacitance	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$	C_O		60		pF
Thermal resistance		R_{thJA}		700		K/W
OUTPUT						
Logic low output voltage	$I_{OL} = 6.4 \text{ mA}$	V_{OL}			0.5	V
Logic high output voltage (except SFH6705)	$I_{OH} = 2.6 \text{ mA}, V_{OH} = V_{CC} - 1.8 \text{ V}$		2.4			V
Output leakage current ($V_{OUT} > V_{CC}$) (except SFH6705)	$V_O = 5.5 \text{ V}, V_{CC} = 4.5 \text{ V}, I_F = 5.0 \text{ mA}$	I_{OHH}		0.5	100	μ A
	$V_O = 15 \text{ V}, V_{CC} = 4.5 \text{ V}, I_F = 5.0 \text{ mA}$	I_{OHH}		1.0	500	μ A
Output leakage current (SFH6705 only)	$V_O = 5.5 \text{ V}, V_{CC} = 5.5 \text{ V}, I_F = 5.0 \text{ mA}$	I_{OHH}		0.5	100	μ A
	$V_O = 15 \text{ V}, V_{CC} = 15 \text{ V}, I_F = 5.0 \text{ mA}$	I_{OHH}		1.0	500	μ A
Logic high enable voltage (SFH6700/19 only)		V_{EH}	2.0			V
Logic low enable voltage (SFH6700/19 only)		V_{EL}			0.8	V
Logic high enable current (SFH6700/19 only)	$V_{EN} = 2.7 \text{ V}$	I_{EH}			20	μ A
	$V_{EN} = 5.5 \text{ V}$	I_{EH}			100	μ A
	$V_{EN} = 15 \text{ V}$	I_{EH}		0.001	250	μ A
Logic low enable current (SFH6700/19 only)	$V_{EN} = 0.4 \text{ V}$	I_{EL}	- 320	- 50		μ A
High impedance state output current (SFH6700/19 only)	$V_O = 0.4 \text{ V}, V_{EN} = 2.0 \text{ V}, I_F = 5.0 \text{ mA}$	I_{OZL}	- 20			μ A
	$V_O = 2.4 \text{ V}, V_{EN} = 2.0 \text{ V}, I_F = 0 \text{ mA}$	I_{OZH}			20	μ A
	$V_O = 5.5 \text{ V}, V_{EN} = 2.0 \text{ V}, I_F = 0 \text{ mA}$	I_{OZH}		0.001	500	μ A
Logic low supply current	$V_{CC} = 5.5 \text{ V}, I_F = 0$	I_{CCL}		3.7	6.0	mA
	$V_{CC} = 15 \text{ V}, I_F = 0$	I_{CCL}		4.1	6.5	mA
Logic high supply current	$V_{CC} = 5.5 \text{ V}, I_F = 5.0 \text{ mA}$	I_{CCH}		3.4	4.0	mA
	$V_{CC} = 15 \text{ V}, I_F = 5.0 \text{ mA}$	I_{CCH}		3.7	5.0	mA
Logic low short circuit output current (2)	$V_O = V_{CC} = 5.5 \text{ V}, I_F = 0$	I_{OSL}	25			mA
	$V_O = V_{CC} = 15 \text{ V}, I_F = 0$	I_{OSL}	40			mA
Logic high short circuit output current (2)	$V_{CC} = 5.5 \text{ V}, V_O = 0 \text{ V}, I_F = 5.0$	I_{OSL}			- 10	mA
	$V_{CC} = 15 \text{ V}, V_O = 0 \text{ V}, I_F = 5.0$	I_{OSL}			- 25	mA
Thermal resistance		R_{thJA}		300		K/W
COUPLER						
Capacitance (input to output)	$f = 1 \text{ MHz}, \text{ pins } 1 \text{ to } 4 \text{ and } 5 \text{ to } 8 \text{ shorted together}$	C_{IO}		0.6		pF
Isolation resistance	$V_{IO} = 500 \text{ V}, T_{amb} = 25 \text{ }^\circ\text{C}$	R_{IO}	10^{12}			Ω
	$V_{IO} = 500 \text{ V}, T_{amb} = 100 \text{ }^\circ\text{C}$	R_{IO}	10^{11}			Ω

Notes

(1) - $40 \text{ }^\circ\text{C} \leq T_{amb} \leq 85 \text{ }^\circ\text{C}$; $4.5 \text{ V} \leq V_{CC} \leq 15 \text{ V}$; $1.6 \text{ mA} \leq I_{Fon} \leq 5.0 \text{ mA}$; $2.0 \leq V_{EH} \leq 15 \text{ V}$; $0 \leq V_{EL} \leq 0.8 \text{ V}$; $0 \text{ mA} \leq I_{Foff} \leq 0.1 \text{ mA}$.

Typical values: $T_{amb} = 25 \text{ }^\circ\text{C}$; $V_{CC} = 5.0 \text{ V}$; $I_{Fon} = 3.0 \text{ mA}$ unless otherwise specified. Minimum and maximum values are testing requirements.

Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

(2) Output short circuit time $\leq 10 \text{ ms}$.



SWITCHING CHARACTERISTICS (1)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low output level, SFH6700/01/02/11/12/19 (2)	Without peaking capacitor		t _{PHL}		120		ns
			t _{PHL}		115	300	ns
	With peaking capacitor		t _{PLH}		125		ns
			t _{PLH}		90	300	ns
Output enable time to logic high (SFH6700/19) (2)			t _{PZH}		20		ns
Output enable time to logic low (SFH6700/19) (2)			t _{PZL}		25		ns
Output disable time from logic low (SFH6700/19) (2)			t _{PLZ}		50		ns
Output rise time (2)	10 % to 90 %		t _r		40		ns
Output fall time (2)	90 % to 10 %		t _f		10		ns
Propagation delay time to logic low output level (3)	Without peaking capacitor	SFH6705	t _{PHL}		115		ns
	With peaking capacitor	SFH6705	t _{PHL}		105	300	ns
	Without peaking capacitor	SFH6705	t _{PLH}		125		ns
	With peaking capacitor	SFH6705	t _{PLH}		90	300	ns
Output rise time (3)	10 % to 90 %		t _r		25		ns
	90 % to 10 %		t _r		4		ns

Notes

- (1) 0 °C ≤ T_{amb} ≤ 85 °C; 4.5 V ≤ V_{CC} ≤ 15 V; 1.6 mA ≤ I_{Fon} ≤ 5.0 mA; 2.0 ≤ V_{EH} ≤ 15 V (SFH6700/19); 0 ≤ V_{EL} ≤ 0.8 V (SFH6700/19); 0 mA ≤ I_{Foff} ≤ 0.1 mA
- (2) Typical values: T_{amb} = 25 °C; V_{CC} = 5.0 V; I_{Fon} = 3.0 mA unless otherwise specified (4)
- (3) Typical values: T_{amb} = 25 °C, V_{CC} = 5.0 V; I_{Fon} = 3.0 mA; R_L = 390 Ω unless otherwise specified (4)
- (4) A 0.1 μF bypass capacitor connected between pins 5 and 8 must be used

COMMON MODE TRANSIENT IMMUNITY (1)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic high common mode transient immunity	V _{CM} = 50 V, I _F = 1.6 mA	SFH6700	CM _H (2)	1000			V/μs
		SFH6701	CM _H (2)	1000			V/μs
		SFH6702	CM _H (2)	1000			V/μs
		SFH6705	CM _H (2)	1000			V/μs
	V _{CM} = 400 V, I _F = 1.6 mA	SFH6711	CM _H (2)	2500			V/μs
		SFH6712	CM _H (2)	2500			V/μs
Logic Low common mode transient immunity	V _{CM} = 50 V, I _F = 0 mA	SFH6700	CM _L (3)	1000			V/μs
		SFH6701	CM _L (3)	1000			V/μs
	V _{CM} = 50 V, I _F = 0 mA	SFH6702	CM _L (3)	1000			V/μs
		SFH6705	CM _L (3)	1000			V/μs
	V _{CM} = 400 V, I _F = 0 mA	SFH6711	CM _L (3)	2500			V/μs
		SFH6712	CM _L (3)	2500			V/μs
		SFH6719	CM _L (3)	2500			V/μs

Notes

- (1) T_{amb} = 25 °C, V_{CC} = 5.0 V
- (2) CM_H is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O > 2.0 V)
- (3) CM_L is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O < 0.8 V)

TYPICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

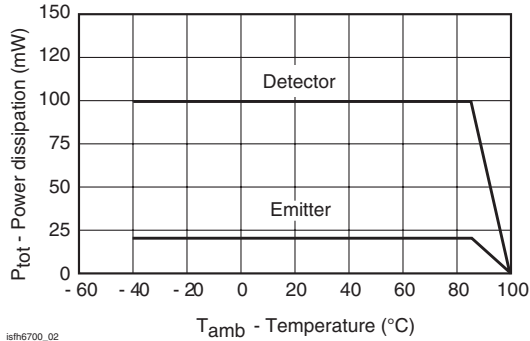


Fig. 2 - Permissible Total Power Dissipation vs. Temperature

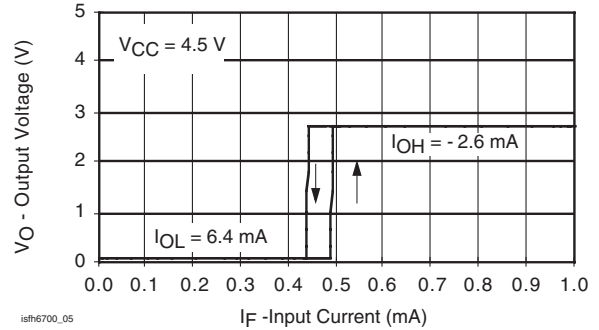


Fig. 5 - Typical Output Voltage vs. Forward Input Current (except SFH6705)

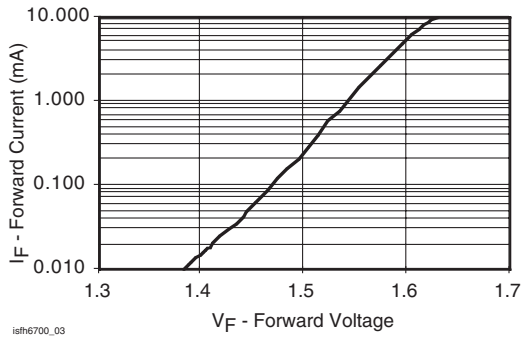


Fig. 3 - Typical Input Diode Forward Current vs. Forward Voltage

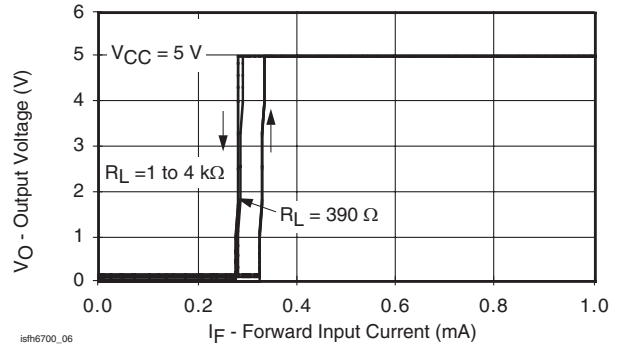


Fig. 6 - Typical Output Forward Voltage vs. Forward Input Current (only SFH6705)

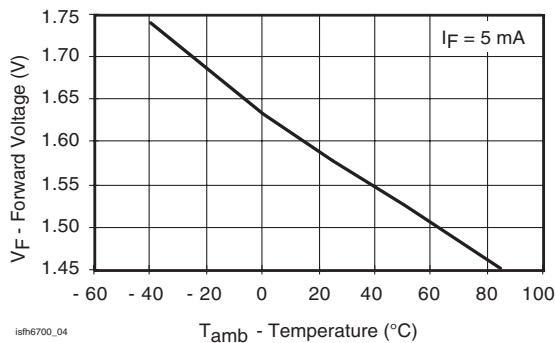


Fig. 4 - Typical Forward Input Voltage vs. Temperature

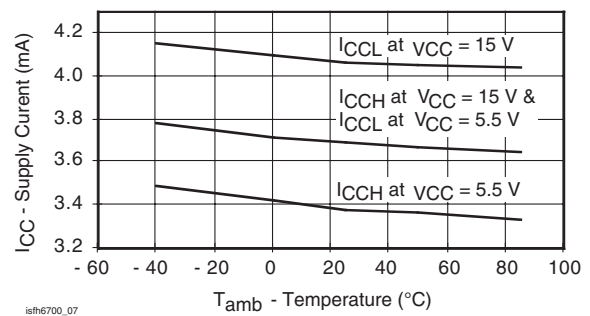


Fig. 7 - Typical Supply Current vs. Temperature

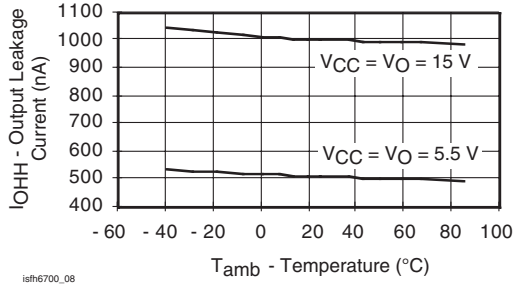


Fig. 8 - Typical Output Leakage Current vs. Temperature

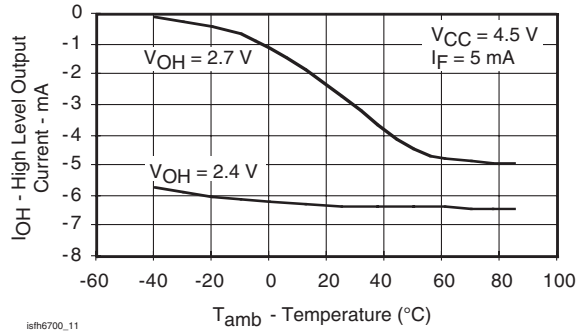


Fig. 11 - Typical High Level Output Current vs. Temperature (except SFH6705)

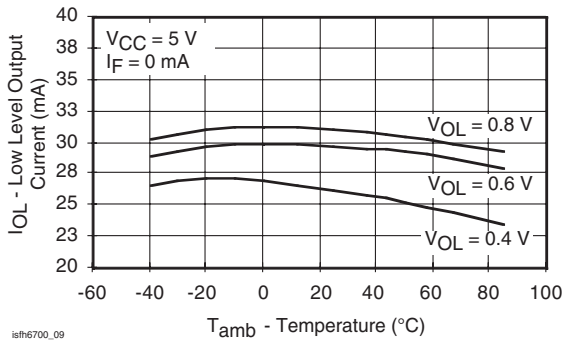


Fig. 9 - Typical Low Level Output Current vs. Temperature

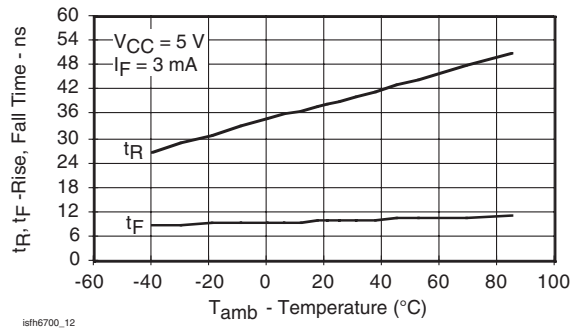


Fig. 12 - Typical Rise, Fall Time vs. Temperature (except SFH6705)

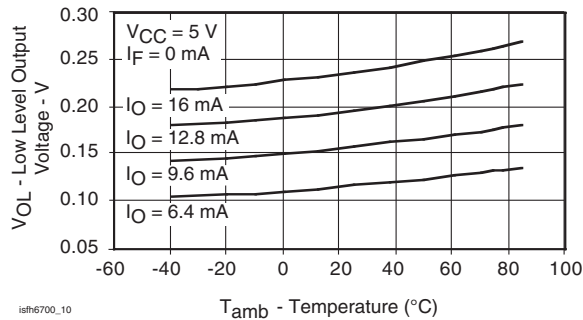


Fig. 10 - Typical Low Level Output Voltage vs. Temperature

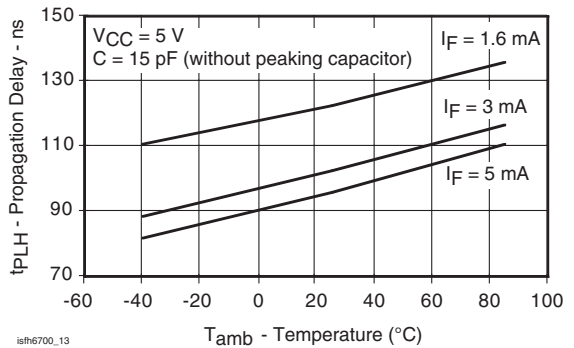


Fig. 13 - Typical Propagation Delay to Logic High vs. Temperature (except SFH6705)

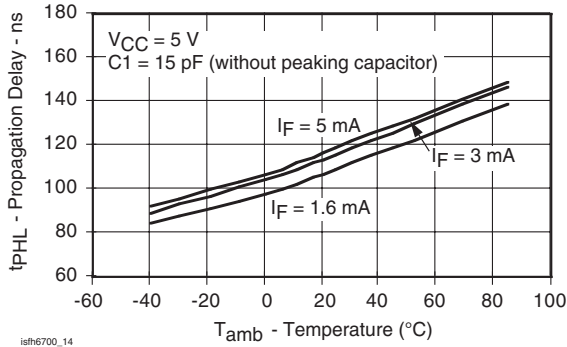


Fig. 14 - Typical Propagation Delay to Logic Low vs. Temperature (except SFH6705)

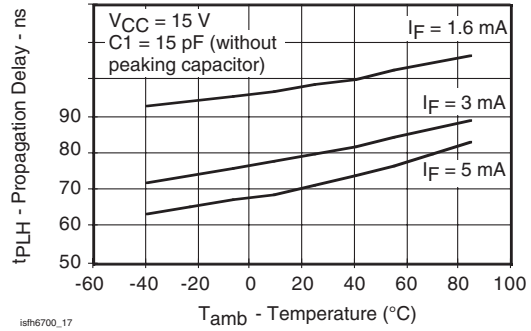


Fig. 17 - Typical Propagation Delays to Logic High vs. Temperature

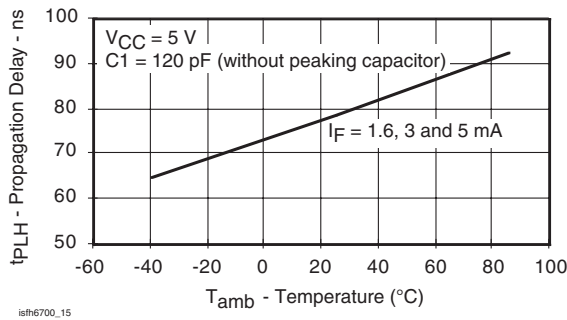


Fig. 15 - Typical Propagation Delays to Logic High vs. Temperature (except SFH6705)

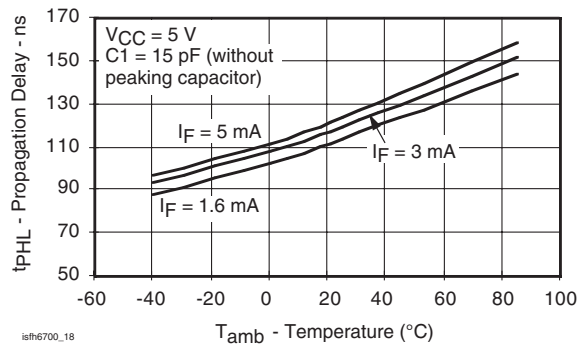


Fig. 18 - Typical Propagation Delays to Logic Low vs. Temperature

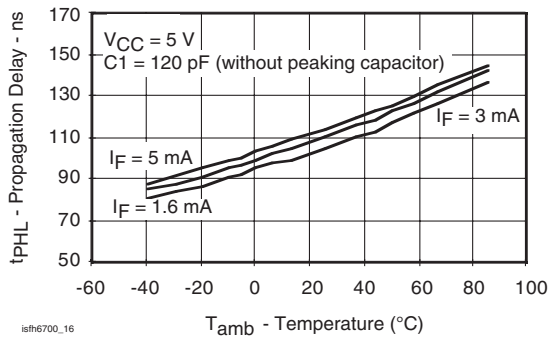


Fig. 16 - Typical Propagation Delay to Logic Low vs. Temperature

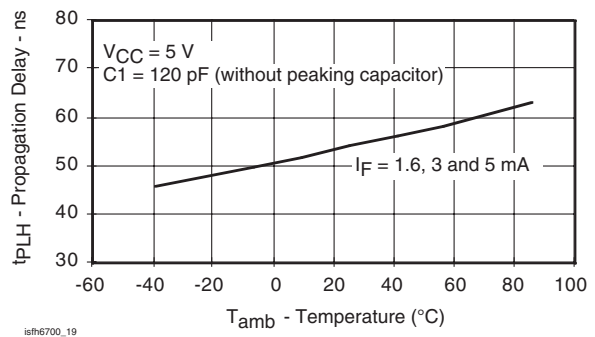


Fig. 19 - Typical Propagation Delays to Logic High vs. Temperature

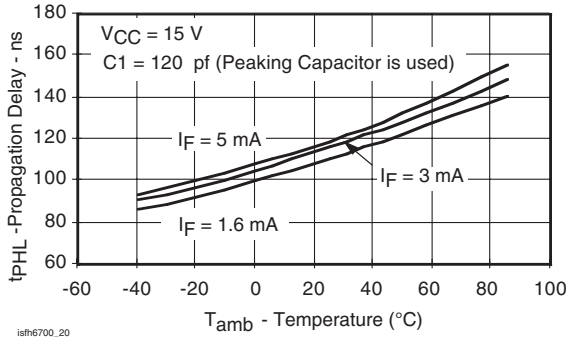


Fig. 20 - Typical Propagation Delays to Logic Low vs. Temperature (except SFH6705)

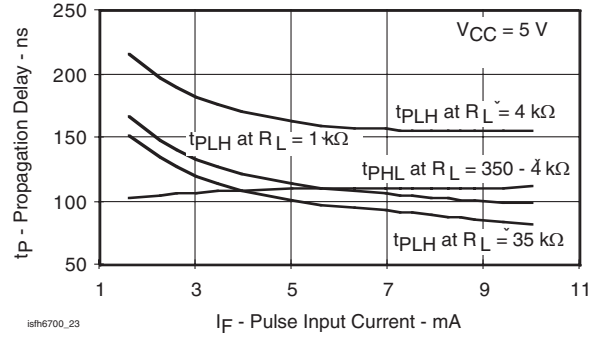


Fig. 23 - Typical Propagation Delays vs. Pulse Input Current (only SFH6705)

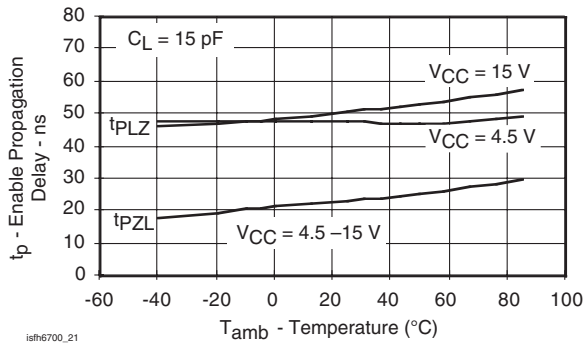


Fig. 21 - Typical Logic Low Enable Propagation Delays vs. Temperature (only SFH6700/11)

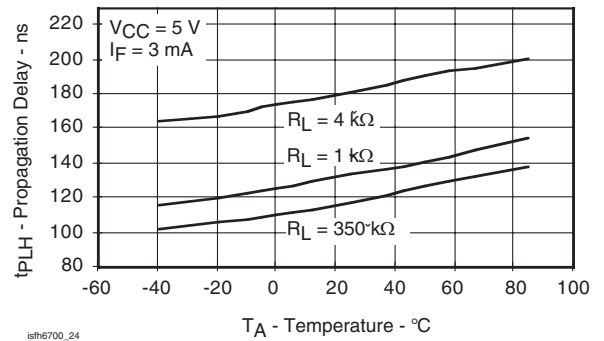


Fig. 24 - Typical Propagation Delays to High Level vs. Temperature (only SFH6705)

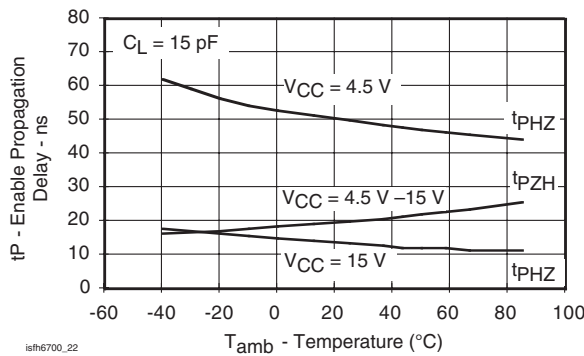


Fig. 22 - Typical Logic High Enable Propagation Delays vs. Temperature (only SFH6700/11)

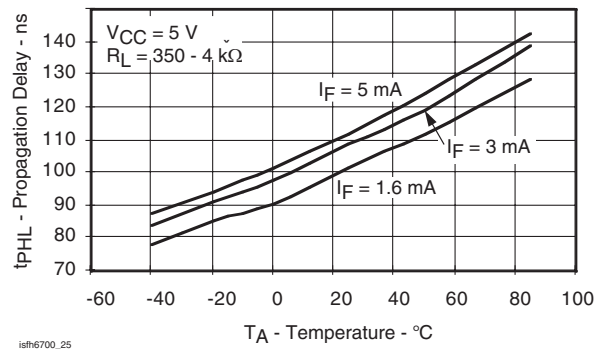


Fig. 25 - Typical Propagation Delays to Low Level vs. Temperature (only SFH6705)

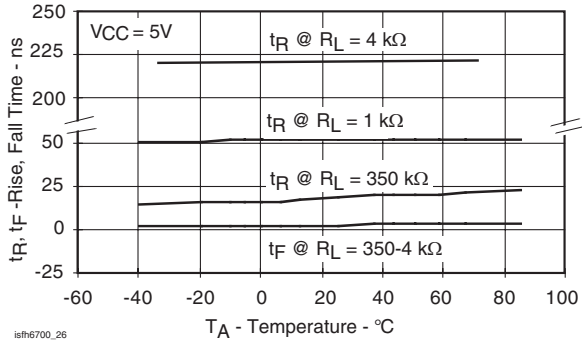


Fig. 26 - Typical Rise, Fall Time vs. Temperature (only SFH6705)

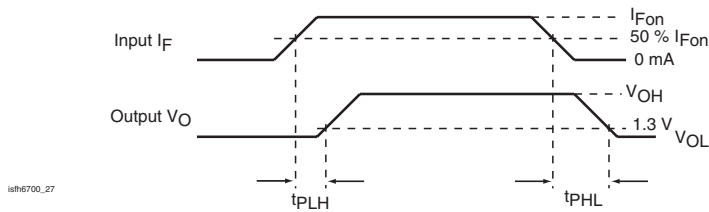
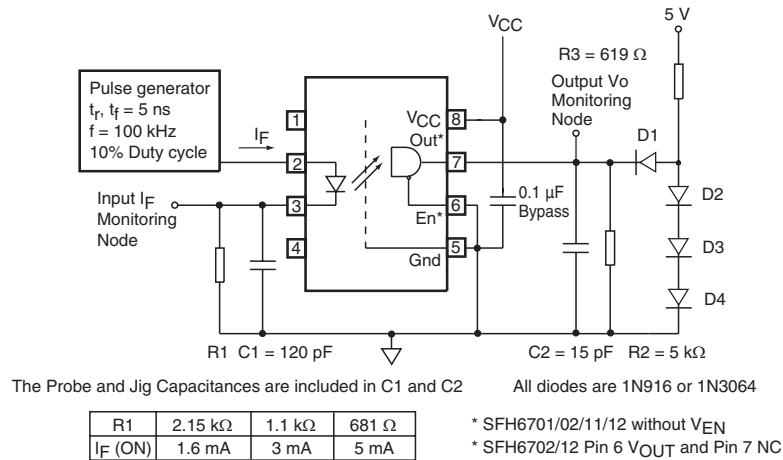
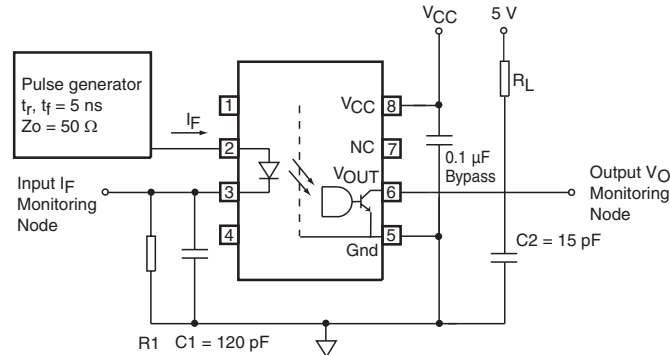
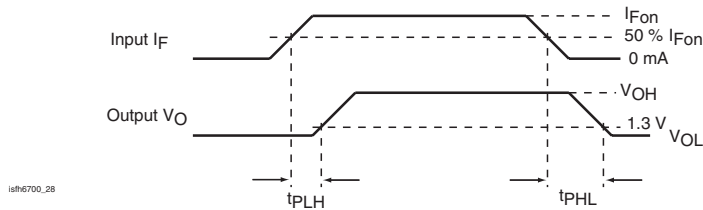


Fig. 27 Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f



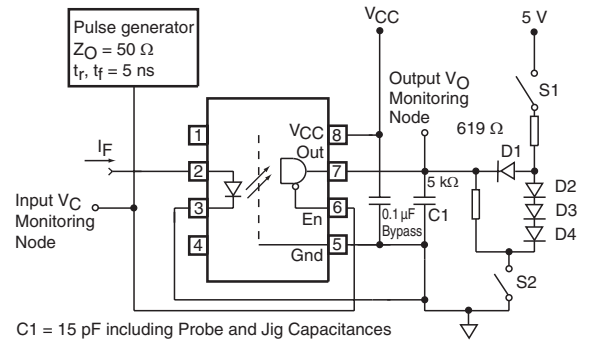
The Probe and Jig Capacitances are included in C1 and C2

R1	2.15 k Ω	1.1 k Ω	681 Ω
I _F (ON)	1.6 mA	3 mA	5 mA



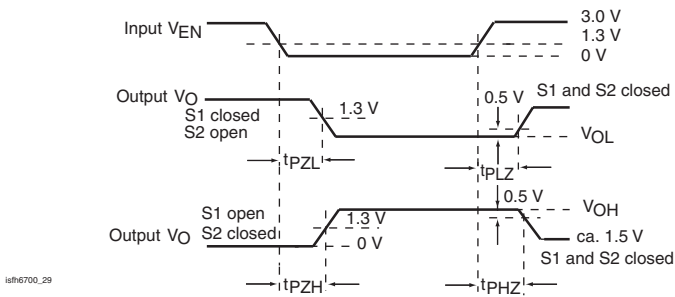
isf6700_28

Fig. 28 Test Circuit for t_{PLH} , t_{PHL} , t_r and - SFH6705



C1 = 15 pF including Probe and Jig Capacitances

All diodes are 1N916 or 1N3064



isf6700_29

Fig. 29 Test Circuit for t_{PHZ} , t_{PZH} , t_{PLZ} and t_{PZL} - SFH6700/19

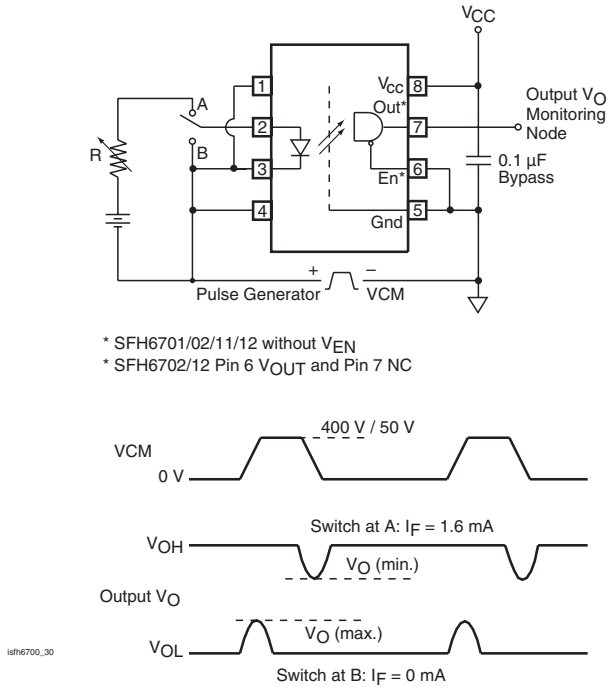


Fig. 30 Test Circuit for Common Mode Transient Immunity and Typical Waveforms - SFH6700/01/02/11/12/19

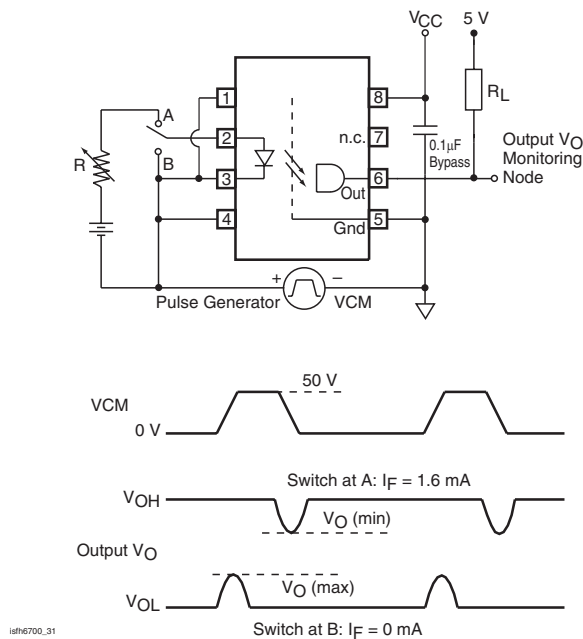
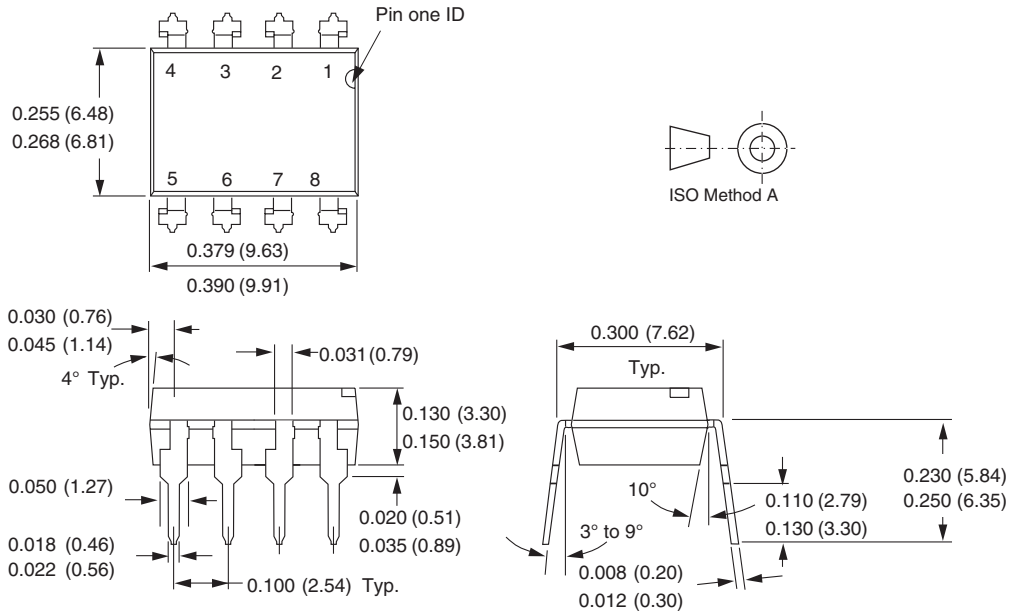


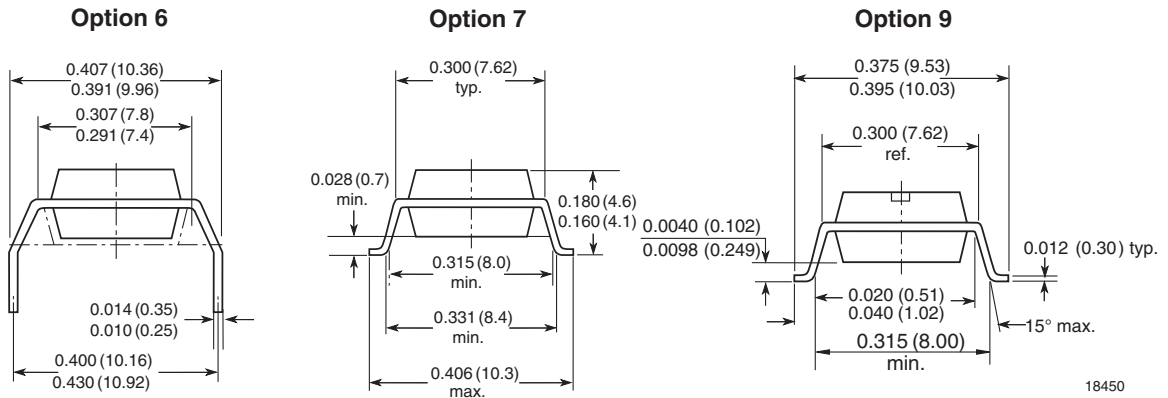
Fig. 31 Test Circuit for Common Mode Transient Immunity and Typical Waveforms - SFH6705



PACKAGE DIMENSIONS in inches (millimeters)



i178006



18450

OZONE DEPLETING SUBSTANCES POLICY STATEMENT

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively.
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design
and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany



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