

## Phase Control Thyristors (Hockey PUK Version), 650 A



TO-200AB (E-PUK)

**FEATURES**

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (E-PUK)
- Lead (Pb)-free
- Designed and qualified for industrial level


**RoHS  
COMPLIANT**
**TYPICAL APPLICATIONS**

- DC motor controls
- Controlled DC power supplies
- AC controllers

**PRODUCT SUMMARY**

$I_{T(AV)}$	650 A
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**MAJOR RATINGS AND CHARACTERISTICS**

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		650	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		1290	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	8000	A
	60 Hz	8380	
$I^2t$	50 Hz	320	kA <sup>2</sup> s
	60 Hz	292	
$V_{DRM}/V_{RRM}$		400 to 2000	V
$t_q$	Typical	100	μs
$T_J$		- 40 to 125	°C

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST300C..C	04	400	500	50
	08	800	900	
	12	1200	1300	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		650 (320)	A
				55 (75)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		1290	
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	8000	A
		t = 8.3 ms		100 % $V_{RRM}$ reapplied	
		t = 10 ms	Sinusoidal half wave, initial $T_J = T_J$ maximum		
		t = 8.3 ms		7040	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied	320	kA <sup>2</sup> s
		t = 8.3 ms		100 % $V_{RRM}$ reapplied	
		t = 10 ms	226		
		t = 8.3 ms	207		
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		3200	kA <sup>2</sup> /s
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.97	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.98	
Low level value of on-state slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.74	mΩ
High level value of on-state slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.73	
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 1635$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse		2.18	V
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load		600	mA
Typical latching current	$I_L$			1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	$di/dt$	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage $\leq 80\%$ $V_{DRM}$		1000	A/μs
Typical delay time	$t_d$	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67\%$ $V_{DRM}$ , $T_J = 25$ °C		1.0	μs
Typical turn-off time	$t_q$	$I_{TM} = 300$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs		100	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum linear to 80 % rated $V_{DRM}$		500	V/μs
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied		50	mA



<b>TRIGGERING</b>					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			TYP.	MAX.	
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0		
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20		V
Maximum peak negative gate voltage	$-V_{GM}$		5.0		
DC gate current required to trigger	$I_{GT}$	$T_J = -40$ °C	200	-	mA
		$T_J = 25$ °C	100	200	
		$T_J = 125$ °C	50	-	
DC gate voltage required to trigger	$V_{GT}$	$T_J = -40$ °C	2.5	-	V
		$T_J = 25$ °C	1.8	3.0	
		$T_J = 125$ °C	1.1	-	
DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum	10.0		mA
DC gate voltage not to trigger	$V_{GD}$		0.25		V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	$T_J$		- 40 to 125	°C
Maximum storage temperature range	$T_{Stg}$		- 40 to 150	
Maximum thermal resistance, junction to heatsink	$R_{thJ-hs}$	DC operation single side cooled	0.09	K/W
		DC operation double side cooled	0.04	
Maximum thermal resistance, case to heatsink	$R_{thC-hs}$	DC operation single side cooled	0.02	
		DC operation double side cooled	0.01	
Mounting force, $\pm 10$ %			9800 (1000)	N (kg)
Approximate weight			83	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (E-PUK)	

<b><math>\Delta R_{thJ-hs}</math> CONDUCTION</b>						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.010	0.011	0.007	0.007	$T_J = T_J$ maximum	K/W
120°	0.012	0.012	0.012	0.013		
90°	0.015	0.015	0.016	0.017		
60°	0.022	0.022	0.023	0.023		
30°	0.036	0.036	0.036	0.037		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJ-hs}$  when devices operate at different conduction angles than DC

# ST300CPbF Series



Vishay High Power Products Phase Control Thyristors  
(Hockey PUK Version), 650 A

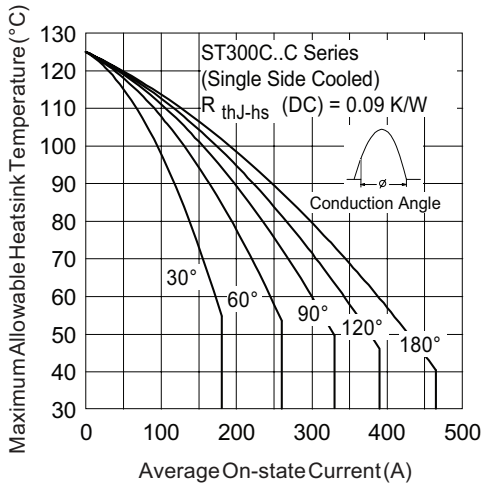


Fig. 1 - Current Ratings Characteristics

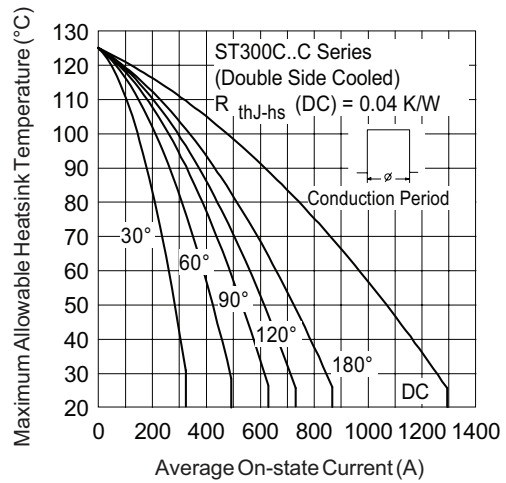


Fig. 4 - Current Ratings Characteristics

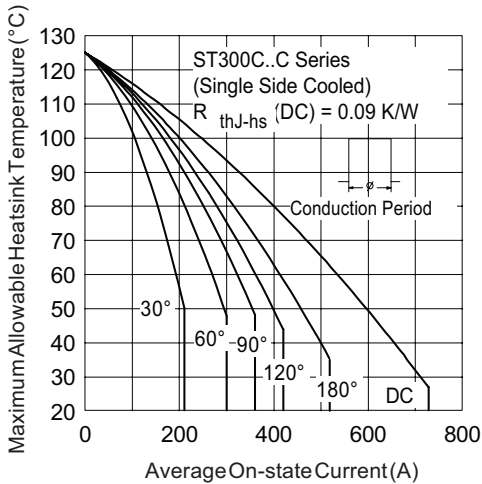


Fig. 2 - Current Ratings Characteristics

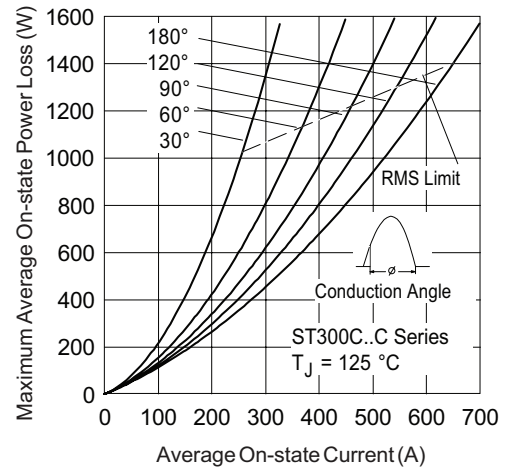


Fig. 5 - On-State Power Loss Characteristics

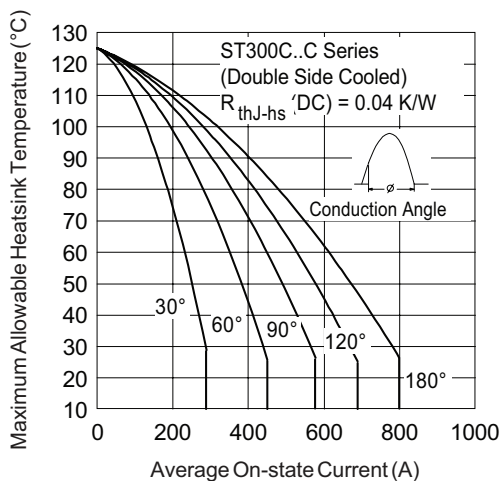


Fig. 3 - Current Ratings Characteristics

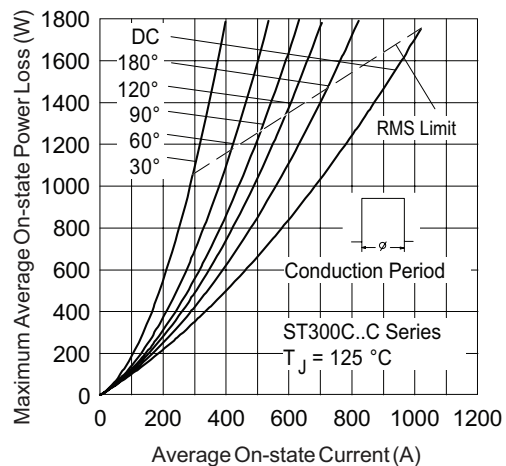


Fig. 6 - On-State Power Loss Characteristics

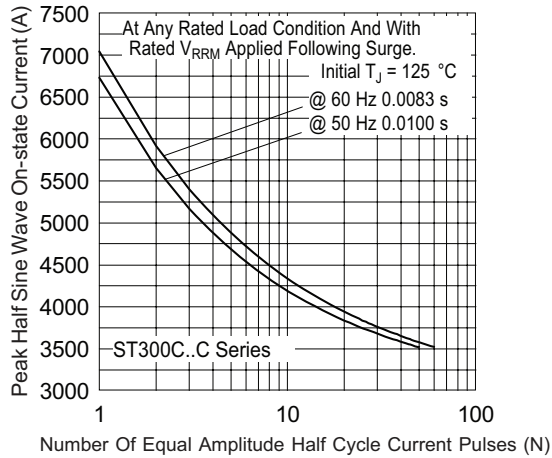


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

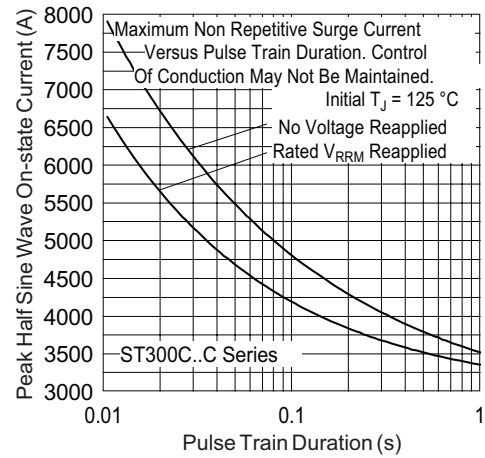


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

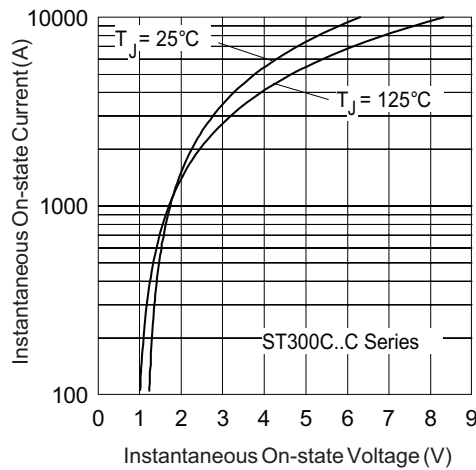


Fig. 9 - On-State Voltage Drop Characteristics

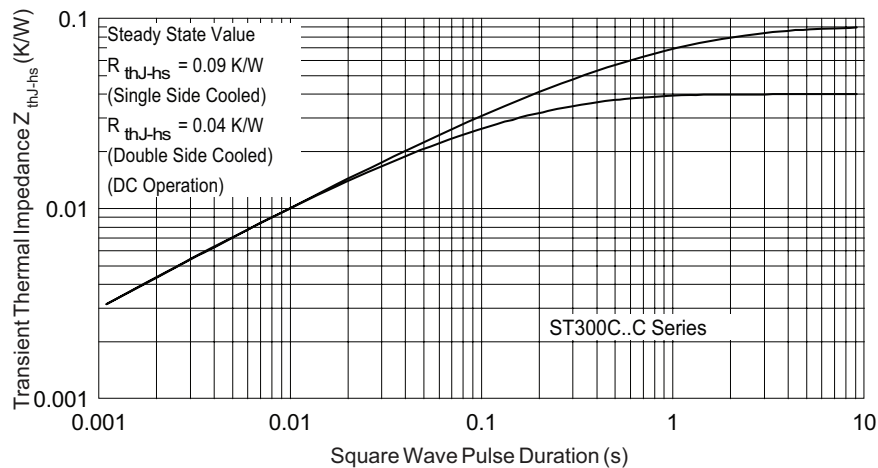


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

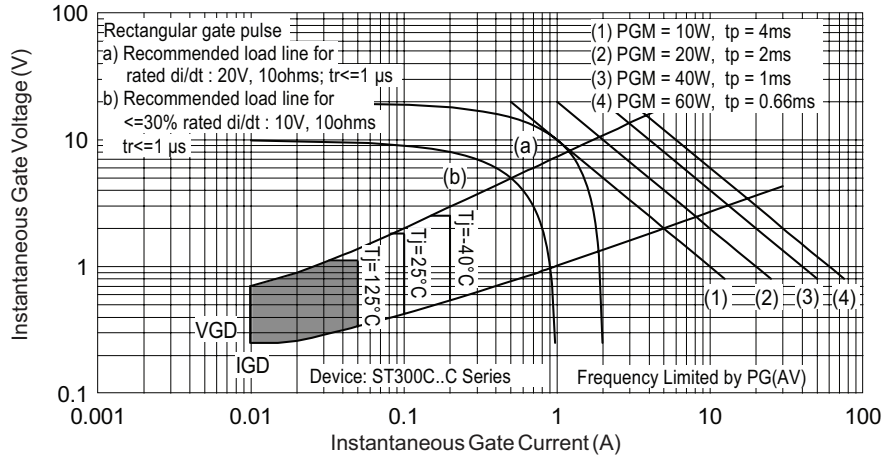


Fig. 11 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	<b>ST</b>	<b>30</b>	<b>0</b>	<b>C</b>	<b>20</b>	<b>C</b>	<b>1</b>	<b>-</b>	<b>PbF</b>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)

- 1** - Thyristor
- 2** - Essential part number
- 3** - 0 = Converter grade
- 4** - C = Ceramic PUK
- 5** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- 6** - C = PUK case TO-200AB (E-PUK)
- 7** - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)  
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)  
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)  
3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 8** - Critical dV/dt: • None = 500 V/ $\mu$ s (standard value)  
• L = 1000 V/ $\mu$ s (special selection)
- 9** - Lead (Pb)-free

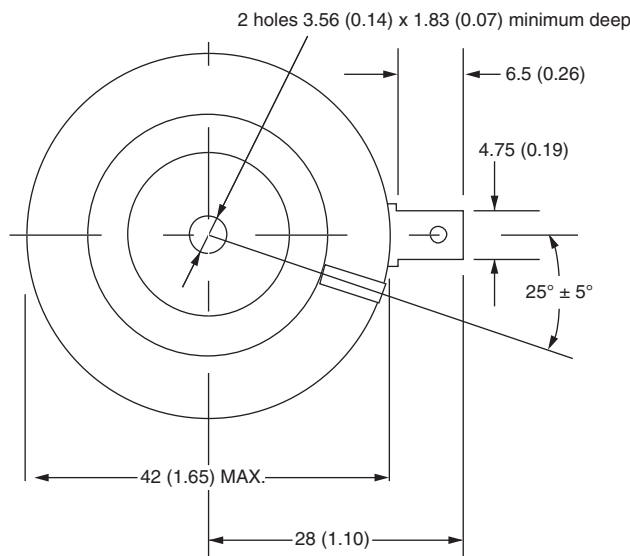
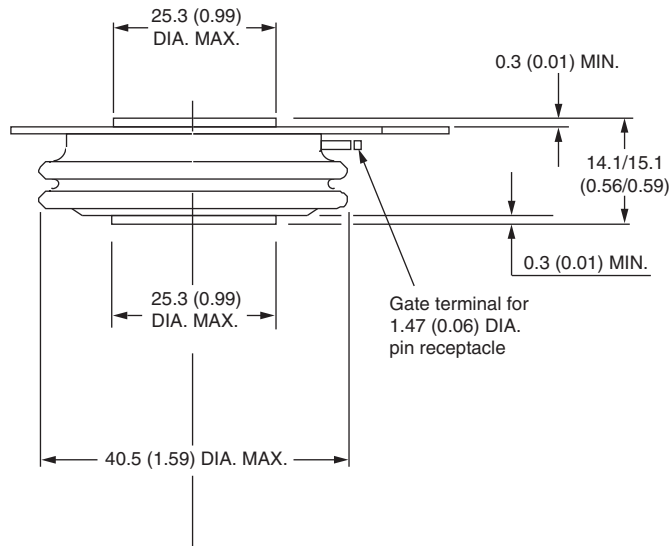
### LINKS TO RELATED DOCUMENTS

Dimensions	<a href="http://www.vishay.com/doc?95075">http://www.vishay.com/doc?95075</a>
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## TO-200AB (E-PUK)

**DIMENSIONS** in millimeters (inches)

Anode to gate  
 Creepage distance: 11.18 (0.44) minimum  
 Strike distance: 7.62 (0.30) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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