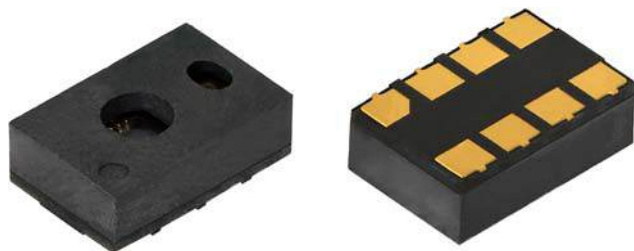


# Proximity Sensor With VCSEL in Single Package, I<sup>2</sup>C Interface



## DESCRIPTION

VCNL36687S integrates a proximity and a high power VCSEL (vertical-cavity surface-emitting laser) into one small package. It incorporates photodiodes, amplifiers, and analog to digital converting circuits into a single chip by CMOS process. PS programmable interrupt features of individual high and low thresholds offers the best utilization of resource and power saving on the microcontroller. With just 20 mA pulse current, the VCNL36687S can detect the Kodak Gray Card in a distance of 20 cm, where other sensors need 200 mA.

The 12 bits proximity sensing function uses an intelligent cancellation scheme, so that cross talk is eliminated effectively. To accelerate the PS response time, smart persistence prevents the misjudgment of proximity sensing but also allows for a fast response time. Active force mode, one time trigger by one instruction, is a feature offering more power saving.

PS functions are easily operated via the simple command format of I<sup>2</sup>C (SMBus compatible) interface protocol. Operating voltage ranges from 1.65 V to 1.95 V. VCNL36687S is packaged in a lead (Pb)-free 8 pin molding package, which offers the best market-proven reliability quality.

## APPLICATIONS

- Proximity sensor especially for battery operated devices
- Mobile devices (e.g. smart phones, tablets) for touch screen locking, power saving etc.
- VR / AR headsets to detect if the headset has been put on or taken off

## FEATURES

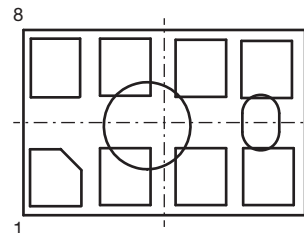
- Package type: surface-mount
- Dimensions (L x W x H in mm): 3.05 x 2 x 1.0
- Integrated modules: proximity sensor (PS), and VCSEL in single package
- Interrupt function
- Smallest light hole opening design
- Supply voltage range V<sub>DD</sub>: 1.65 V to 1.95 V
- Communication via I<sup>2</sup>C interface
- I<sup>2</sup>C bus H-level range: 1.65 V to 3.6 V
- Floor life: 168 h, MSL 3, according to J-STD-020
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## PROXIMITY FUNCTION

- Immunity to red glow (940 nm VCSEL)
- Programmable I<sub>VCSEL</sub> sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce PS response time
- 12 bits PS output data
- Programmable interrupt function for PS with upper and lower thresholds
- Adjustable persistence to prevent false triggers for PS

## PIN DEFINITION



|   |                 |   |         |
|---|-----------------|---|---------|
| 1 | GND             | 5 | VCSEL_C |
| 2 | V <sub>PP</sub> | 6 | INT     |
| 3 | V <sub>DD</sub> | 7 | SDA     |
| 4 | VCSEL_A         | 8 | SCL     |

## PRODUCT SUMMARY

| PART NUMBER | OPERATING RANGE (mm) | OPERATING VOLTAGE RANGE (V) | I <sup>2</sup> C BUS VOLTAGE RANGE (V) | VCSEL DRIVING CURRENT <sup>(1)</sup> (mA) | OUTPUT CODE              | ADC RESOLUTION PROXIMITY / AMBIENT LIGHT |
|-------------|----------------------|-----------------------------|----------------------------------------|-------------------------------------------|--------------------------|------------------------------------------|
| VCNL36687S  | 200                  | 1.65 to 1.95                | 1.65 to 3.6                            | 20                                        | 12 bit, I <sup>2</sup> C | 12 bit / -                               |

### Note

<sup>(1)</sup> Base on VCSEL period = 8 ms, 16 ms, 32 ms, and 64 ms

**ORDERING INFORMATION**

| ORDERING CODE | PACKAGING     | VOLUME <sup>(1)</sup>        | REMARKS                   |
|---------------|---------------|------------------------------|---------------------------|
| VCNL36687S    | Tape and reel | MOQ: 2500 pcs, 2500 pcs/reel | 3.05 mm x 2.0 mm x 1.0 mm |

**Note**

<sup>(1)</sup> MOQ: minimum order quantity

**ABSOLUTE MAXIMUM RATINGS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                   | TEST CONDITION | SYMBOL    | MIN. | MAX. | UNIT               |
|-----------------------------|----------------|-----------|------|------|--------------------|
| Supply voltage              |                | $V_{DD}$  | 1.65 | 1.95 | V                  |
| Operation temperature range |                | $T_{amb}$ | -40  | +85  | $^{\circ}\text{C}$ |
| Storage temperature range   |                | $T_{stg}$ | -40  | +85  | $^{\circ}\text{C}$ |

**BASIC CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                                 | TEST CONDITION                                                                              | SYMBOL              | MIN. | TYP. | MAX. | UNIT               |
|-------------------------------------------|---------------------------------------------------------------------------------------------|---------------------|------|------|------|--------------------|
| Supply voltage                            |                                                                                             | $V_{DD}$            | 1.65 | 1.8  | 1.95 | V                  |
|                                           |                                                                                             | $V_{PP}$            | 1.65 | 1.8  | 1.95 | V                  |
| Supply current                            | Excluding VCSEL driving                                                                     | $I_{DD}$            | -    | 160  | -    | $\mu\text{A}$      |
|                                           | Light condition = dark;<br>$V_{DD} = 1.8\text{ V}$ , $T_{amb} = 25\text{ }^{\circ}\text{C}$ | $I_{DD}(\text{SD})$ | -    | 0.5  | -    | $\mu\text{A}$      |
| I <sup>2</sup> C supply voltage           |                                                                                             | $V_{PULL\ UP}$      | 1.65 | 1.8  | 3.6  | V                  |
| I <sup>2</sup> C signal input, logic high | $V_{DD} = 1.8\text{ V}$                                                                     | $V_{IH}$            | 1.26 | -    | -    | V                  |
| I <sup>2</sup> C signal input, logic low  | $V_{DD} = 1.8\text{ V}$                                                                     | $V_{IL}$            | -    | -    | 0.73 | V                  |
| Full PS counts                            | 12-bit resolution                                                                           |                     | -    | -    | 4095 | steps              |
| Operating temperature                     |                                                                                             | $T_{amb}$           | -40  | -    | +85  | $^{\circ}\text{C}$ |
| VCSEL driving voltage                     | <sup>(2)</sup>                                                                              |                     | 2.68 | -    | 4.8  | V                  |
| VCSEL driving current                     | <sup>(1)</sup>                                                                              |                     | 7    | -    | 20   | mA                 |
| PS view angle                             | <sup>(3)</sup>                                                                              |                     | -    | 60   | -    | $^{\circ}$         |

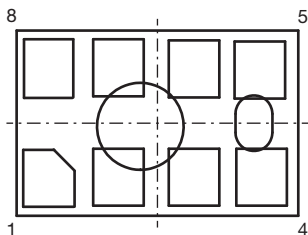
**Notes**

<sup>(1)</sup> Base on VCSEL period = 8 ms, 16 ms, 32 ms, and 64 ms

<sup>(2)</sup> Base on VCSEL current setting, VCSEL min. voltage need adjust, example as below

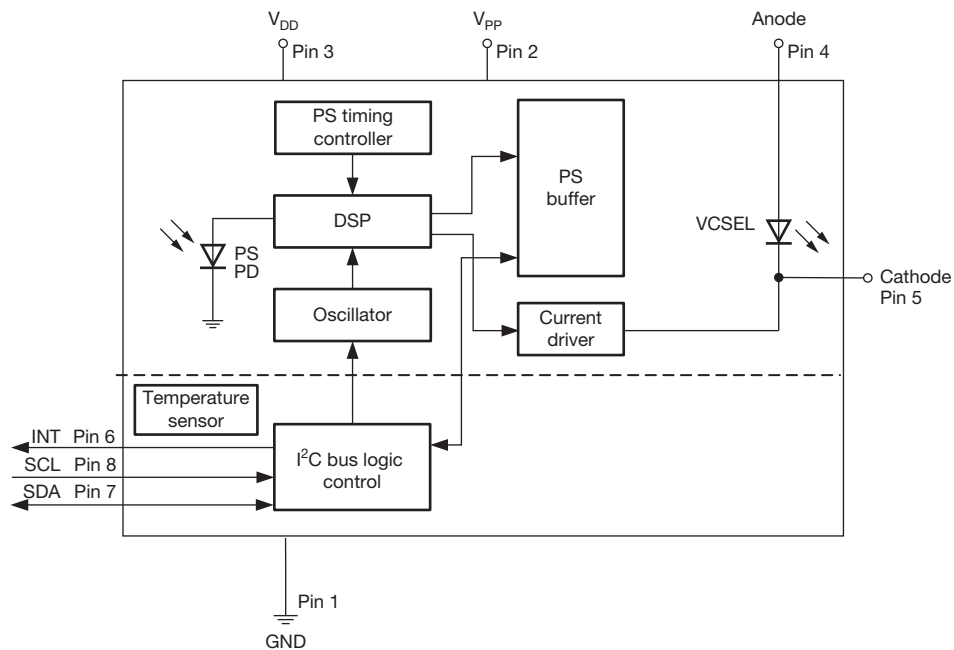
|                                                                |        |        |        |        |        |
|----------------------------------------------------------------|--------|--------|--------|--------|--------|
| ILD                                                            | 7 mA   | 11 mA  | 14 mA  | 17 mA  | 20 mA  |
| VCSEL current setting, $V_F$                                   | 2.08 V | 2.30 V | 2.43 V | 2.55 V | 2.69 V |
| VCSEL min. voltage, $V_{LD}$ ( $V_{LD} = V_F + 0.6\text{ V}$ ) | 2.68 V | 2.90 V | 3.03 V | 3.15 V | 3.29 V |

<sup>(3)</sup> Shows total view angle of X-axis (X-axis:  $+10^{\circ}$  to  $-50^{\circ}$ ; Y-axis:  $\pm 45^{\circ}$ )

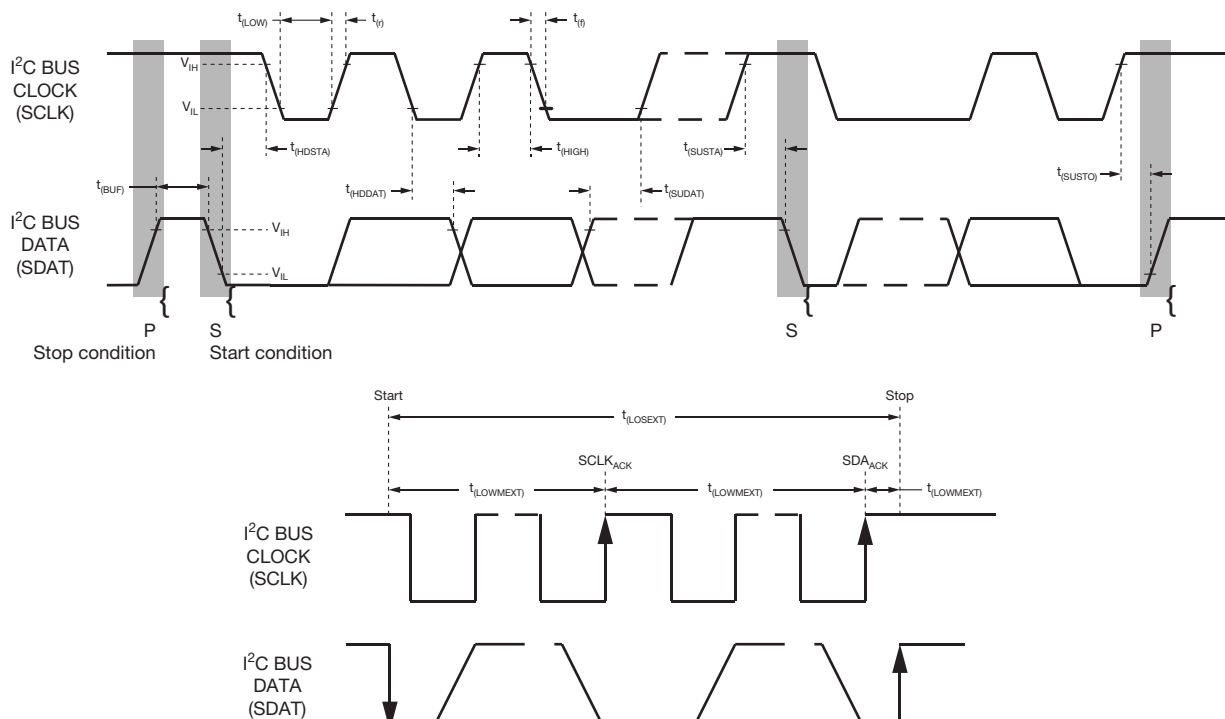




**BLOCK DIAGRAM**



| <b>I<sup>2</sup>C BUS TIMING CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified) |                |               |      |           |      |               |
|-------------------------------------------------------------------------------------------------------------------------|----------------|---------------|------|-----------|------|---------------|
| PARAMETER                                                                                                               | SYMBOL         | STANDARD MODE |      | FAST MODE |      | UNIT          |
|                                                                                                                         |                | MIN.          | MAX. | MIN.      | MAX. |               |
| Clock frequency                                                                                                         | $f_{(I2CCLK)}$ | 10            | 100  | 10        | 400  | kHz           |
| Bus free time between start and stop condition                                                                          | $t_{(BUF)}$    | 4.7           | -    | 1.3       | -    | $\mu\text{s}$ |
| Hold time after (repeated) start condition;<br>after this period, the first clock is generated                          | $t_{(HDSTA)}$  | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Repeated start condition setup time                                                                                     | $t_{(SUSTA)}$  | 4.7           | -    | 0.6       | -    | $\mu\text{s}$ |
| Stop condition setup time                                                                                               | $t_{(SUSTO)}$  | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Data hold time                                                                                                          | $t_{(HDDAT)}$  | -             | 3450 | -         | 900  | ns            |
| Data setup time                                                                                                         | $t_{(SUDAT)}$  | 250           | -    | 100       | -    | ns            |
| I <sup>2</sup> C clock (SCK) low period                                                                                 | $t_{(LOW)}$    | 4.7           | -    | 1.3       | -    | $\mu\text{s}$ |
| I <sup>2</sup> C clock (SCK) high period                                                                                | $t_{(HIGH)}$   | 4.0           | -    | 0.6       | -    | $\mu\text{s}$ |
| Clock / data fall time                                                                                                  | $t_{(f)}$      | -             | 300  | -         | 300  | ns            |
| Clock / data rise time                                                                                                  | $t_{(r)}$      | -             | 1000 | -         | 300  | ns            |


Fig. 1 - I<sup>2</sup>C Bus Timing Diagram



## PARAMETER TIMING INFORMATION

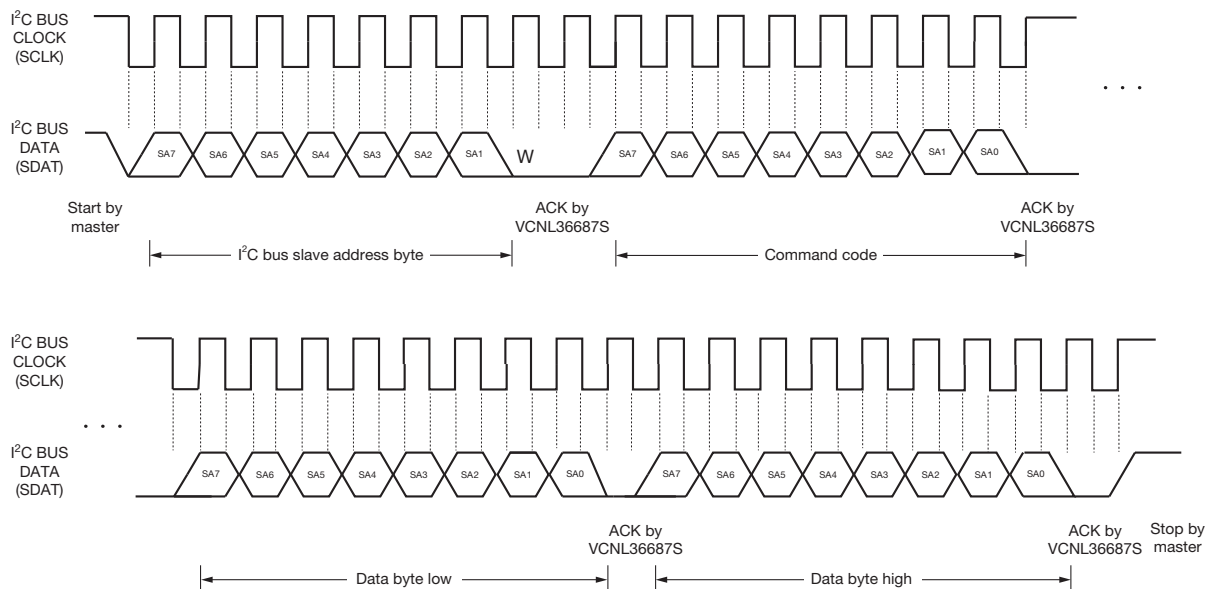


Fig. 2 - I<sup>2</sup>C Bus Timing for Sending Word Command Format

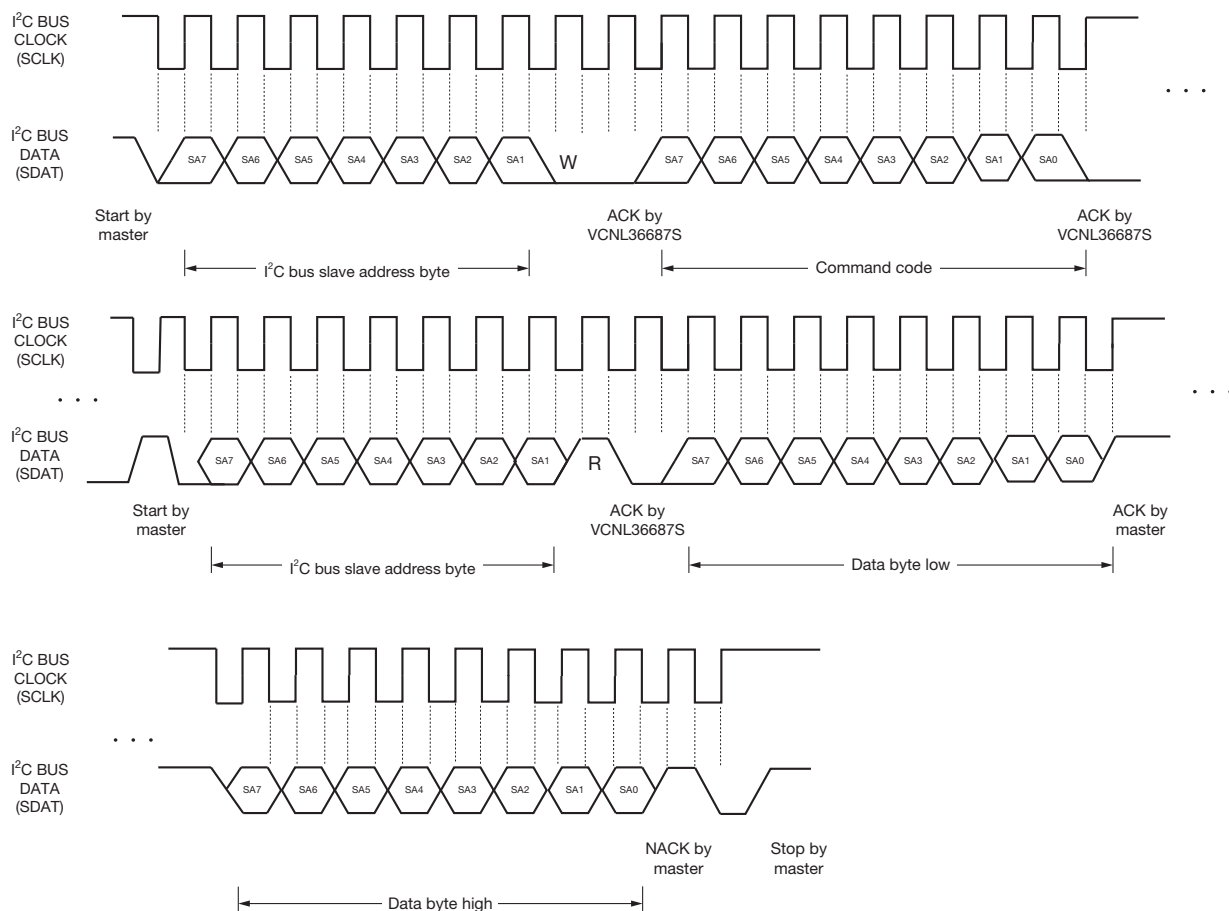


Fig. 3 - I<sup>2</sup>C Bus Timing for Receiving Word Command Format

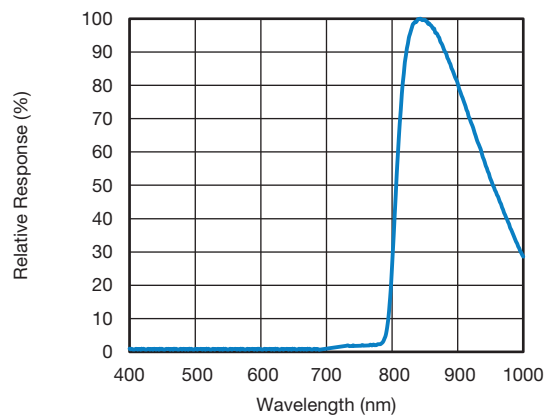
**TYPICAL PERFORMANCE CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 4 - Normalized Spectral Response

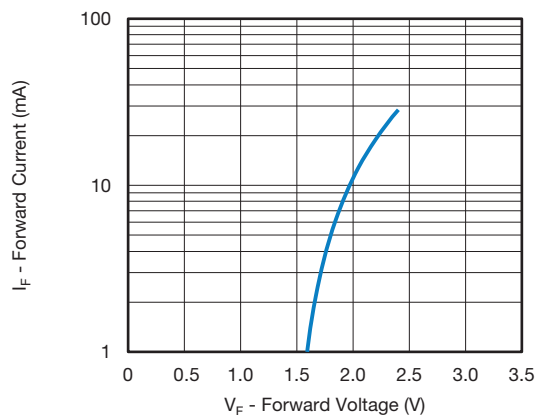


Fig. 5 - Forward Current vs. Forward Voltage

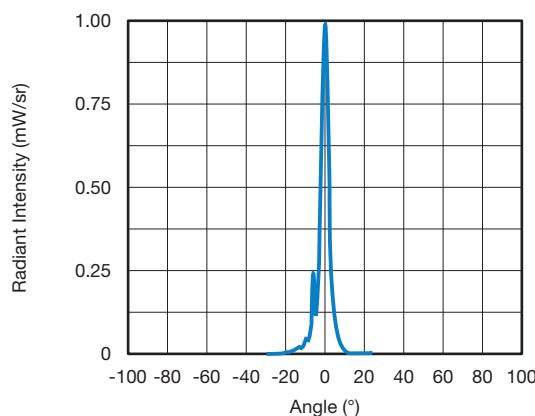
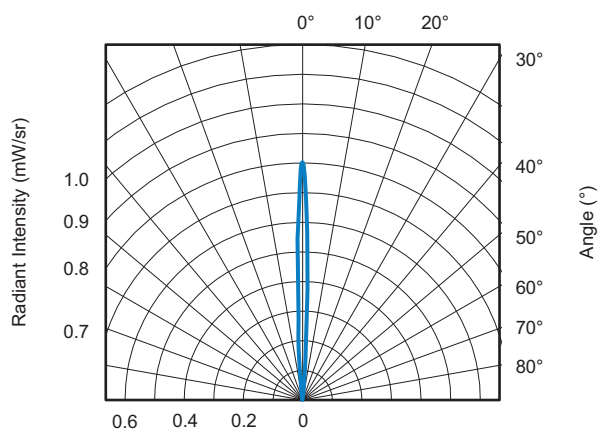


Fig. 6 - VCSEL Profile

VCNL36687S offers a high detection range already with very low pulse current of  $\leq 20\text{ mA}$ .

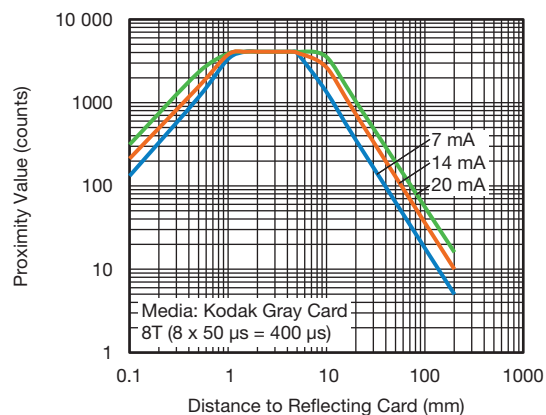


Fig. 7 - Proximity Value vs. Distance; PS\_IT = 8T

For more information please study the application note “Designing the VCNL36687S Into an Application” ([www.vishay.com/doc?84951](http://www.vishay.com/doc?84951))

## APPLICATION INFORMATION

### Pin Connection with the Host

VCNL36687S integrates proximity sensor and VCSEL all together with an I<sup>2</sup>C interface. It is easy for the baseband (CPU) to access PS output data via I<sup>2</sup>C interface without additional software algorithms. The hardware schematic is shown in the following diagram.

Two additional capacitors in the circuit can be used for the following purposes: (1) the 1  $\mu$ F capacitor near the V<sub>DD</sub> pin is used for power supply noise rejection, (2) the 1  $\mu$ F capacitor is used to prevent the VCSEL voltage from instantly dropping when the VCSEL is turned on, and (3) 2.2 k $\Omega$  is suitable for the pull up resistor of I<sup>2</sup>C except for the 10 k $\Omega$  applied on the INT pin.

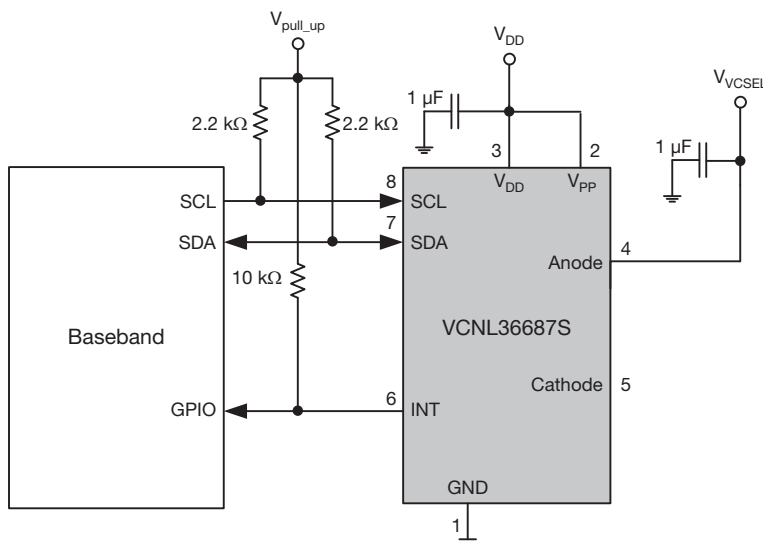
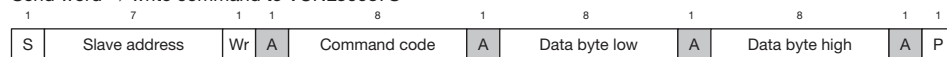


Fig. 8 - Hardware Pin Connection Diagram

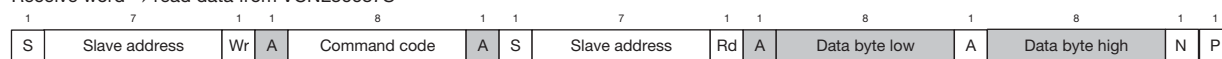
### Digital Interface

VCNL36687S applies single slave address 0x60 (HEX) of 7-bit addressing following I<sup>2</sup>C protocol. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VCNL36687S. As Fig. 9 shows, VCNL36687S's I<sup>2</sup>C command format is simple for read and write operations between VCNL36687S and the host. The white sections indicate host activity and the gray sections indicate VCNL36687S's acknowledgement of the host access activity. Write word and read word protocol is suitable for accessing registers particularly for 12-bit PS data. Interrupt can be cleared by reading data out from register: INT\_Flag. All command codes should follow read word and write word protocols.

Send word → write command to VCNL36687S



Receive word → read data from VCNL36687S



S = start condition  
P = stop condition  
A = acknowledge  
N = not acknowledge

☐ Host action

☒ VCNL36687S response

Fig. 9 - Write Word and Read Word Protocol

**Function Description**

For proximity sensor function, VCNL36687S supports different kinds of mechanical designs to achieve the best proximity detection performance for any color of object with more flexibility. The basic PS function settings, such as period, persistence, INT, and shut down are handled by the register: PS\_CONF1. Period controls the PS response time. Integration time represents the duration of the energy being received. The Interrupt is asserted when the PS detection levels over the high threshold level setting (register: PS\_THDH) or lower than low threshold (register: PS\_THDL). If the Interrupt function is enabled, the host reads the PS output data from VCNL36687S that saves host loading from periodically reading PS data. More than that, INT flag (register: INT\_Flag) indicates the behavior of INT triggered under different conditions. PS persistence (PS\_PERS) sets up the PS INT asserted conditions as long as the PS output value continually exceeds the threshold level. The intelligent cancellation level can be set on register: PS\_CANC to reduce the cross talk phenomenon.

VCNL36687S also supports easy use of proximity detection logic output mode that outputs just high / low levels saving loading from the host. Normal operation mode or proximity detection logic output mode can be selected on the register: PS\_MS. A smart persistence is provided to get faster PS response time and prevent false trigger for PS. Descriptions of each slave address operation are shown in Table 1.

**TABLE 1 - COMMAND CODE AND REGISTER DESCRIPTION**

| COMMAND CODE | DATE BYTE LOW / HIGH | REGISTER NAME | R / W | DEFAULT VALUE | FUNCTION DESCRIPTION                                                     |
|--------------|----------------------|---------------|-------|---------------|--------------------------------------------------------------------------|
| 0x03         | L                    | PS_CONF1      | R/W   | 0x01          | PS period, persistence, INT and smart persistence and function selection |
|              | H                    | PS_CONF2      | R/W   | 0x00          | PS IT and start selection                                                |
| 0x04         | L                    | PS_CONF3      | R/W   | 0x00          | PS active force mode                                                     |
|              | H                    | PS_CONF4      | R/W   | 0x00          | PS VCSEL current selection                                               |
| 0x05         | L                    | PS_THDL_L     | R/W   | 0x00          | PS low interrupt threshold setting LSB byte                              |
|              | H                    | PS_THDL_M     | R/W   | 0x00          | PS low interrupt threshold setting MSB byte                              |
| 0x06         | L                    | PS_THDH_L     | R/W   | 0x00          | PS high interrupt threshold setting LSB byte                             |
|              | H                    | PS_THDH_M     | R/W   | 0x00          | PS high interrupt threshold setting MSB byte                             |
| 0x07         | L                    | PS_CANC_L     | R/W   | 0x00          | PS cancellation level setting                                            |
|              | H                    | PS_CANC_M     | R/W   | 0x00          | PS cancellation level setting                                            |
| 0x08         | L                    | PS_CONF5      | R/W   | 0x00          | PS power on start setting                                                |
|              | H                    | Reserved      | R/W   | 0x00          | Reserved                                                                 |
| 0xF2         | L                    | PS_Data_L     | R     | 0x00          | PS LSB output data                                                       |
|              | H                    | PS_Data_M     | R     | 0x00          | PS MSB output data                                                       |
| 0xF3         | L                    | Reserved      | R     | 0x00          | Reserved                                                                 |
|              | H                    | INT_Flag      | R     | 0x00          | PS interrupt flags                                                       |
| 0xF4         | L                    | ID_L          | R     | 0x88          | Device ID LSB                                                            |
|              | H                    | ID_M          | R     | 0x05          | Device ID MSB                                                            |

**Note**

- All of reserved register are used for internal test. Please keep as default setting

**Command Register Format**

VCNL36687S provides an 8-bit command register for PS controlling independently. The description of each command format is shown in the following tables.

**TABLE 2 - REGISTER: PS\_CONF1 DESCRIPTION**

| REGISTER NAME |       | COMMAND CODE: 0x03_L (0x00 DATA BYTE LOW)                                                                                           |
|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| Command       | Bit   | Description                                                                                                                         |
| PS_Period     | 7 : 6 | (0 : 0) = 8 ms, (0 : 1) = 16 ms, (1 : 0) = 32 ms, (1 : 1) = 64 ms<br>PS sample period setting                                       |
| PS_PERS       | 5 : 4 | (0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 3, (1 : 1) = 4<br>PS interrupt persistence setting                                              |
| PS_INT        | 3 : 2 | (0 : 0) = interrupt disable, (0 : 1) = interrupt disable, (1 : 0) = interrupt enable,<br>(1 : 1) = trigger by logic high / low mode |
| PS_SMART_PERS | 1     | 0 = disable ; 1 = enable PS smart persistence                                                                                       |
| PS_SD         | 0     | 0 = PS power on, 1 = PS shut down, default = 1                                                                                      |

**TABLE 3 - REGISTER: PS\_CONF2 DESCRIPTION**

|          |       | COMMAND CODE: 0x03_H (0x03 DATA BYTE HIGH)                                    |
|----------|-------|-------------------------------------------------------------------------------|
| Command  | Bit   | Description                                                                   |
| PS_IT    | 7 : 6 | (0 : 0) = 1T, (0 : 1) = 2T, (1 : 0) = 4T, (1 : 1) = 8T                        |
| PS_MPS   | 5 : 4 | (0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 4, (1 : 1) = 8;<br>PS multi-pulse setting |
| PS_ITB   | 3     | 0 = 25 $\mu$ s, 1 = 50 $\mu$ s, PS IT bank setting                            |
| Reserved | 2 : 0 | Default = 0                                                                   |

**TABLE 4 - REGISTER: PS\_CONF3 DESCRIPTION**

|             |       | COMMAND CODE: 0x04_L (0x04 DATA BYTE LOW)                                                                                                                                            |
|-------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register    | Bit   | Description                                                                                                                                                                          |
| Reserved    | 7     | 0                                                                                                                                                                                    |
| PS_AF       | 6     | 0 = auto mode; 1 = force mode                                                                                                                                                        |
| PS_FOR_Trig | 5     | 0 = no PS active force mode trigger, 1 = trigger one time cycle<br>VCNL36687S output one cycle data every time host writes in "1" to sensor. The state returns to "0" automatically. |
| Reserved    | 4     | 0                                                                                                                                                                                    |
| Reserved    | 3 : 0 | (0 : 0 : 0 : 0)                                                                                                                                                                      |

**TABLE 5 - REGISTER: PS\_CONF4 DESCRIPTION**

|           |       | COMMAND CODE: 0x04_H (0x04 DATA BYTE HIGH)                                                                                                                                                 |
|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register  | Bit   | Description                                                                                                                                                                                |
| PS_SC_EN  | 7     | 0 = turn off sunlight cancel; 1 = turn on sunlight cancel; PS sunlight cancel function enable setting                                                                                      |
| PS_SC_CUR | 6 : 5 | (0 : 0) = 1 x typical sunlight cancel current, (0 : 1) = 2 x typical sunlight cancel current, (1 : 0) = 4 x typical sunlight cancel current, (1 : 1) = 8 x typical sunlight cancel current |
| PS_HD     | 4     | 0 = PS output is 12 bits, 1 = PS output is 16 bits                                                                                                                                         |
| Reserved  | 3     | 0                                                                                                                                                                                          |
| VCSEL_I   | 2 : 0 | (0 : 0 : 0) = 7 mA; (0 : 0 : 1) = 11 mA; (0 : 1 : 0) = 14 mA; (0 : 1 : 1) = 17 mA; (1 : 0 : 0) = 20 mA;<br>VCSEL current selection setting                                                 |

**TABLE 6 - REGISTER: PS\_THDL\_L AND PS\_THDL\_M DESCRIPTION**

| COMMAND CODE: 0x05_L (0x05 DATA BYTE LOW) AND 0x05_H (0x05 DATA BYTE HIGH) |       |                                                           |
|----------------------------------------------------------------------------|-------|-----------------------------------------------------------|
| Command                                                                    | Bit   | Description                                               |
| PS_THDL_L                                                                  | 7 : 0 | 0x00 to 0xFF, PS interrupt low threshold setting_LSB byte |
| PS_THDL_M                                                                  | 7 : 0 | 0x00 to 0x0F, PS interrupt low threshold setting_MSB byte |

**TABLE 7 - REGISTER: PS\_THDH\_L AND PS\_THDH\_M DESCRIPTION**

| COMMAND CODE: 0x06_L (0x06 DATA BYTE LOW) AND 0x06_H (0x06 DATA BYTE HIGH) |       |                                                            |
|----------------------------------------------------------------------------|-------|------------------------------------------------------------|
| Command                                                                    | Bit   | Description                                                |
| PS_THDH_L                                                                  | 7 : 0 | 0x00 to 0xFF, PS interrupt high threshold setting_LSB byte |
| PS_THDH_M                                                                  | 7 : 0 | 0x00 to 0x0F, PS interrupt high threshold setting_MSB byte |

**TABLE 8 - REGISTER: PS\_CANC\_L AND PS\_CANC\_M DESCRIPTION**

| COMMAND CODE: 0x07_L (0x07 DATA BYTE LOW) AND 0x07_H (0x07 DATA BYTE HIGH) |       |                                                          |
|----------------------------------------------------------------------------|-------|----------------------------------------------------------|
| Command                                                                    | Bit   | Description                                              |
| PS_CANC_L                                                                  | 7 : 0 | 0x00 to 0xFF, PS cancellation level setting_LSB byte     |
| PS_CANC_M                                                                  | 7 : 0 | 0x00 to 0x0F, PS MSB cancellation level setting_MSB byte |

**TABLE 9 - REGISTER: PS\_CONF5 DESCRIPTION**

| COMMAND CODE: 0x08_L (0x08 DATA BYTE LOW) AND 0x08_H (0x08 DATA BYTE HIGH) |       |                                      |
|----------------------------------------------------------------------------|-------|--------------------------------------|
| Register                                                                   | Bit   | Description                          |
| Reserved_L                                                                 | 7 : 1 | Reserved                             |
| POR_S                                                                      | 0     | When use PS function, must write "1" |
| Reserved_M                                                                 | 7 : 0 | Reserved                             |

**TABLE 10 - READ OUT REGISTER DESCRIPTION**

| Register  | Command Code                 | Bit                                  | Description                                                                                                                                                                                                         |
|-----------|------------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PS_Data_L | 0xF2_L (0xF2 data byte low)  | 7 : 0                                | 0x00 to 0xFF, PS LSB output data                                                                                                                                                                                    |
| PS_Data_M | 0xF2_H (0xF2 data byte high) | 7 : 0                                | 3 : 0 PS output code<br>6 : 4 reserved<br>7 : "0" Normal output, "1" enter sunlight protection mode<br>PS_Data_L= 00000000<br>PS_Data_M= 10000000                                                                   |
| Reserved  | 0xF3_L (0xF3 data byte low)  | 7 : 0                                | Default = 0x00                                                                                                                                                                                                      |
| INT_Flag  | 0xF3_H (0xF3 data byte high) | 7<br>6<br>5<br>4<br>3<br>2<br>1<br>0 | Reserved<br>Reserved<br>Reserved<br>PS_SPFLAG, PS entering protection mode<br>Reserved<br>Reserved<br>PS_IF_CLOSE, PS rises above PS_THDH INT trigger event<br>PS_IF_AWAY, PS drops below PS_THDL INT trigger event |
| ID_L      | 0xF4_L (F4H data byte low)   | 7 : 0                                | 88H for MP version sample<br>Device ID LSB byte                                                                                                                                                                     |
| ID_M      | 0xF4_H (F4H data byte high)  | 7 : 6<br>5 : 4<br>3 : 0              | (0 : 0)<br>(0 : 0) slave address = 0x60<br>Version code (0 : 1 : 0 : 1); device ID MSB byte                                                                                                                         |

## Initialization

VCNL36687S includes default values for each register. As long as power is on, it is ready to be controlled by host via I<sup>2</sup>C bus.

**Threshold Window Setting**

- **Programmable PS Threshold**  
VCNL36687S provides both high and low thresholds 12-bit data setting for PS (register: PS\_THDL, PS\_THDH).
- **PS Persistence**  
The PS persistence function (PS\_PERS, 1\2\3\4) helps to avoid false trigger of the PS INT. For example, if PS\_PERS = 3 times, the PS INT will not be asserted unless the PS value is greater than the PS threshold (PS\_THDH) value for three periods of time continuously
- **PS Active Force Mode**  
An extreme power saving way to use PS is to apply PS active force (register: PS\_CONF3 command: PS\_AF = 1) mode. Anytime host would like to read out just one of PS data, write in "1" at register: PS\_CONF3 command: PS\_FOR\_Trig. Without commands placed, there is no PS data output. VCNL36687S stays in standby mode constantly
- **PS Detection Object**  
Any color of object is detectable by VCNL36687S

**Data Access**

For PS data reading, it has to apply two bytes. One byte is for LSB, and the other byte is for MSB (4 bits) as shown in Table 11.

| TABLE 11 - VCNL36687S 12-BIT PS DATA FORMAT |                                                                                                       |    |    |    |          |    |   |   |          |   |   |   |   |   |   |   |
|---------------------------------------------|-------------------------------------------------------------------------------------------------------|----|----|----|----------|----|---|---|----------|---|---|---|---|---|---|---|
|                                             | VCNL36687S                                                                                            |    |    |    |          |    |   |   |          |   |   |   |   |   |   |   |
| Bit                                         | 15                                                                                                    | 14 | 13 | 12 | 11       | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register                                    | Bit 15: “0” normal operation, “1” enter sunlight protection mode, PS output = 1000000000000000(32768) |    |    |    | PS_DataM |    |   |   | PS_DataL |   |   |   |   |   |   |   |

**Intelligent Cancellation**

VCNL36687S provides an intelligent cancellation method to reduce cross talk for the proximity sensor. The output data will be subtracted by the input value stored in register: PS\_CANC.

**Interruption (INT)**

VCNL36687S has PS interrupt feature operated by a single pin "INT". The purpose of the interrupt feature is to actively inform the host once INT has been asserted. With the interrupt function applied, the host does not need to be constantly pulling data from the sensor, but to read data from the sensor while receiving interrupt request from the sensor.

**Interruption Flag**

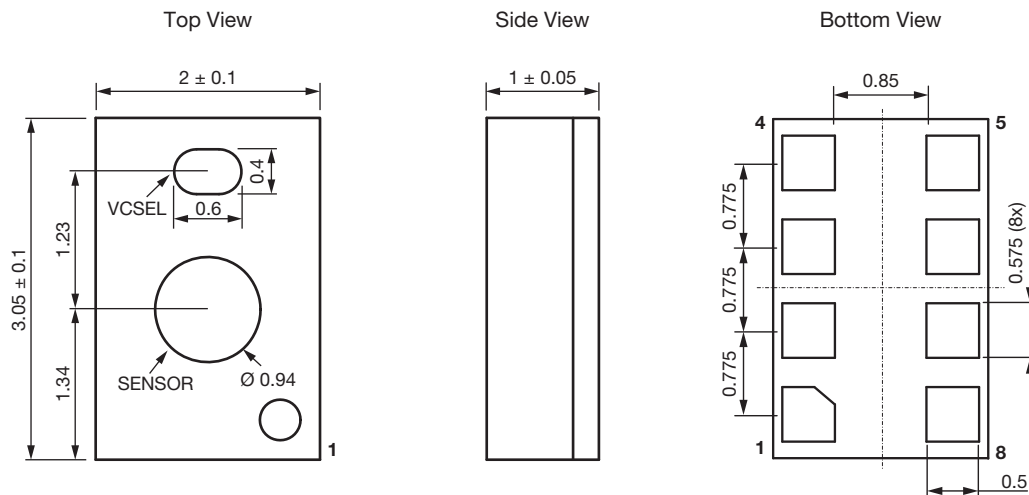
Register: INT\_Flag represents all of interrupt trigger status for PS. Any flag value changes from "0" to "1" state, the level of INT pin will be pulled low. As long as host reads INT\_Flag data, the bit will change from "1" state to "0" state after reading out, the INT level will be returned to high afterwards.

**PROXIMITY DETECTION LOGIC OUTPUT MODE**

VCNL36687S provides a proximity detection logic output mode that uses INT pin (pin 6) as a proximity detection logic high / low output (register: PS\_INT = 3). When this mode is selected, the PS output (pin 6; INT/P<sub>OUT</sub>) is pulled low when an object is closing to be detected and returned to level high when the object moves away. Register: PS\_THDHL defines how sensitive PS detection is.

**PROXIMITY DETECTION HYSTERESIS**

A PS detection hysteresis is important that keeps PS state in a certain range of detection distance. For example, PS INT asserts when PS value over PS\_THDH. Host switches off panel backlight and then clears INT. When PS value is less than PS\_THDL, Host switches on panel backlight. Any PS value lower than PS\_THDH or higher than PS\_THDL, PS INT will not be asserted. Host does keep the same state.

**PACKAGE INFORMATION**


|   |                 |   |         |
|---|-----------------|---|---------|
| 1 | GND             | 5 | VCSEL_C |
| 2 | V <sub>PP</sub> | 6 | INT     |
| 3 | V <sub>DD</sub> | 7 | SDA     |
| 4 | VCSEL_A         | 8 | SCL     |

Fig. 10 - VCNL36687S Package Dimensions

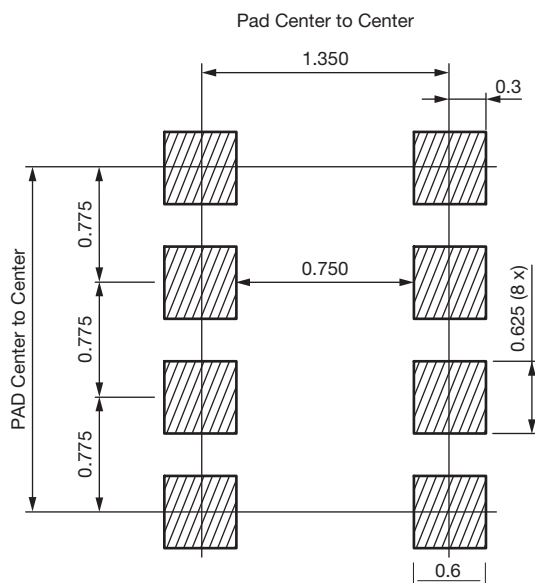
**LAYOUT PAD INFORMATION**


Fig. 11 - VCNL36687S PCB Layout Footprint

# APPLICATION CIRCUIT BLOCK REFERENCE

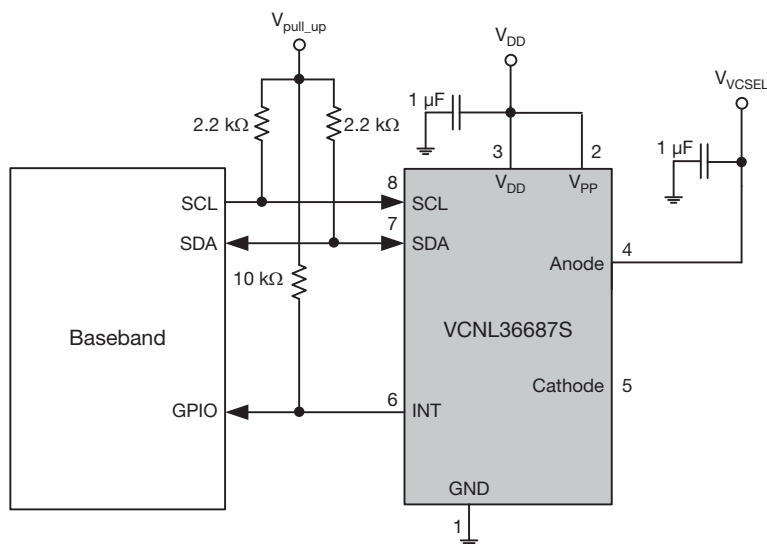


Fig. 12 - VCNL36687S Application Circuit (normal operation with interrupt function)

| RECOMMENDED STORAGE AND REBAKING CONDITIONS |                                                          |      |      |        |
|---------------------------------------------|----------------------------------------------------------|------|------|--------|
| PARAMETER                                   | CONDITIONS                                               | MIN. | MAX. | UNIT   |
| Storage temperature                         |                                                          | 5    | 50   | °C     |
| Relative humidity                           |                                                          | -    | 60   | %      |
| Open time                                   |                                                          | -    | 168  | h      |
| Total time                                  | From the date code on the aluminized envelope (unopened) | -    | 12   | months |
| Rebaking                                    | Tape and reel: 60 °C                                     | -    | 22   | h      |
|                                             | Tube: 60 °C                                              | -    | 22   | h      |

## RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020 C

| IR REFLOW PROFILE CONDITION                |            |                                       |               |
|--------------------------------------------|------------|---------------------------------------|---------------|
| PARAMETER                                  | CONDITIONS | TEMPERATURE                           | TIME          |
| Peak temperature                           |            | 260 °C + 5 °C / - 5 °C (max.: 265 °C) | 10 s          |
| Preheat temperature range and timing       |            | 150 °C to 200 °C                      | 60 s to 180 s |
| Timing within 5 °C to peak temperature     |            | -                                     | 10 s to 30 s  |
| Timing maintained above temperature / time |            | 217 °C                                | 60 s to 150 s |
| Timing from 25 °C to peak temperature      |            | -                                     | 8 min (max.)  |
| Ramp-up rate                               |            | 3 °C/s (max.)                         | -             |
| Ramp-down rate                             |            | 6 °C/s (max.)                         | -             |

Recommend Normal Solder Reflow is 235 °C to 265 °C

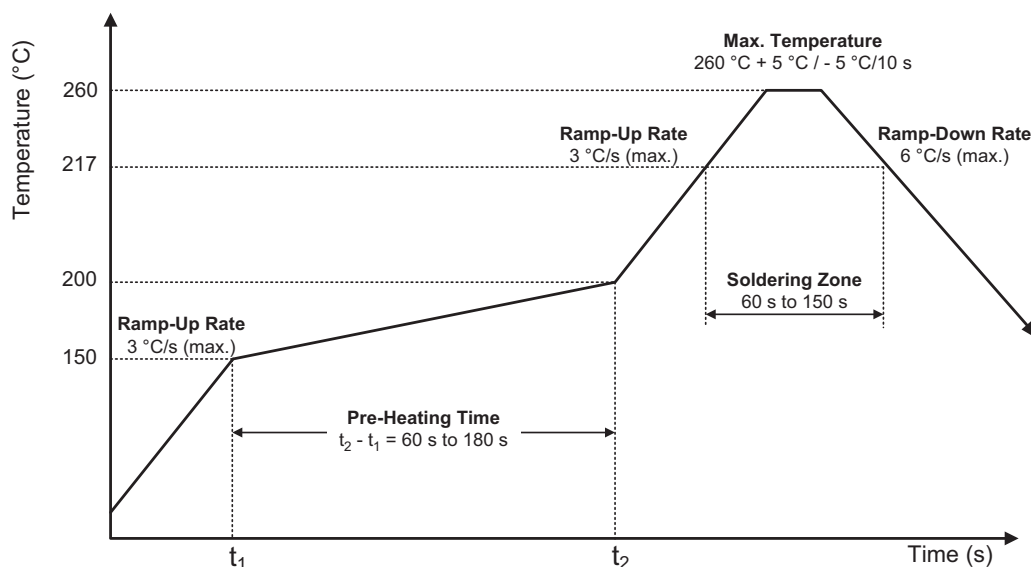


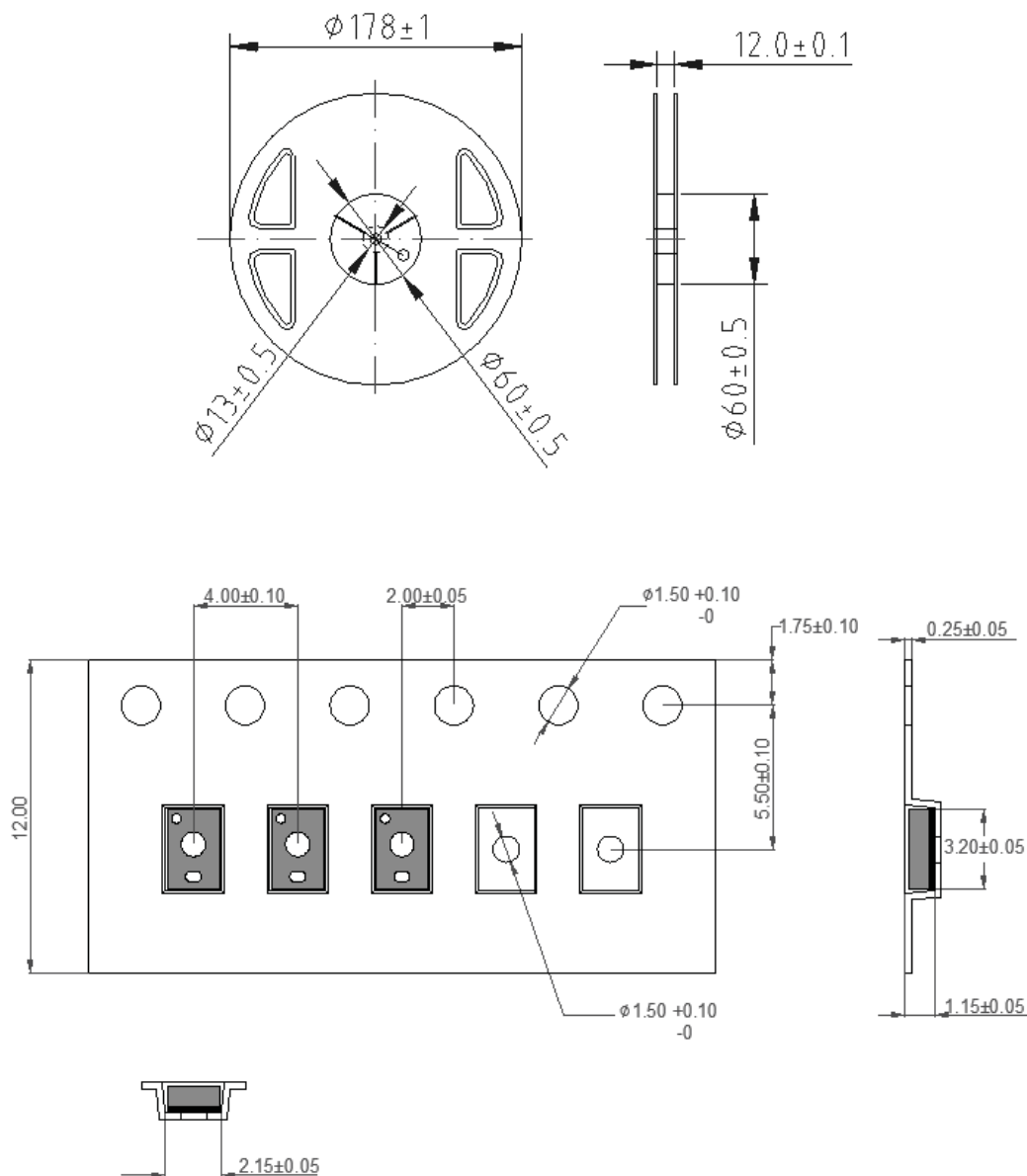
Fig. 13 - VCNL36687S Solder Reflow Profile Chart

## RECOMMENDED IRON TIP SOLDERING CONDITION AND WARNING HANDLING

- Solder the device with the following conditions:
  - Soldering temperature: 400 °C (max.)
  - Soldering time: 3 s (max.)
- If the temperature of the method portion rises in addition to the residual stress between the leads, the possibility that an open or short circuit occurs due to the deformation or destruction of the resin increases
- The following methods: VPS and wave soldering, have not been suggested for the component assembly
- Cleaning method conditions:
  - Solvent: methyl alcohol, ethyl alcohol, isopropyl alcohol
  - Solvent temperature < 45 °C (max.)
  - Time: 3 min (min.)



**TAPE PACKAGING INFORMATION** in millimeters





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