Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35 µW) with high speed (t_{ON}: 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Vishay Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411, DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- 44 V supply max. rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 25 Ω
- Fast switching - t_{ON}: 110 ns
- Ultra low power - P_D: 0.35 µW
- TTL, CMOS compatible
- Single supply capability
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

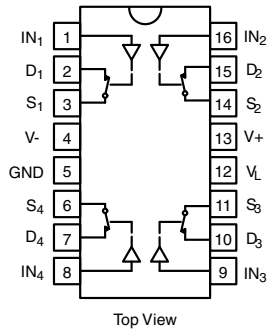
- Widest dynamic range
- Low signal errors and distortion
- Break-bevor-make switching action
- Simple interfacing

APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals

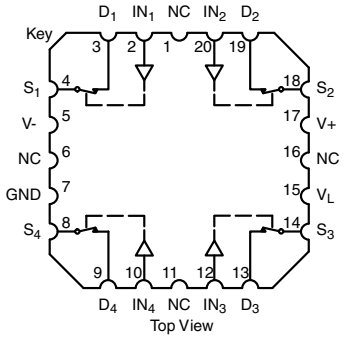
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG411
Dual-In-Line and SOIC



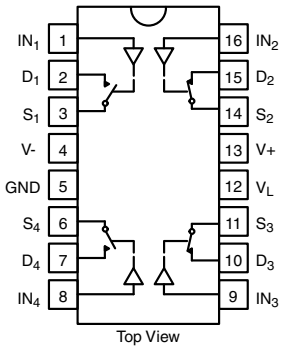
Top View

DG411
LCC



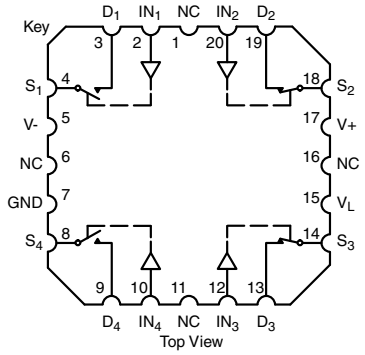
Top View

DG413
Dual-In-Line and SOIC



Top View

DG413
LCC



Top View

TRUTH TABLE		
Logic	**DG411**	**DG412**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE		
Logic	**SW_1, SW_4**	**SW_2, SW_3**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin plastic DIP	DG411DJ DG411DJ-E3
		DG412DJ DG412DJ-E3
		DG413DJ DG413DJ-E3
	16-pin narrow SOIC	DG411DY DG411DY-E3 DG411DY-T1 DG411DY-T1-E3
		DG412DY DG412DY-E3 DG412DY-T1 DG412DY-T1-E3
		DG413DY DG413DY-E3 DG413DY-T1 DG413DY-T1-E3
	16-pin TSSOP	DG411DQ-E3 DG411DQ-T1-E3
		DG412DQ-E3 DG412DQ-T1-E3
		DG413DQ-E3 DG413DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V + to V -		44	V
GND to V -		25	
V_L		(GND - 0.3) to (V+) + 0.3	
Digital Inputs[a], V_S, V_D		(V-) -2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle)		100	
Storage Temperature	(AK, AZ suffix)	- 65 to 150	°C
	(DJ, DY suffix)	- 65 to 125	
Power Dissipation (Package)[b]	16-pin plastic DIP[c]	470	mW
	16-pin narrow SOIC[d]	600	
	16-pin CerDIP[e]	900	
	LCC-20[e]	900	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V + or V - will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 25 °C.
d. Derate 7.6 mW/°C above 75 °C.
e. Derate 12 mW/°C above 75 °C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V + = 15 V, V - = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V + = 13.5 V, V - = - 13.5 V I_S = - 10 mA, V_D = ± 8.5 V	Room Full	25		35 45		35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V + = 16.5, V - = - 16.5 V V_D = ± 15.5 V, V_S = ± 15.5 V	Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA
	$I_{D(off)}$		Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	V + = 16.5 V, V - = - 16.5 V V_S = V_D = ± 15.5 V	Room Full	± 0.1	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 10 V, see figure 2	Room Full	110		175 240		175 220	ns
Turn-Off Time	t_{OFF}		Room Full	100		145 160		145 160	
Break-Before-Make Time Delay	t_D	DG413 only, V_S = 10 V R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 0 V, R_g = 0 Ω C_L = 10 nF	Room	5					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	9					
Channel On Capacitance[e]	$C_{D(on)}$		Room	35					
Power Supplies									
Positive Supply Current	I+	V + = 16.5 V, V - = - 16.5 V V_{IN} = 0 V or 5 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Full	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room Full	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Full	- 0.0001	- 1 - 5		- 1 - 5		

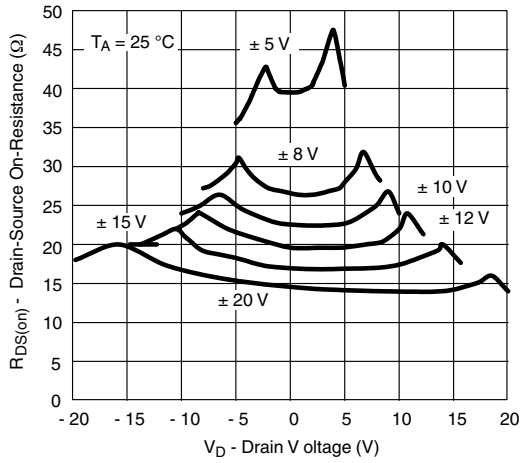
SPECIFICATIONS[a] (for Unipolar Supplies)

Parameter	Symbol	Test Conditions Unless Specified V + = 12 V, V - = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min.[d]	Max.[d]	Min.[d]	Max.[d]	
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			12		12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V + = 10.8 V, I_S = - 10 mA, V_D = 3 V, 8 V	Room Full	40		80 100		80 100	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 8 V, see figure 2	Room Hot	175		250 400		250 315	ns
Turn-Off Time	t_{OFF}		Room Hot	95		125 140		125 140	
Break-Before-Make Time Delay	t_D	DG413 only, V_S = 8 V R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 6 V, R_g = 0 Ω, C_L = 10 nF	Room	25					pC
Power Supplies									
Positive Supply Current	I+	V + = 13.5 V, V_{IN} = 0 V or 5 V	Room Hot	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Hot	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room Hot	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Hot	- 0.0001	- 1 - 5		- 5		

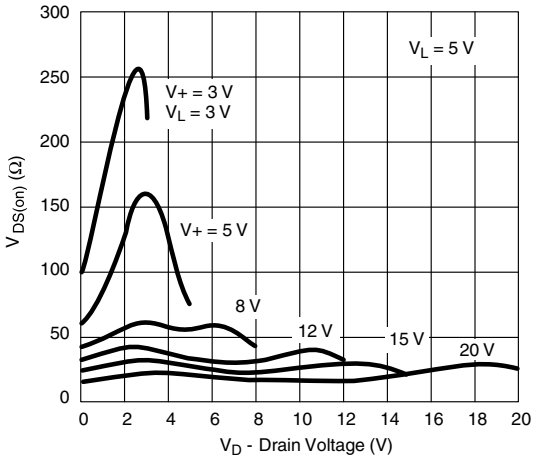
Notes:
a. Refer to process option flowchart.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

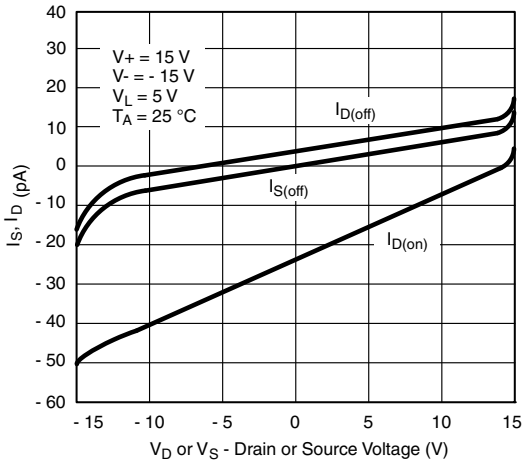


On-Resistance vs. V_D and Power Supply Voltage

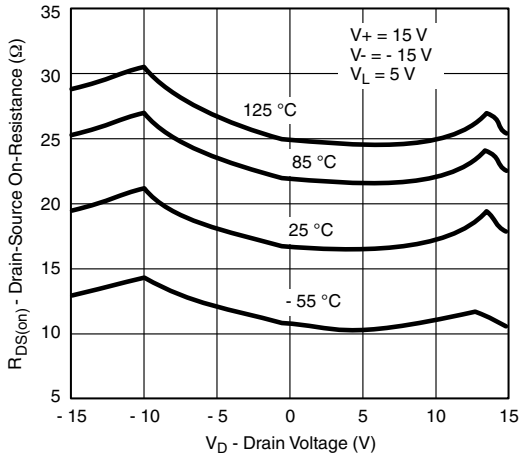


On-Resistance vs. V_D and Unipolar Supply Voltage

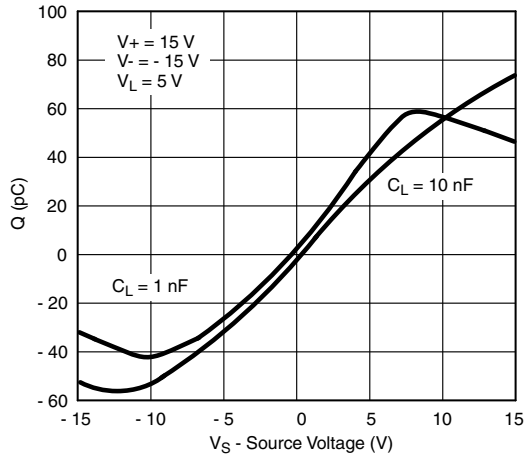
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



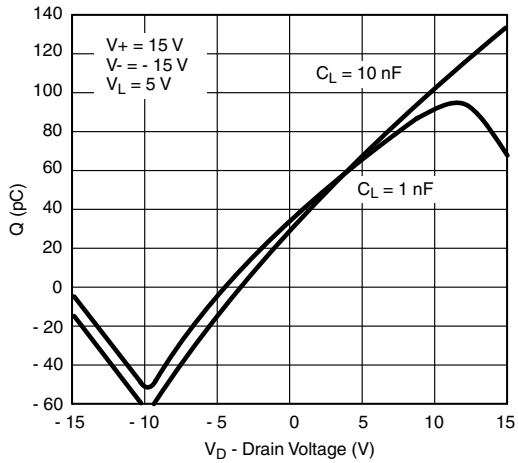
Leakage Current vs. Analog Voltage



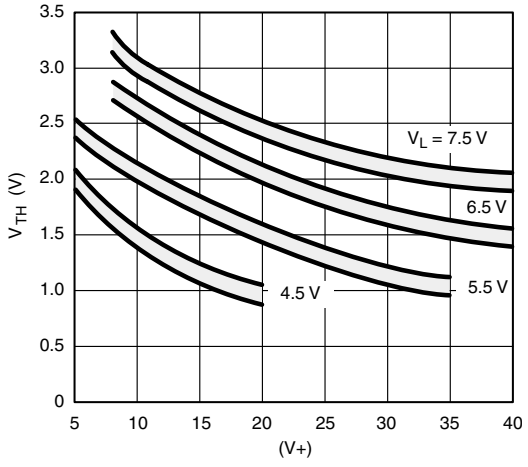
I_D, I_S Leakages vs. Temperature



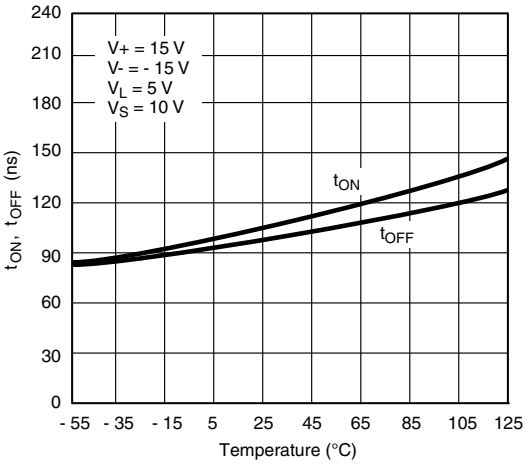
Charge Injection vs. Analog Voltage



Charge Injection vs. Analog Voltage

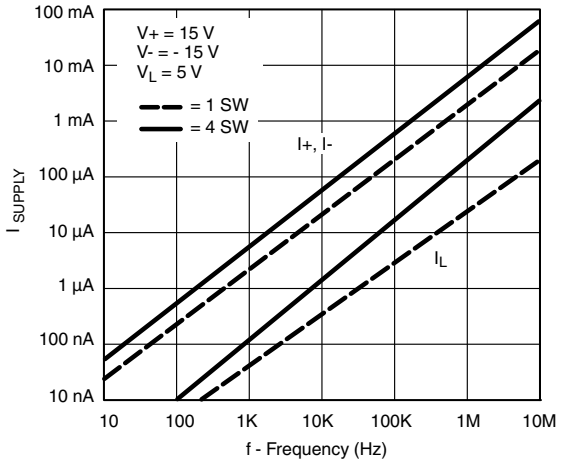


Input Switching Threshold vs. Supply Voltage



Switching Time vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Supply Current vs. Input Switching Frequency

SCHEMATIC DIAGRAM (Typical Channel)

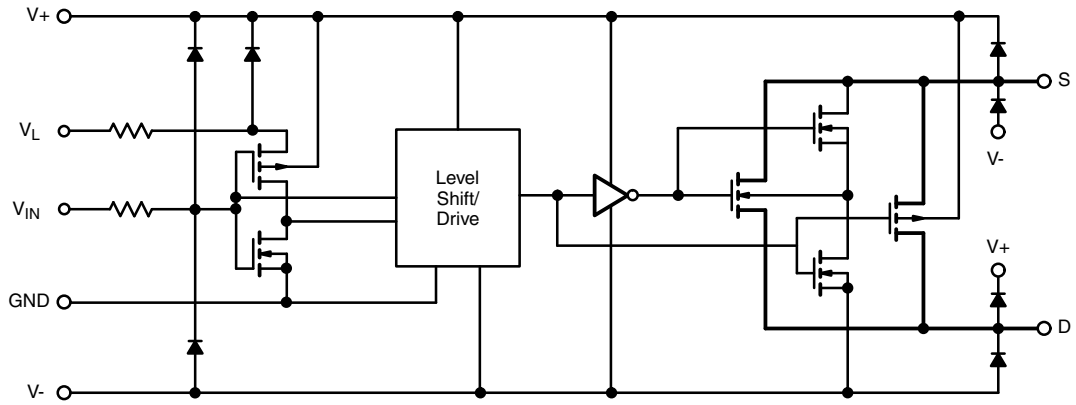
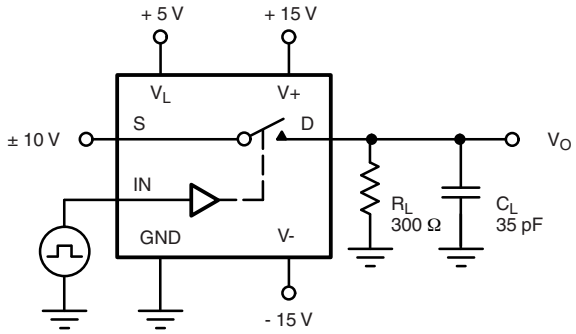


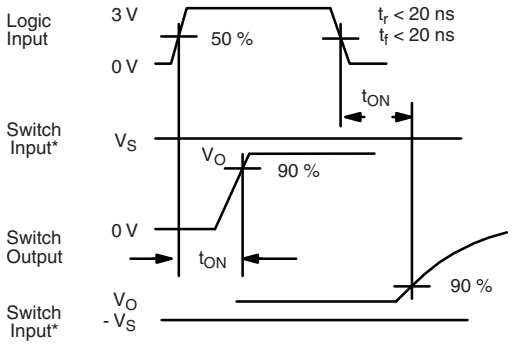
Figure 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

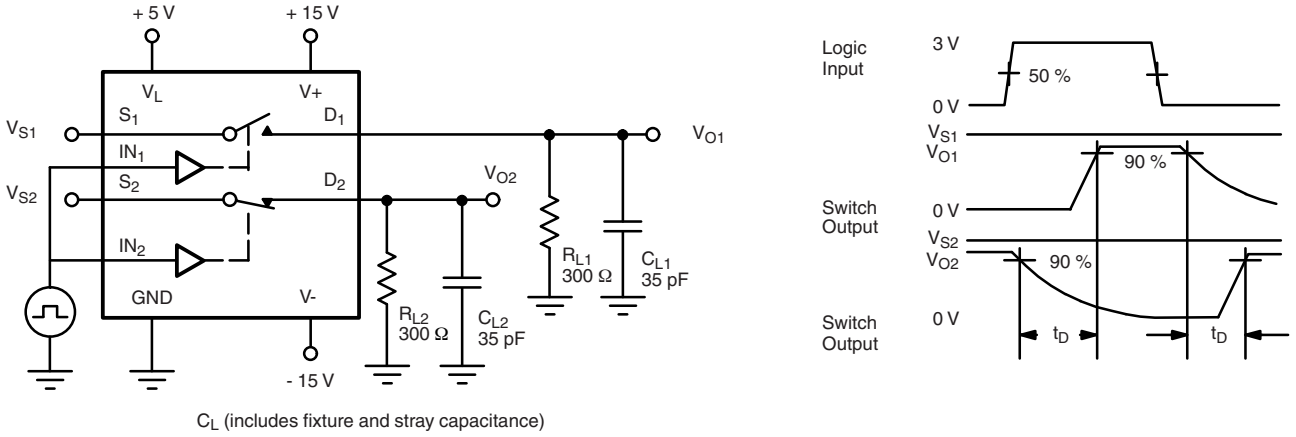


* V_S = 10 V for t_{ON}, V_S = - 10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

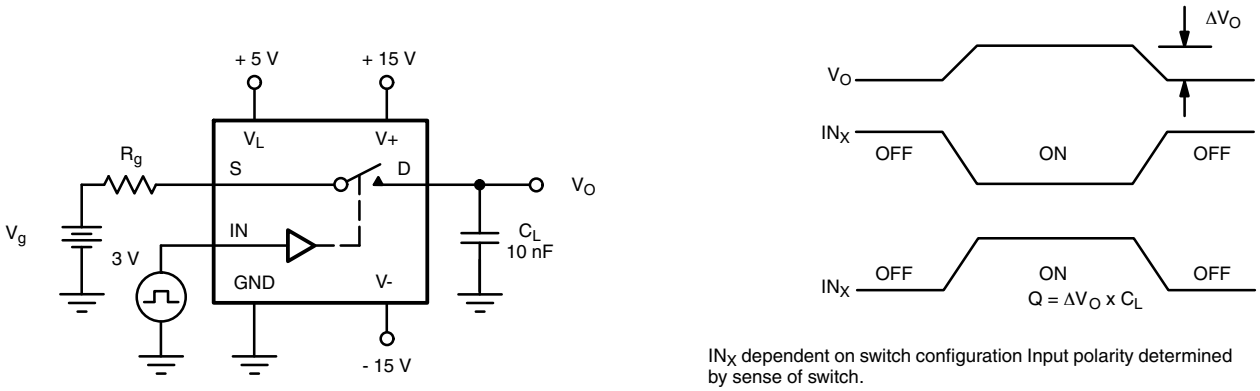
Figure 2. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make (DG413)



IN_X dependent on switch configuration Input polarity determined by sense of switch.

Figure 4. Charge Injection

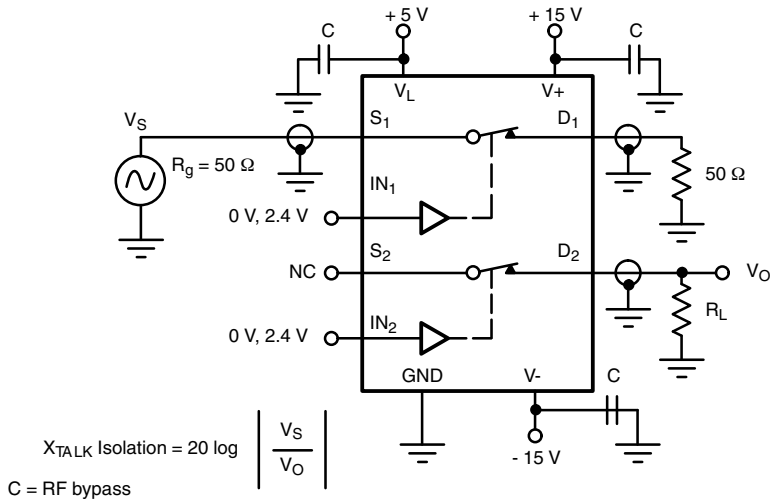


Figure 5. Crosstalk

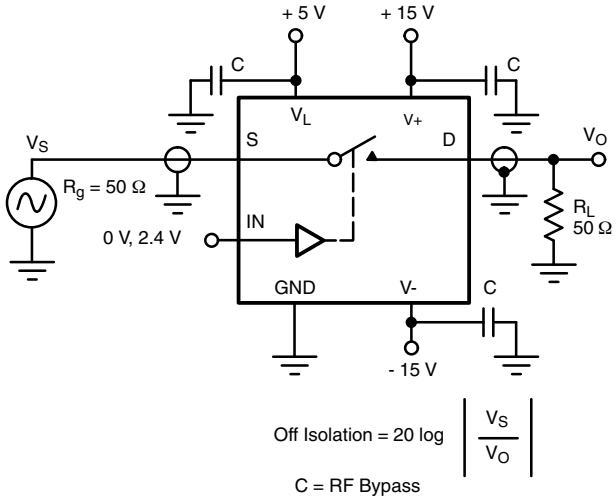


Figure 6. Off Isolation

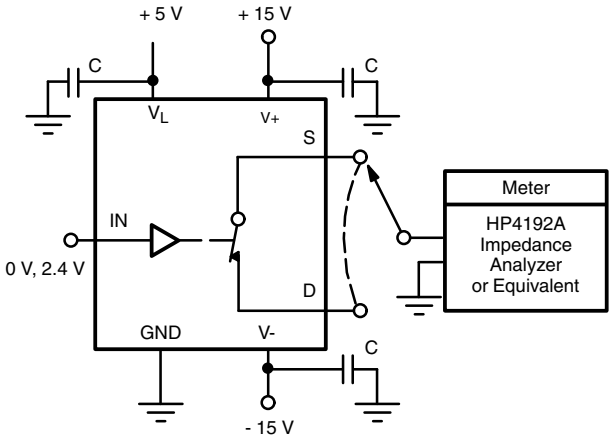


Figure 7. Source/Drain Capacitances

APPLICATIONS

Single Supply Operation:

The DG411, DG412, DG413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is tied to V_L and V- is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for V_L versus input threshold requirments.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

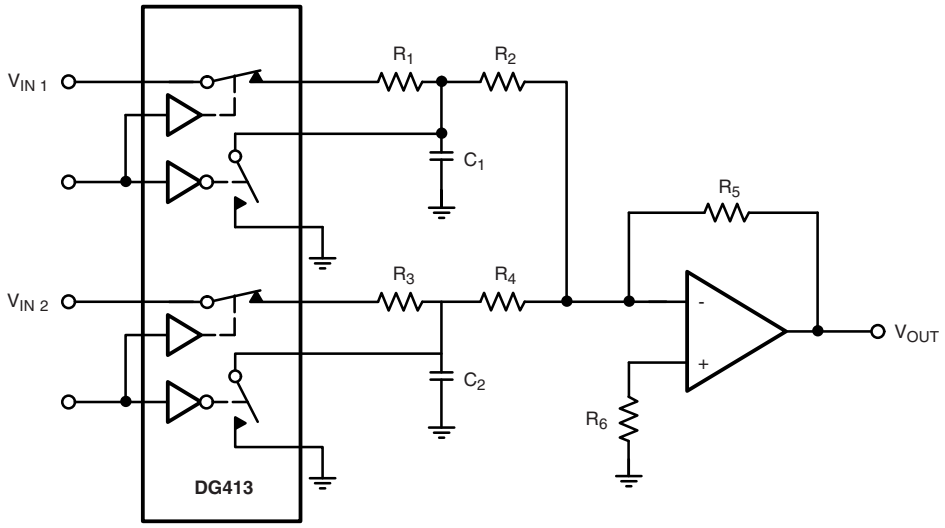


Figure 8. Summing Amplifier

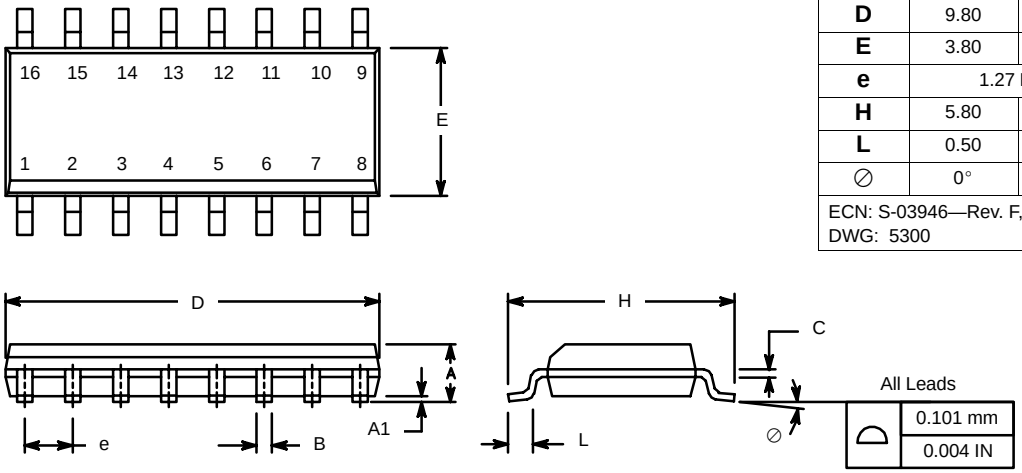
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70050.

SOIC (NARROW): 16-LEAD

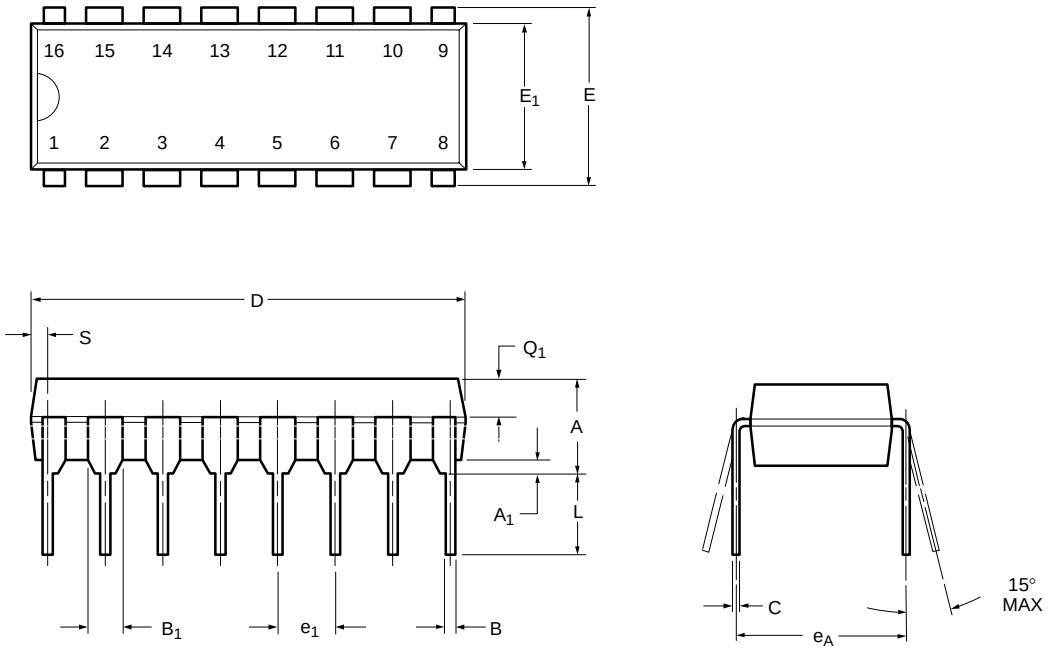
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

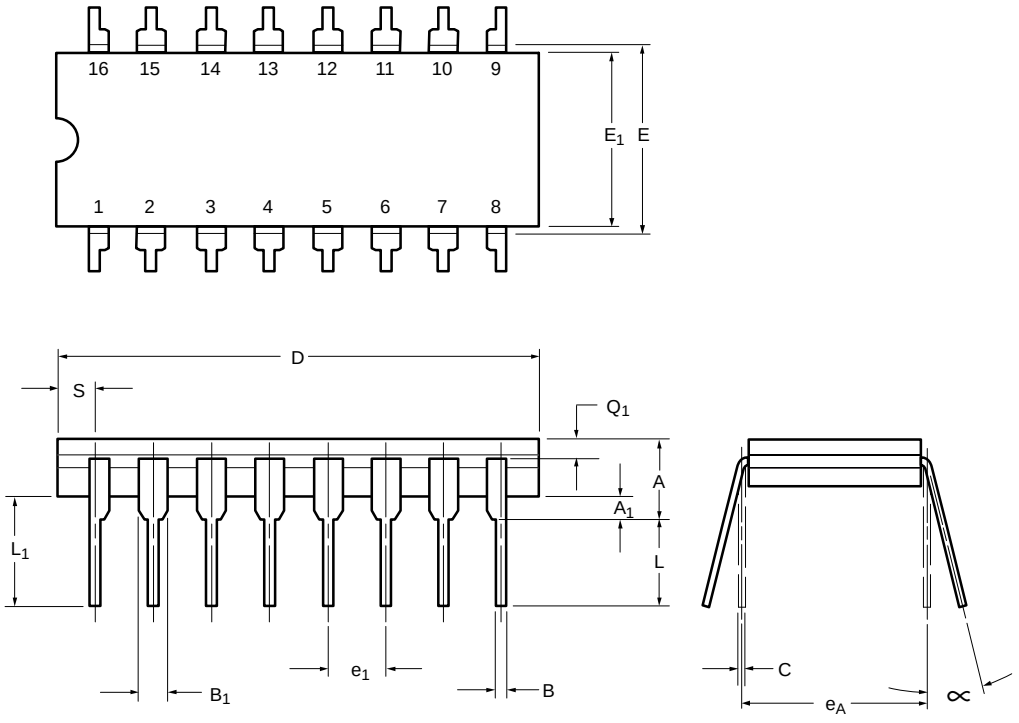


PDIP: 16-LEAD



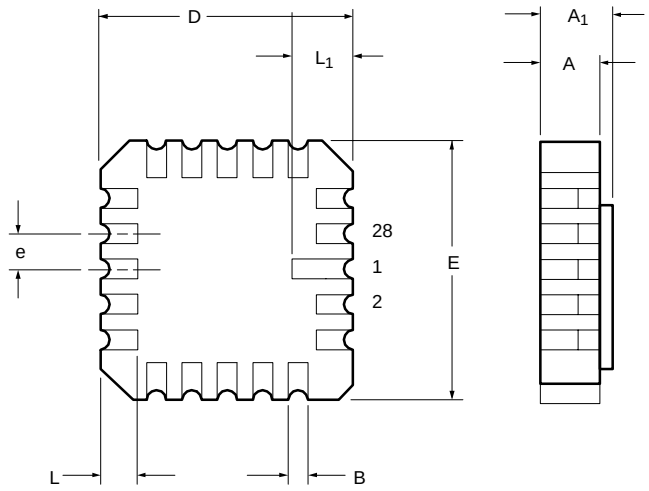
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				

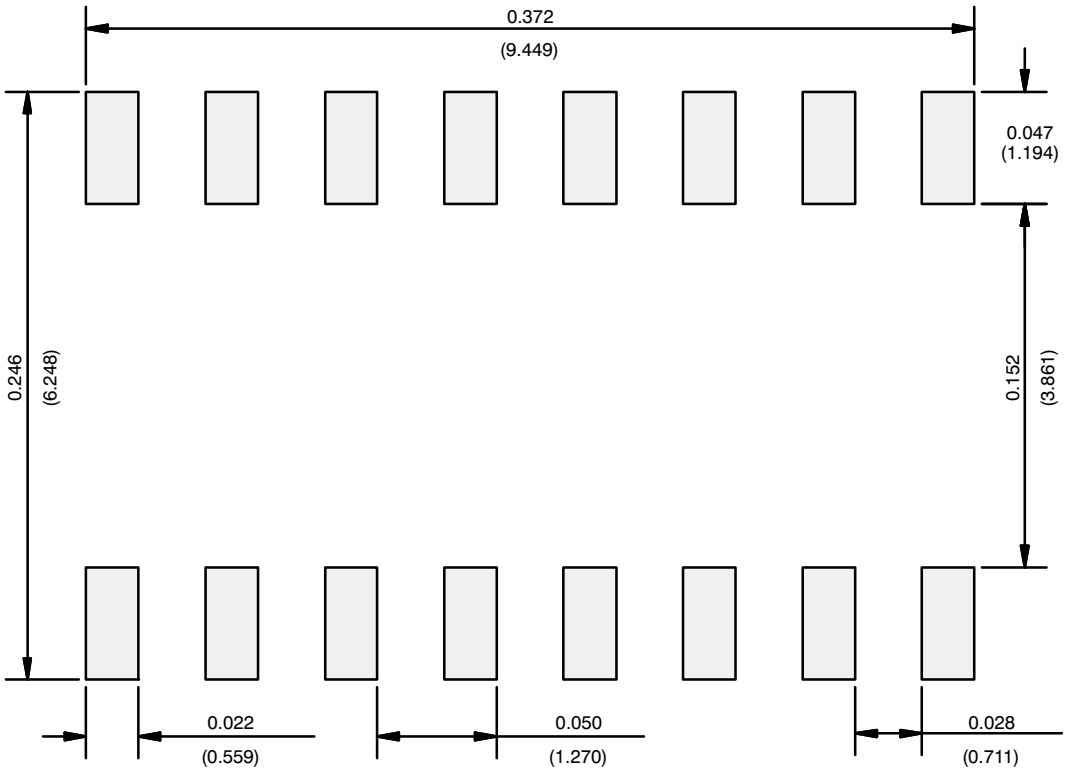
20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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