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Vishay Siliconix

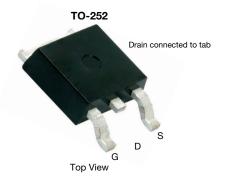
# Automotive N-Channel 60 V (D-S) 175 °C MOSFET

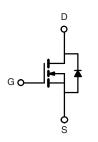
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	60				
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS}$ = 10 V	0.022				
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.033				
I <sub>D</sub> (A)	25				
Configuration	Single				
Package	TO-252				

#### **FEATURES**

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R<sub>q</sub> and UIS tested
- AEC-Q101 qualified d
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>







N-Channel MOSFET

ABSOLUTE MAXIMUM RATING	<b>GS</b> (T <sub>C</sub> = 25 °C, unless	s otherwise noted	d)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	± 20		
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	- I <sub>D</sub>	25	А
	T <sub>C</sub> = 125 °C		20	
Continuous Source Current (Diode Conduc	ction) <sup>a</sup>	I <sub>S</sub>	25	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	100	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	24	
Single Pulse Avalanche Energy	L = U.1 MH	E <sub>AS</sub>	28	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	Б	62	10/
	T <sub>C</sub> = 125 °C	$P_{D}$	20	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stq</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)			2.4	C/VV

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300 \,\mu\text{s}$ , duty cycle  $\leq 2 \,\%$ .
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	vise noted) TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					l	L	l	
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1.0		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	25	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.018	0.022	Ω	
Drain-Source On-State Resistance a	D	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.039		
Drain-Source On-State Resistance 4	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.049		
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 25 °C	-	0.027	0.033		
Forward Transconductance <sup>a</sup>	9fs	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12 A		-	32	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			=	1580	1975	pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	305	382		
Reverse Transfer Capacitance	C <sub>rss</sub>			-	130	163		
Total Gate Charge <sup>c</sup>	Qg			-	33	50		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, I_D = 25 \text{ A}$	-	5.3	-	nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	6.8			
Gate Resistance	$R_g$	f = 1 MHz		0.5	1.3	3.3	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 30 \text{ V}, \text{ R}_L = 1.2 \Omega$ $I_D \cong 25 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	8	12		
Rise Time <sup>c</sup>	t <sub>r</sub>			-	10	15	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	24	36		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	6	9		
Source-Drain Diode Ratings and Chara	cteristics b							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	100	Α	
Forward Voltage	$V_{SD}$	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0 V		-	0.9	1.5	V	

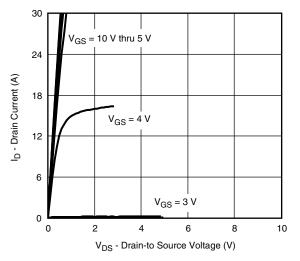
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

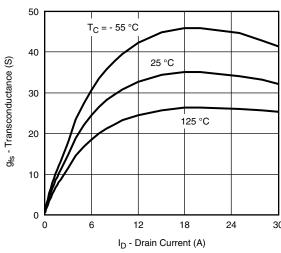
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



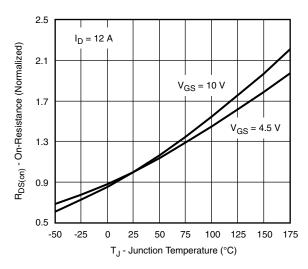
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



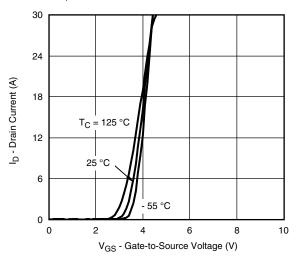




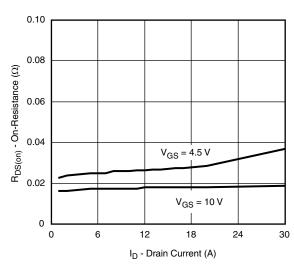
Transconductance



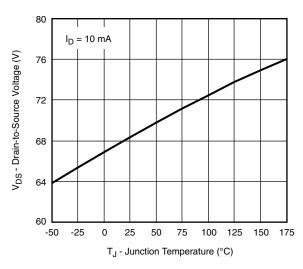
On-Resistance vs. Junction Temperature



**Transfer Characteristics** 



On-Resistance vs. Drain Current

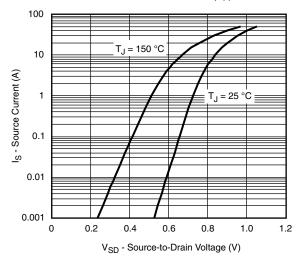


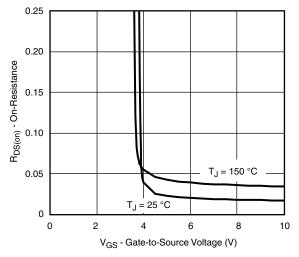
Drain Source Breakdown vs. Junction Temperature

For technical questions, contact: automostech



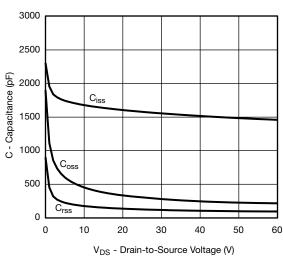
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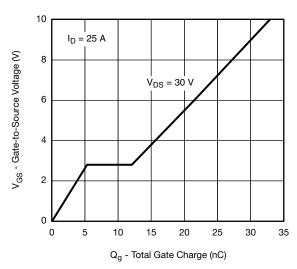




#### **Source Drain Diode Forward Voltage**

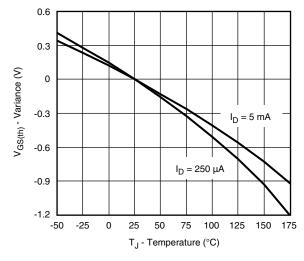






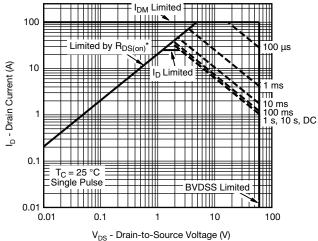
### Capacitance

**Gate Charge** 



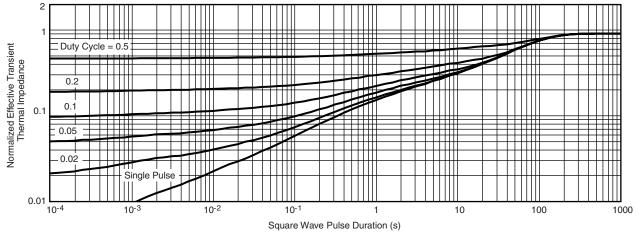


### **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



 $V_{DS}$  - Drain-to-Source Voltage (V) \*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

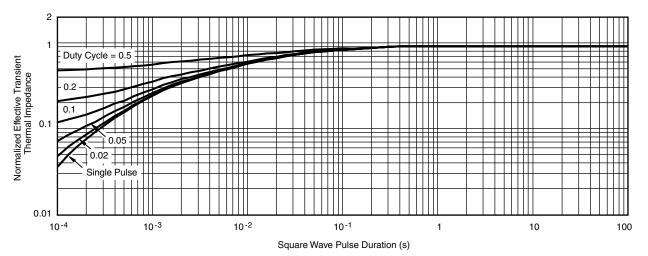
#### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg265360">www.vishay.com/ppg265360</a>.



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REVISION HISTORY a				
REVISION	DATE	DESCRIPTION OF CHANGE		
D	04-Aug-15	Revised R <sub>g</sub> minimum limit		

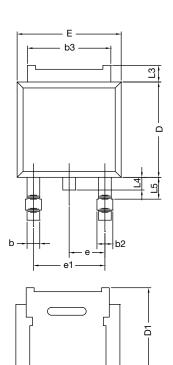
#### Note

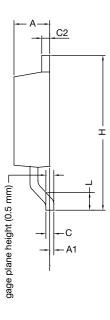
a. As of April 2014





## **TO-252AA Case Outline**





	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
А	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
С	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
Е	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
Н	9.40	10.41	0.370	0.410
е	2.28	BSC	0.090	BSC
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13				

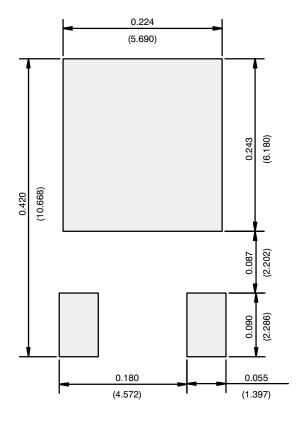
### DWG: 6019

Note

• Dimension L3 is for reference only.



### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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