

Overview

The purpose of this notification is to advise customers of an additional requirement for the Zynq-7000 All Programmable SoC during the processor system (PS) power-off sequence to ensure PS eFUSE integrity.

Description

The Zynq-7000 AP SoC requires the PS_POR_B input to be asserted to GND during the PS power-on sequence until V_{CCPINT} , V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels.

In addition, the Zynq-7000 AP SoC requires at least one of the four following *conditions* during the PS power-off sequence before V_{CCPINT} reaches 0.80V:

- the PS_POR_B input is asserted to GND, or
- the reference clock to the PS_CLK input is disabled, or
- V_{CCPAUX} is lower than 0.70V, or
- V_{CCO_MIO0} is lower than 0.90V.

The above *condition(s)* must be held through the PS power-off sequence until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

If a design does not meet these PS power-on and power-off requirements, then the PS eFUSE integrity can be affected and the resulting symptoms can include the following:

- Failure to boot due to unintended enable of RSA authentication or incorrect RSA PPK hash value,
- Longer than expected boot times due to unintended enable of OCM ROM 128KB CRC check,
- Error during PS eFUSE programming due to unintended write-protect setting or blank check error.

For additional information, see the Recommendations section and Additional Documentation section.

Products Affected

This change affects all Zynq-7000 AP SoCs including Commercial/Industrial (XC), Automotive (XA), Defense-grade (XQ), and all associated specification control document (SCD) devices.

Traceability

[Figure 1](#) shows an example device top mark for the Zynq-7000 AP SoCs which includes the “ZYNQ” family label and a device type that begins with “XC7Z”, “XA7Z”, or “XQ7Z”.

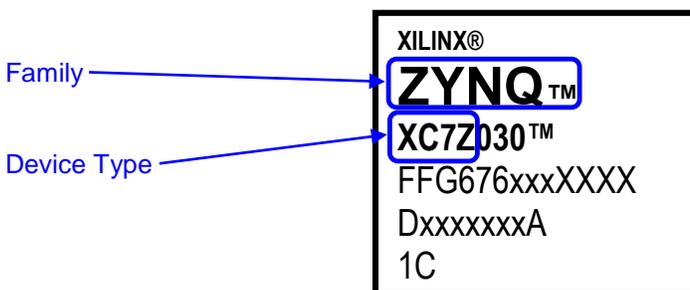


Figure 1: Example Device Top Mark

Recommendations

Xilinx recommends reviewing board designs for the Zynq-7000 AP SoC. All new designs must meet the PS power-on and power-off power supply sequencing requirements that are specified in the data sheets to ensure PS eFUSE integrity. Existing designs should be reviewed against the solutions described in [Answer Record 65240](#). Links to the data sheets and Answer Record 65240 are available in the Additional Documentation section, below.

Response

No response is required. For additional information or questions, please contact [Xilinx Technical Support](#).

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Additional Documentation

Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics Data Sheet (DS187), v1.16 or later:

http://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf

Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100): DC and AC Switching Characteristics Data Sheet (DS191), v1.16 or later:

http://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

Answer Record 65240: <http://www.xilinx.com/support/answers/65240.htm>

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/28/2015	1.0	Initial release.

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