MAX20077/MAX25277 36V, 2.5A Mini Buck Converters with 3.5µA I_Q

General Description

The MAX20077/MAX25277 is a small, synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver up to 2.5A (2.0A for the MAX20077ATCC/VY+ variant) with 3.5V to 36V input voltages while using only 3.5µA quiescent current at no load.

The device provides an accurate output voltage of ±2% in FPWM mode within the normal 6V to 18V operation input range. With 20ns minimum on-time capability, the converter is capable of large input-to-output conversion ratios. Voltage quality can be monitored by observing the PGOOD signal. The device can operate in dropout by running at 99% duty cycle, making it ideal for automotive and industrial applications. The device offers two fixed 5V and 3.3V output voltages. In addition, the device can be configured for 1V to 10V output voltages using an external resistor-divider. Frequency is internally fixed at 2.1MHz, which allows for small external components and reduced output ripple, and guarantees no AM interference. A 400kHz option is also offered to provide minimum switching losses and maximum efficiency. The device automatically enters skip mode at light loads with ultra-low 3.5µA quiescent current at no load. The device offers pin-enabled spread-spectrum-frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX20077/MAX25277 variants are available in a small (3mm x 3mm), 12-pin, side-wettable TDFN package with an exposed pad, and requires very few external components.

Applications

- Automotive
- Industrial
- High-Voltage DC-DC Converters

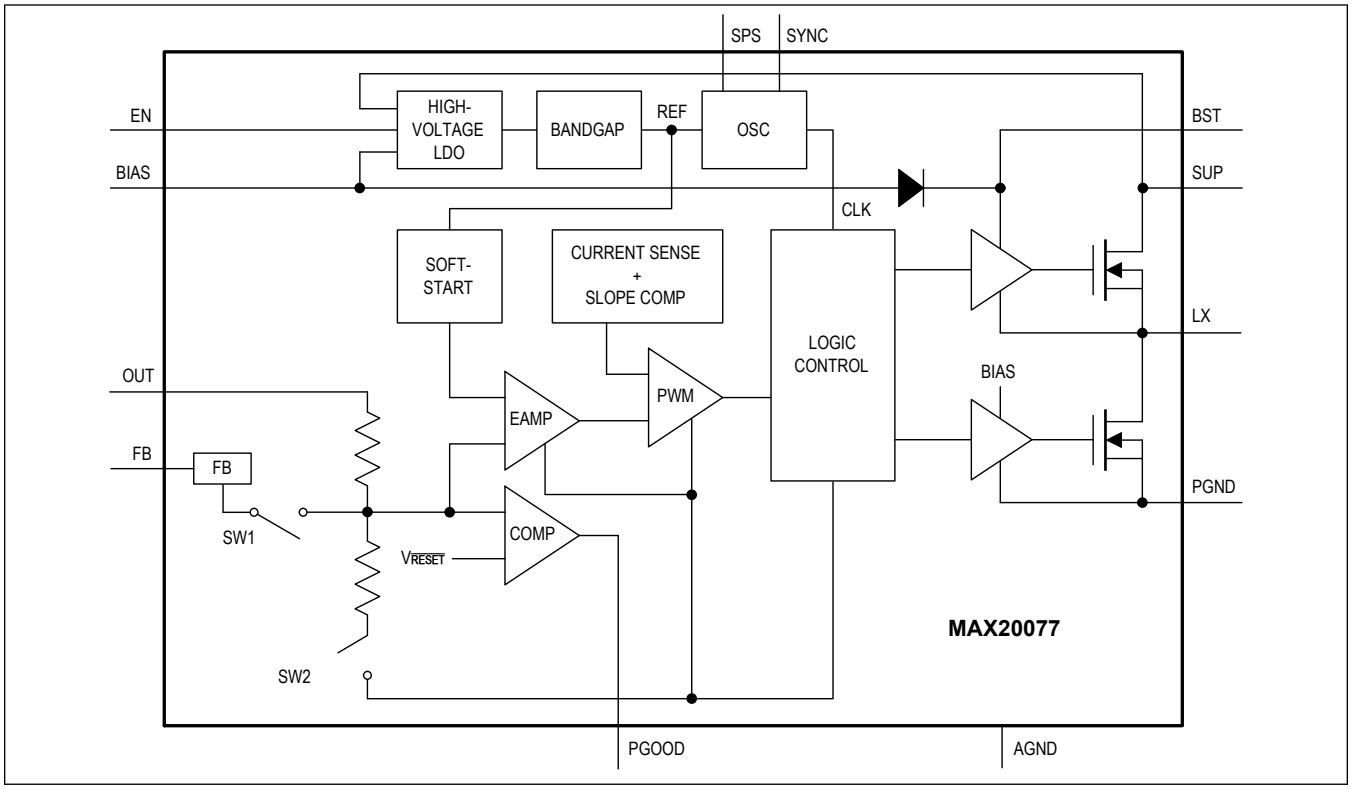
Benefits and Features

- Synchronous DC-DC Converter with Integrated FETs
  - MAX20077ATCA/VY+/B/D/E = 2.5A I_{OUT}
  - MAX20077ATCC/VY+ = 2.0A I_{OUT}
  - 3.5µA Quiescent Current in Standby Mode
- Small Solution Size Saves Space
  - 20ns Minimum On-Time
  - 2.1MHz or 400kHz Operating Frequency
  - Programmable 1V to 10V Output
  - Voltages, or Fixed 5V/3.3V Options Available
  - Fixed 3.5ms Internal Soft-Start
  - Fixed Output Voltage with ±2% Output Accuracy
  - in FPWM Mode (5V/3.3V), or Externally Resistor Adjustable (1V to 10V) with ±1.5% FB Accuracy
  - Innovative Current-Mode-Control Architecture Minimizes Total Board Space and BOM Count
- PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
- Protection Features and Operating Range Ideal for Automotive Applications
  - 3.5V to 36V Operating VIN Range
  - 40V Load-Dump Protection
  - 99% Duty-Cycle Operation with Low Dropout
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

***Ordering Information** appears at end of data sheet.*

19-100267; Rev 7; 8/22

Simplified Block Diagram



Absolute Maximum Ratings

SUP ..... -0.3V to +40V
EN..... -0.3V to +40V
BST to LX (Note 1) ..... +6V
BST..... -0.3V to +45V
FB ..... -0.3V to V_{BIAS} + 0.3V
SYNC..... -0.3V to V_{BIAS} + 0.3V
SPS ..... -0.3V to V_{BIAS} + 0.3V
OUT ..... -0.3V to +18V
PGOOD ..... -0.3V to +6V
PGND to AGND..... -0.3V to +0.3V
BIAS ..... -0.3V to +6.0V
LX Continuous RMS Current..... 3A
OUT Short-Circuit Duration..... Continuous
ESD Protection
Human Body Model..... ±2kV
Machine Model ..... ±200V
Continuous Power Dissipation (T_A = +70°C)
12-pin SWTDFN .....
(derate 24.4mW/°C above +70°C) 1951mW
Storage Temperature Range ..... -65ºC to +150ºC
Operating Junction Temperature (Note 6) ..... -40ºC to +150ºC
Lead Temperature (Soldering, 10s)..... +300ºC
Soldering Temperature (Reflow)..... +260ºC

Note 1: LX has internal clamp diodes to PGND/AGND and SUP. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40°C to +125°C	

Note: These limits are not guaranteed.

Package Information

12 SWTDFN

Package Code	TD1233Y+2C
Outline Number	21-100176
Land Pattern Number	90-100072

12 SWTDFN

Package Code	TD1233Y+3C
Outline Number	21-100284
Land Pattern Number	90-100072
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN}, VSUP = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}			3.5		36	V
		t < 1s				40	
		MAX25277, after startup (Note 3)		3.0		36	
Supply Current	I_{SUP}	V_{EN} = low			1	5	µA
		MAX20077ATCB/VY+, MAX20077ATCE/VY+, MAX20077ATCB2/VY+, MAX20077ATCE2/VY+	No load, no switching		3.5	8	
			No load (Note 4)		4.5		
		MAX20077ATCA/VY+, MAX20077ATCD/VY+, MAX20077ATCD2/VY+	No load, no switching		6	10	
			No load (Note 4)		7.5		
LX Leakage	$I_{LX,LEAK}$	V_{SUP} = 40V, LX = 0 or 40V, T_A = +25°C		-1		+1	µA
Undervoltage Lockout	UVLO	V_{BIAS} rising		2.53	2.73	2.93	V
		Hysteresis			0.13		
BIAS Voltage	V_{BIAS}	5.5V ≤ V_{SUP} ≤ 36V, PWM mode			5		V
BUCK CONVERTER							
Voltage Accuracy, 5V	V_{OUT}, 5.147V	MAX25277ATCA/VY+ (Note 3)	Skip mode (Note 4)	4.994	5.147	5.250	V
			Fixed-frequency PWM Mode	5.070	5.147	5.224	
	V_{OUT},5V	MAX20077ATCA/VY+, MAX20077ATCD/VY+, MAX20077ATCD2/VY+	Skip mode (Note 4)	4.85	4.99	5.1	
	V_{OUT},5V		Fixed-frequency PWM mode	4.93	5	5.07	
Voltage Accuracy, 3.3V	V_{OUT}, 3.395V	MAX25277ATCB/VY+ (Note 3)	Skip mode (Note 4)	3.293	3.395	3.467	V
			Fixed-frequency PWM mode	3.344	3.395	3.446	
	V_{OUT},3.3V	MAX20077ATCB/VY+, MAX20077ATCB2/VY+ MAX20077ATCE/VY+, MAX20077ATCE2/VY+	Skip mode (Note 4)	3.2	3.3	3.37	
	V_{OUT},3.3V		Fixed-frequency PWM mode	3.25	3.3	3.35	

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, VSUP = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Voltage Range with External Configuration	V_{OUT}	MAX20077ATCC/VY+	1		3	V
		MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCB2/VY+, MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+	3		10	
FB Voltage Accuracy	V_{FB}		0.985	1	1.015	V
FB Current	I_{FB}	V_{FB} = 1V, T_A = +25°C		0.02		µA
FB Line Regulation		V_{SUP} = 6V to 36V		0.02		%/V
High-Side Switch On-Resistance	$R_{ON,HS}$	V_{BIAS} = 5V, I_{LX} = 1A		70	125	mΩ
Low-Side Switch On-Resistance	$R_{ON,LS}$	V_{BIAS} = 5V, I_{LX} = 1A		70	125	mΩ
High-Side Current-Limit Threshold	I_{LIM}	MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCD/VY+, MAX20077ATCE/VY+	3.05	3.50	3.95	A
		MAX20077ATCC/VY+	2.55	2.90	3.25	
		MAX20077ATCE2/VY+, MAX20077ATCB2/VY+ MAX20077ATCD2/VY+	4.10	4.70	5.30	
Low-Side Negative Current-Limit Threshold	I_{NEG}			-1.2		A
Soft-Start Ramp Time (Note 5)	I_{SS}	MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCC/VY+, MAX20077ATCB2/VY+		3.5	5	ms
		MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+		5.5	7.5	
Minimum On-Time	t_{ON}	MAX20077ATCC/VY+			20	ns
		MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCB2/VY+, MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+		65	80	
Maximum Duty Cycle		MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCB2/VY+, MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+	98	99		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, VSUP = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}	MAX20077ATCA/VY+, MAX20077ATCB/VY+, MAX20077ATCB2/VY+, MAX20077ATCC/VY+		1.925	2.1	2.275	MHz
		MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+		360	400	440	kHz
Spread-Spectrum Range	SS	V_{SPS} = 5V			±3		%
PGOOD							
PGOOD Threshold, Rising	$V_{THR,PGD}$	V_{OUT} rising		91	93	95	%
PGOOD Threshold, Falling	$V_{THF,PGD}$	V_{OUT} falling		90	92	94	%
PGOOD Debounce Time	t_{DEB}	MAX20077ATCA/VY+, MAX20077ATCB2/VY+ MAX20077ATCB/VY+, MAX20077ATCC/VY+	PWM mode		60		µs
			Skip mode		90		
		MAX20077ATCD/VY+, MAX20077ATCE/VY+, MAX20077ATCD2/VY+, MAX20077ATCE2/VY+	PWM mode		80		
			Skip mode		110		
PGOOD High-Leakage Current	$I_{LEAK,PGD}$	T_A = +25°C				1	µA
PGOOD Low Level	$V_{OUT,PGD}$	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN Level, High	$V_{IH,EN}$			2.4			V
EN Level, Low	$V_{IL,EN}$					0.6	
EN Input Current	$I_{IN,EN}$	V_{EN} = V_{SUP} = 14V, T_A = +25°C				1	µA
External Input Clock Frequency	FSYNC	MAX20077ATCA/VY+, MAX20077ATCB2/VY+		1.7		2.6	MHz
		MAX20077ATCB/VY+		1.7		2.6	
		MAX20077ATCC/VY+		2.35		2.6	
		MAX20077ATCD/VY+, MAX20077ATCD2/VY+, MAX20077ATCE/VY+, MAX20077ATCE2/VY+		325		500	kHz
SYNC Threshold, High	$V_{IH,SYNC}$			1.4			V
SYNC Threshold, Low	$V_{IL,SYNC}$					0.4	V

Electrical Characteristics (continued)

(V_{SUP} = V_{EN}, VSUP = 14V, V_{SYNC} = 0V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Internal Pulldown	$R_{PD,MODE}$			1000		kΩ
SPS Threshold, High	$V_{IH,SPS}$		1.4			V
SPS Threshold, Low	$V_{IL,SPS}$				0.4	V
SPS Internal Pulldown				1000		kΩ
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	(Note 4)		175		°C
Thermal-Shutdown Hysteresis	$T_{SHDN.HYS}$	(Note 4)		15		°C

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 3: V_{OUT} and V_{SUP} are the only electrical characteristics that differentiate the MAX25277 from MAX20077.

Note 4: Guaranteed by design; not production tested.

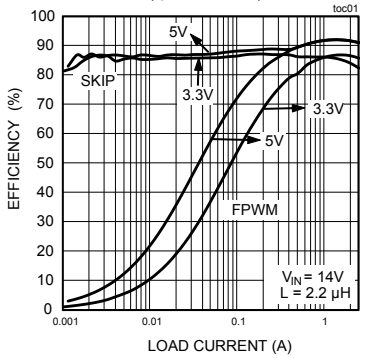
Note 5: Soft-start time is measured as the time taken from EN going high to PGOOD going high.

Note 6: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

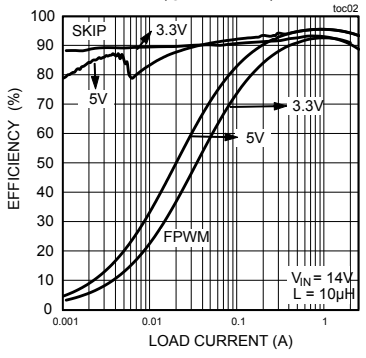
Typical Operating Characteristics

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

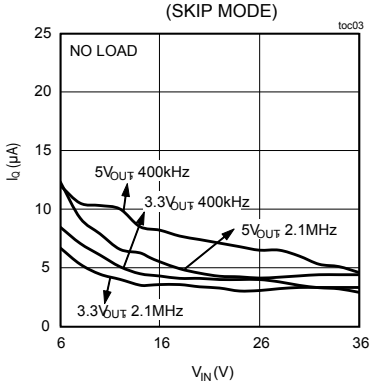
EFFICIENCY vs. LOAD
(f_{SW}= 2.1MHz)



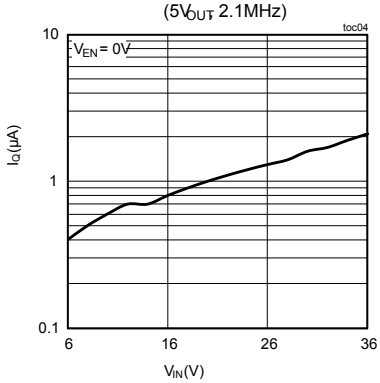
EFFICIENCY vs. LOAD
(f_{SW}= 400kHz)



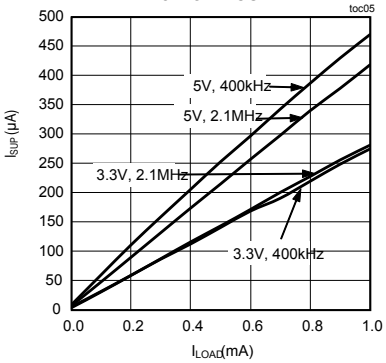
QUIESCENT SUPPLY CURRENT
vs. INPUT VOLTAGE
(SKIP MODE)



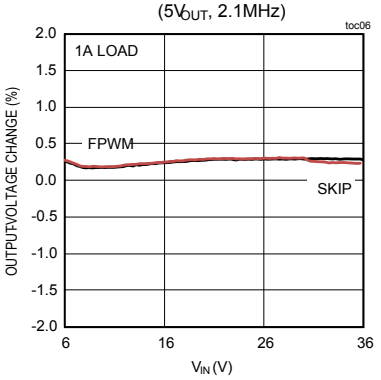
SHUTDOWN SUPPLY CURRENT
vs. INPUT VOLTAGE
(5V_{OUT}, 2.1MHz)



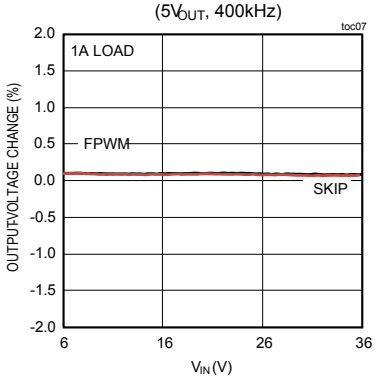
STANDBY CURRENT
vs. LOAD CURRENT



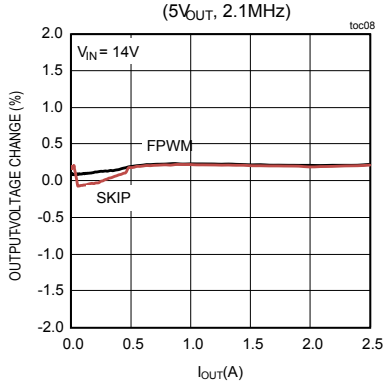
LINE REGULATION
(5V_{OUT}, 2.1MHz)



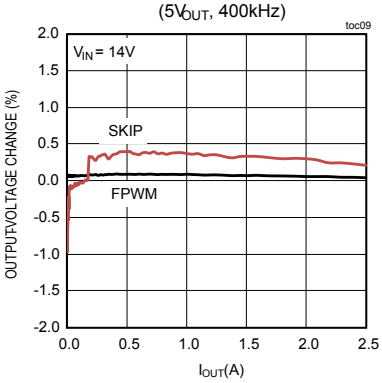
LINE REGULATION
(5V_{OUT}, 400kHz)



LOAD REGULATION
(5V_{OUT}, 2.1MHz)



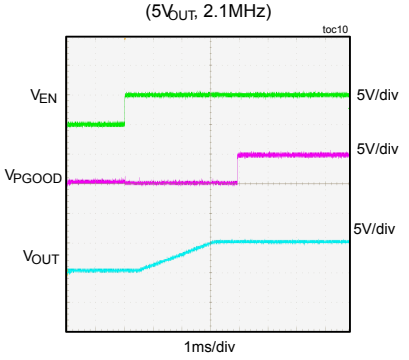
LOAD REGULATION
(5V_{OUT}, 400kHz)



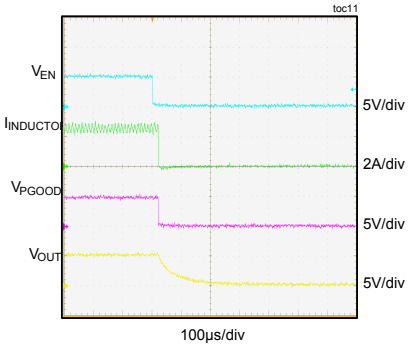
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

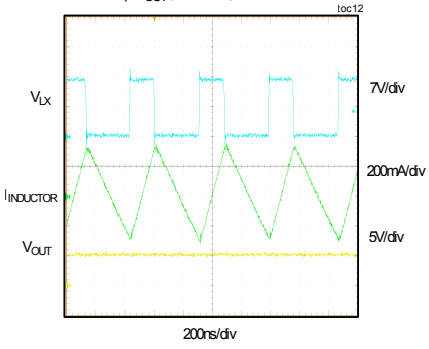
STARTUP WAVEFORM
($5V_{OUT}$, 2.1MHz)



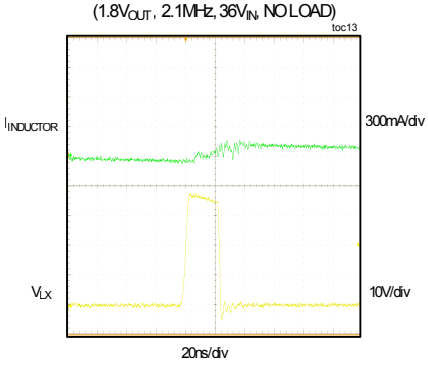
SHUTDOWN WAVEFORM
($5V_{OUT}$, 2.1MHz, 2.5A LOAD)



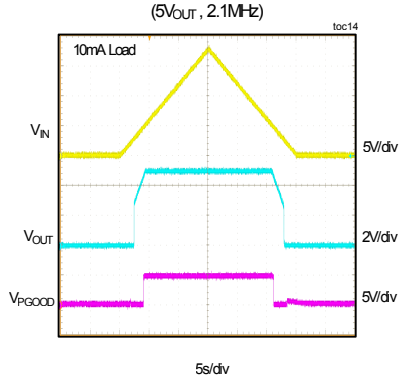
STEADY-STATE SWITCHING WAVEFORM
($5V_{OUT}$, 2.1MHz, NO LOAD



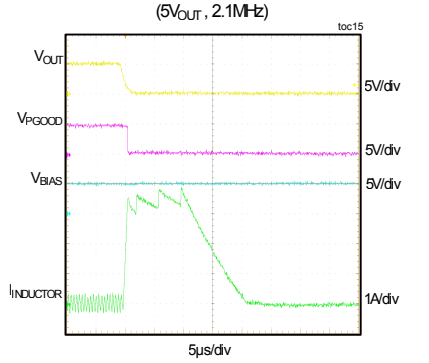
MINIMUM ON-TIME
($1.8V_{OUT}$, 2.1MHz, $36V_{IN}$, NO LOAD)



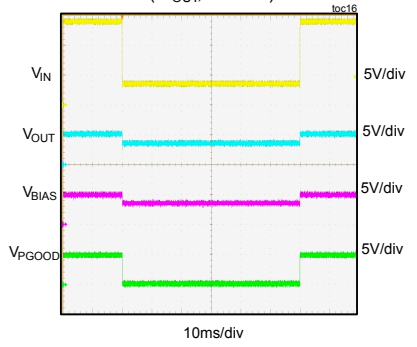
SLOW V_{IN} RAMP
($5V_{OUT}$, 2.1MHz)



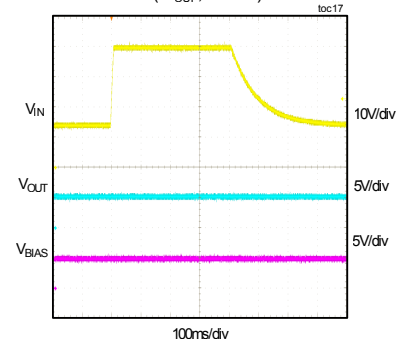
SHORT-CIRCUIT RESPONSE
($5V_{OUT}$, 2.1MHz)



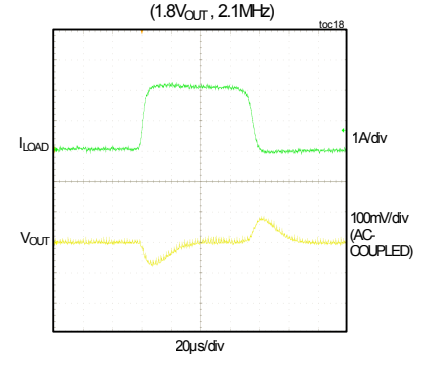
UNDERVOLTAGE PULSE
($5V_{OUT}$, 2.1MHz)



LOAD-DUMP TEST
($5V_{OUT}$, 2.1MHz)



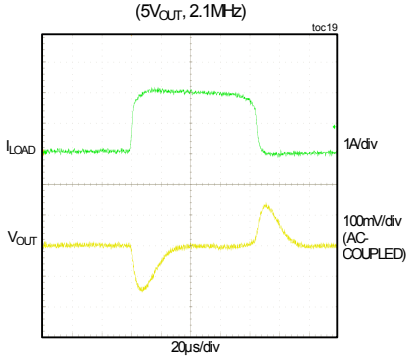
LOAD-TRANSIENT RESPONSE
($1.8V_{OUT}$, 2.1MHz)



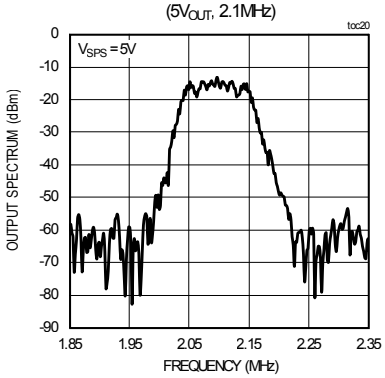
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

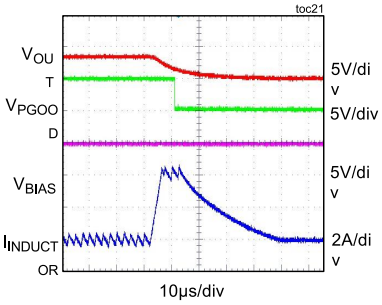
LOAD-TRANSIENT RESPONSE
($5V_{OUT}$, 2.1MHz)



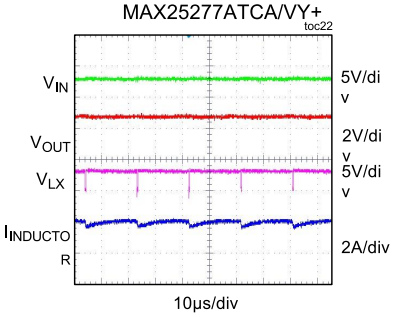
SPECTRAL-ENERGY DENSITY
vs. FREQUENCY
($5V_{OUT}$, 2.1MHz)



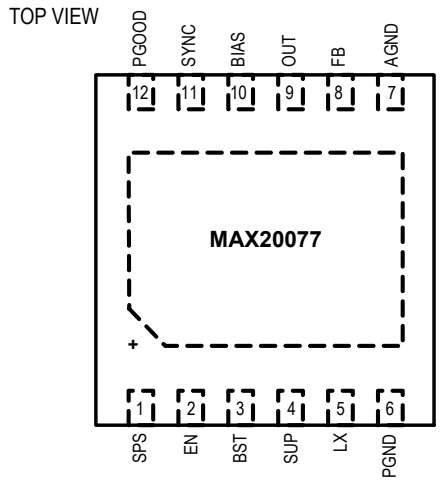
SHORT-CIRCUIT RESPONSE
($3.3V_{OUT}$, 400kHz)
MAX20077ATCE2/VY+



STEADY-STATE SWITCHING WAVEFORM
MAX25277ATCA/VY+



Pin Configuration



SWTDFN
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	SPS	Spread-Spectrum Enable. Connect logic-high to enable spread spectrum of internal oscillator, or logic-low to disable spread spectrum. This pin has a 1MΩ internal pulldown.
2	EN	High-Voltage-Compatible Enable Input. If this pin is low, the part is off.
3	BST	Bootstrap Pin for HS Driver. It is recommended to use 0.1µF from BST to LX.
4	SUP	Supply Input. Connect a 4.7µF ceramic capacitor from SUP to PGND.
5	LX	Buck Switching Node. Connect inductor between LX and OUT. See the *Inductor Selection* section. If the part is off, this node is high impedance.
6	PGND	Power Ground. Ground return path for all high-current/high-frequency noisy signals.
7	AGND	Analog Ground. Ground return path for all ‘quiet’ signals.
8	FB	Feedback Pin. Connect a resistor-divider from OUT to FB to ground for external adjustment of the output voltage. Connect FB to BIAS for internal fixed voltages.
9	OUT	Buck Regulator Output-Voltage-Sense Input. Bypass OUT to PGND with ceramic capacitors.
10	BIAS	5V Internal Bias Supply. Connect a 1µF (min) ceramic capacitor to AGND.
11	SYNC	Sync Input. If connected to ground or open, skip-mode operation is enabled under light loads; if connected to BIAS, forced-PWM mode is enabled. This pin has a 1MΩ internal pulldown.
12	PGOOD	Open-Drain Reset Output. External pullup required.
-	EP	Exposed Pad. EP must be connected to ground plane on PCB, but is not a current-carrying path and is only needed for thermal transfer.

Detailed Description

The MAX20077/MAX25277 family of small, current-mode-controlled buck converters features synchronous rectification and requires no external compensation network. The devices are designed for 2.5A output current (2A for MAX20077ATCC/VY+) and can stay in dropout by running at 99% duty cycle. Each device provides an accurate output voltage of ±2% in FPWM mode within the 6V to 18V input range. With 20ns minimum on-time, the devices can regulate < 3V output voltages directly off the car battery. This eliminates the need for traditional two-stage designs for voltage rails < 3V. Voltage quality can be monitored by observing the PGOOD signal. The devices operate at 2.1MHz (typ) frequency, which allows for small external components, reduced output ripple, and guarantees no AM band interference. The devices are also available at 400kHz (typ) for minimum switching losses and maximum efficiency.

Each device features an ultra-low 3.5µA (typ) quiescent supply current in standby mode. The device enters standby mode automatically at light loads if the high-side FET (HSFET) does not turn on for eight consecutive clock cycles. The devices operate from a 3.5V to 36V supply voltage and can tolerate transients up to 40V, making them ideal for automotive applications. The devices are available in factory-trimmed output voltages (5V, 3.3V) and are programmable with an external resistor-divider. For fixed output voltages outside of 3.3V and 5V, contact factory for availability.

Enable Input (EN)

Each device is activated by driving EN high. EN is compatible from a 3.3V logic level to automotive battery levels. EN can be controlled by microcontrollers and automotive KEY or CAN inhibit signals. The EN input has no internal pullup/pulldown current to minimize the overall quiescent supply current. To realize a programmable undervoltage-lockout level, use a resistor-divider from SUP to EN to AGND.

Bias/UVLO

Each device features undervoltage lockout. When the device is enabled, an internal bias generator turns on. LX begins switching after V_{BIAS} has exceeded the internal undervoltage-lockout level, V_{UVLO} = 2.73V (typ).

Soft-Start

Each device features an internal soft-start timer. The output voltage soft-start time is 3.5ms (typ), which includes the delay in PGOOD. If a short circuit or undervoltage is encountered after the soft-start time has expired, the device is disabled for 7ms (typ) and then reattempts soft-start again. This pattern repeats until the short circuit has been removed.

Oscillator/Synchronization and Efficiency (SYNC)

Each device has an on-chip oscillator that provides a 2.1MHz (typ) or 400kHz (typ) switching frequency. Depending on the condition of SYNC, two operation modes exist. If SYNC is unconnected or at AGND, the device operates in highly efficient pulse-skipping mode. If SYNC is connected to BIAS or has a clock applied to it, the device is in forced PWM mode (FPWM). The device can be switched during operation between FPWM mode and skip mode by switching SYNC.

Skip-Mode Operation

Skip mode is entered when the SYNC pin is connected to ground or is unconnected and the peak load current is < 600mA (typ). In this mode, the HSFET is turned on until the inductor current ramps up to 100mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1.0V, typ). At this point, both the HSFETs and low-side FETs (LSFETs) are turned off. Depending on the choice of the output capacitor and the load current, the HSFET turns on when OUT (valley) drops below the 1.0V (typ) feedback voltage.

Achieving High Efficiency at Light Loads

Each device operates with very low-quiescent current at light loads to enhance efficiency and conserve battery life. When the device enters skip mode, the output current is monitored to adjust the quiescent current. The lowest quiescent-current standby mode is only available for factory-trimmed devices between 3.0V and 5.5V output voltages. When the output current is < ~5mA, the device operates in the lowest quiescent-current mode, also called standby mode. In this mode, the majority of the internal circuitry (excluding that necessary to maintain regulation) in the device is turned off to save current. Under no load and with skip mode enabled, the device typically draws 3.5µA for the 3.3V parts, and 6µA for the 5.0V parts. For load currents > 5mA, the device enters normal skip mode and still maintains very high efficiency.

Output-Voltage Overshoot Protection

In dropout, the output voltage closely follows the input voltage, but is below the regulation point. The device runs at maximum duty cycle to satisfy the loop, and the internal error-amplifier output is railed high. When the input voltage rises above the output, the device comes out of dropout, but the internal error-amplifier output takes some time to get back to steady state. This causes an overshoot in the output voltage. To limit this overshoot, the device clamps the output of the error amplifier while coming out of dropout, causing it to discharge faster and limiting the output-voltage overshoot. The actual value of the overshoot depends on the output capacitor, inductor, and load.

Controlled EMI with Forced-Fixed Frequency

In FPWM mode, the device attempts to operate at a constant switching frequency for all load currents. For tightest frequency control, apply the operating frequency to SYNC. The advantage of FPWM is a constant switching frequency, which improves EMI performance; the disadvantage is that considerable current can be thrown away. If the load current during a switching cycle is less than the current flowing through the inductor, the excess current is diverted to AGND.

Extended Input Voltage Range

In some cases, the device is forced to deviate from its operating frequency, independent of the state of SYNC. For input voltages above 18V (for MAX20077ATCB/VY+), the required duty cycle to regulate its output may be smaller than the minimum on-time (65ns, typ). In this event, the device is forced to lower its switching frequency by skipping pulses. If the output voltage being regulated is < 3V, then the MAX20077ATCC/VY+ can operate at 2.1MHz without skipping pulses for a larger voltage range of 20ns (typ) minimum on-time. If the input voltage is reduced and the device approaches dropout, it continuously tries to turn on the HSFET. To maintain gate charge on the HSFET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the HSFET is turned off every 20µs and the LSFET is turned on for ~200ns. This gives an effective duty cycle of > 99%, and a switching frequency of 50kHz when in dropout. Since the MAX20077ATCC/VY+ supports voltages of < 3V, it does not support operation with SUP ≤ OUT.

Spread-Spectrum Option

Each device has an optional spread spectrum enabled by the SPS pin. If SPS is pulled high, the internal operating frequency varies by ±3% relative to the internally generated 2.1MHz (typ) operating frequency. Spread spectrum is offered to improve EMI performance of the device. The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the device is running with an internally generated switching frequency.

Power-Good (PGOOD)

Each device features an open-drain power-good output. PGOOD is an active-high output that pulls low when the output voltage is below 92% (typ) of its nominal value. PGOOD is high impedance when the output voltage is above 93% (typ) of its nominal value. Connect a 20kΩ (typ) pullup resistor to an external supply, or to the on-chip BIAS output.

Overcurrent Protection

Each device limits the peak output current to 3.5A (typ) for the MAX20077ATCA/VY+/B/D/E and 2.9A (typ) for the MAX20077ATCC/VY+. The accuracy of the current limit is ±12%, making selection of external components very easy. To protect against short-circuit events, the device shuts off when OUT is below 50% of V_{OUT} (25% of V_{OUT} for the MAX20077ATCC/VY+) and an overcurrent event is detected. The device attempts a soft-start restart every 7ms and stays off if the short circuit has not been removed. When the current limit is no longer present, it reaches the output voltage by following the normal soft-start sequence. If the device's die reaches the thermal limit of 175°C (typ) during the current-limit event, it immediately shuts off.

Thermal-Overload Protection

Each device features thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed +5V/3.3V output voltage. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB to AGND (see Figure 1). Select RFB2 (FB to AGND resistor) ≤ 500kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2} [(V_{OUT}/V_{FB}) - 1)]$$

where VFB = 1V (see the *Electrical Characteristics* table).

Input Capacitor

A 4.7µF low-ESR ceramic input capacitor is recommended for proper device operation. This value can be adjusted based on application input-voltage-ripple requirements.

The discontinuous input current of the buck converter causes large input-ripple current. Switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input-capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input-capacitance requirement.

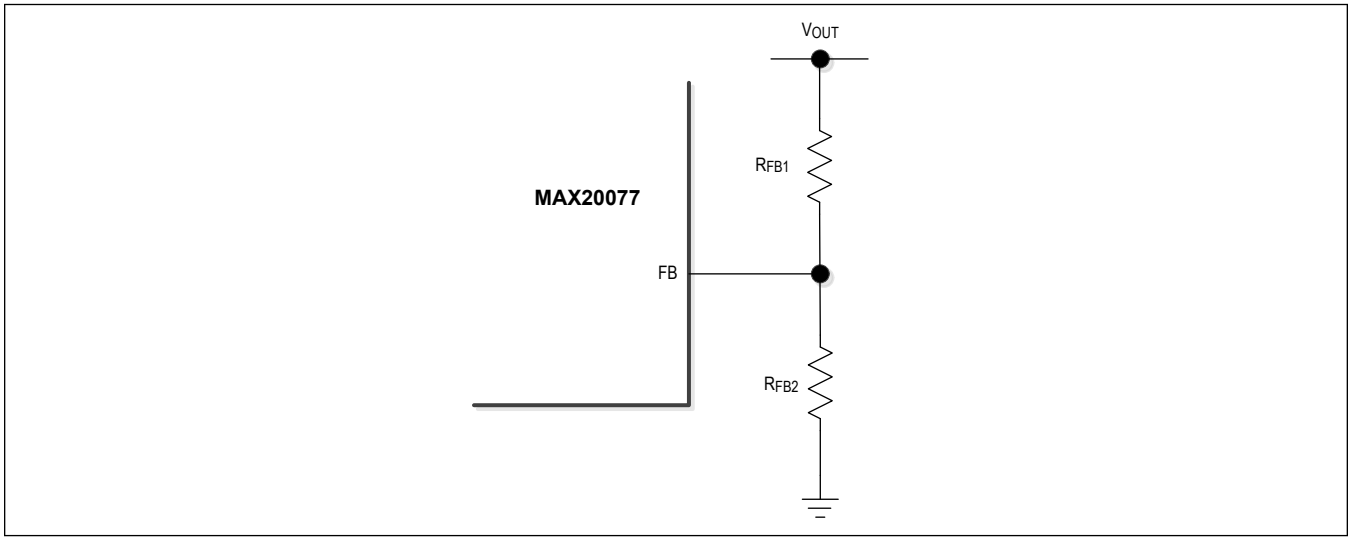


Figure 1. Adjustable Output-Voltage Setting

The input ripple is mainly comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume that input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

Equation 1:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT} + (\Delta I_{P-P}/2)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta VQ \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Inductor Selection

See Table 1 for inductor selection. The nominal standard value selected should be within ±50% of the specified inductance.

Table 1. Inductor Selection

PART	INDUCTANCE (µH)
For fSW = 2.1MHz	2.2
MAX20077ATCC/VY+	4.7
For fSW = 400kHz	10

Table 2. Output-Capacitance Selection

PART	OUTPUT CAPACITANCE (µF)
MAX20077ATCA/VY+/B/B2	30
MAX20077ATCC/VY+/D/E	44
MAX25277ATCA/VY+/B	30

Output Capacitor

For optimal phase margin (> 60 degrees, typ), the recommended output capacitances are shown in Table 2. Recommended values are the actual capacitances after voltage derating is taken into account.

If a lower output capacitance is required, contact the factory for recommendations. Additional output capacitance may be needed based on application-specific output-voltage-ripple requirements. If the total output capacitance is more than 80µF effective, use MAX20077ATCE2/VY+, and for effective output capacitance more than 60µF, use MAX20077ATCD2/VY+ for 400kHz applications. For similar requirements in 2MHz application, contact the factory for an optimized solution.

Note: For MAX20077ATCC, with load less than 1A and input voltage between 6V and 18V, the minimum required effective cap is 24µF.

The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determine the output capacitance and its ESR. The output ripple comprises ΔVQ (caused by the capacitor discharge) and ΔVESR (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔVESR. Use Equation 2 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 2:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 3:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} \geq I_{STEP}^2 \times \frac{L}{2 \times (V_{SUP} - V_{OUT}) \times D_{MAX} \times \Delta V_Q} + I_{STEP} \times \frac{t_{DELAY}}{\Delta V_Q}$$

where I_{STEP} is the load step and t_{DELAY} is the delay for the PWM mode, the worst-case delay would be (1-D) tSW when the load step occurs right after a turn-on cycle. This delay is higher in Skip mode.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1. Place the input capacitor (CIN) close to the device to reduce the input AC-current loop. AC current flows on the loop formed by the input capacitor and the half-bridge MOSFETs internal to the device (see Figure 2). A small loop would reduce the radiating effect of high-switching currents and improve EMI functionality.
2. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer.
3. Connect PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.
4. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
5. Using internal PCB layers as ground plane helps to improve the EMI functionality as ground planes act as a shield against radiated noise. Have multiple vias spread around the board, especially near the ground connections to have better overall ground connection.
6. Keep the bias capacitor (C_{BIAS}) close to the device to reduce the bias current loop. This helps to reduce noise on the bias for smoother operation.

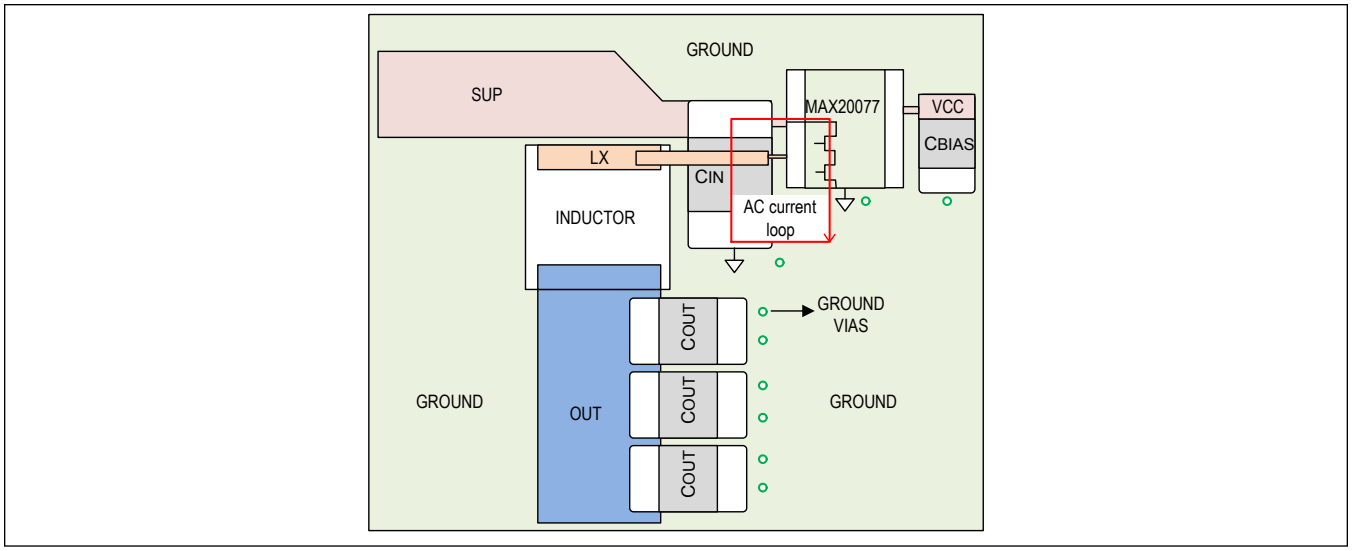
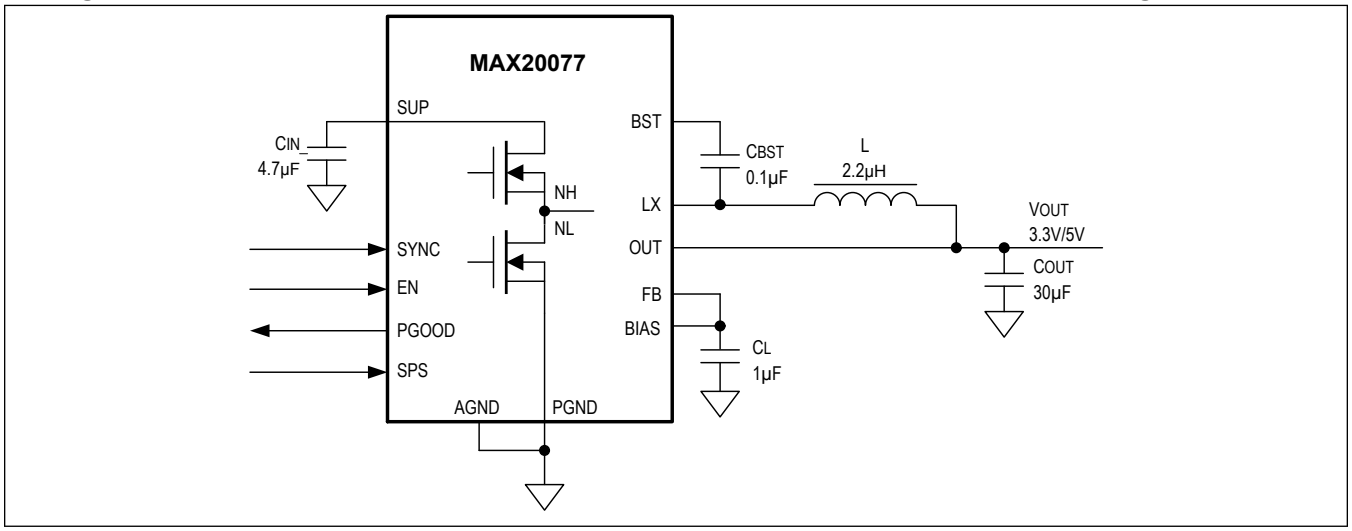


Figure 2. Recommended PCB Layout for the MAX20077/MAX25277

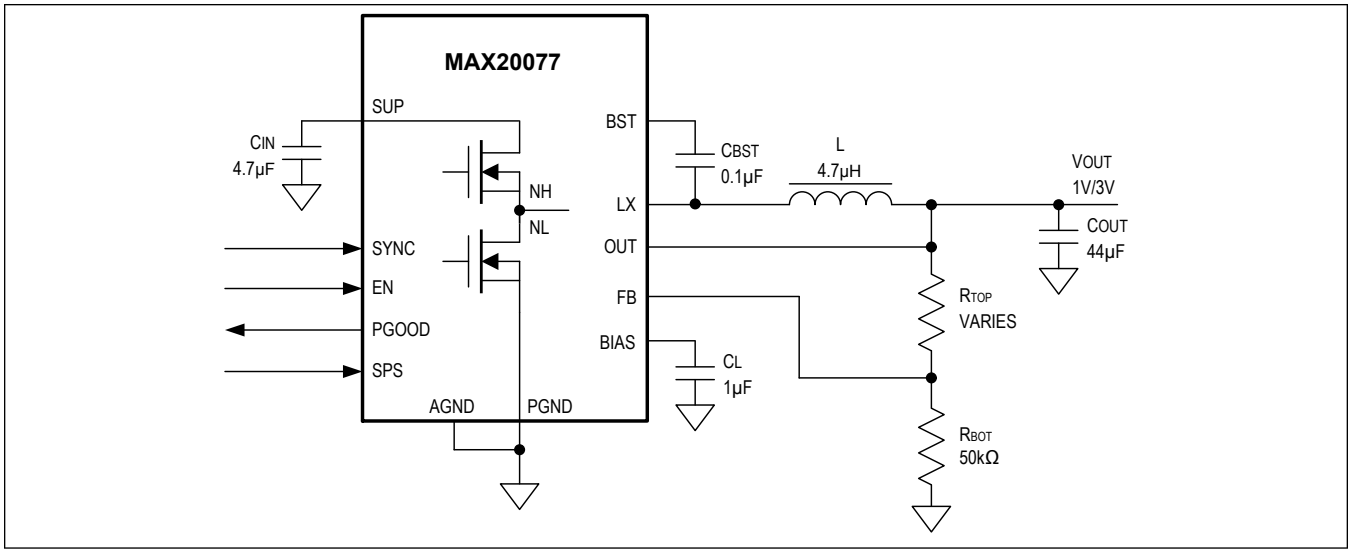
Typical Application Circuits

Configuration: 2.1MHz, 5V/3.3V Fixed Output in 12-Pin Side-Wettable TDFN Package

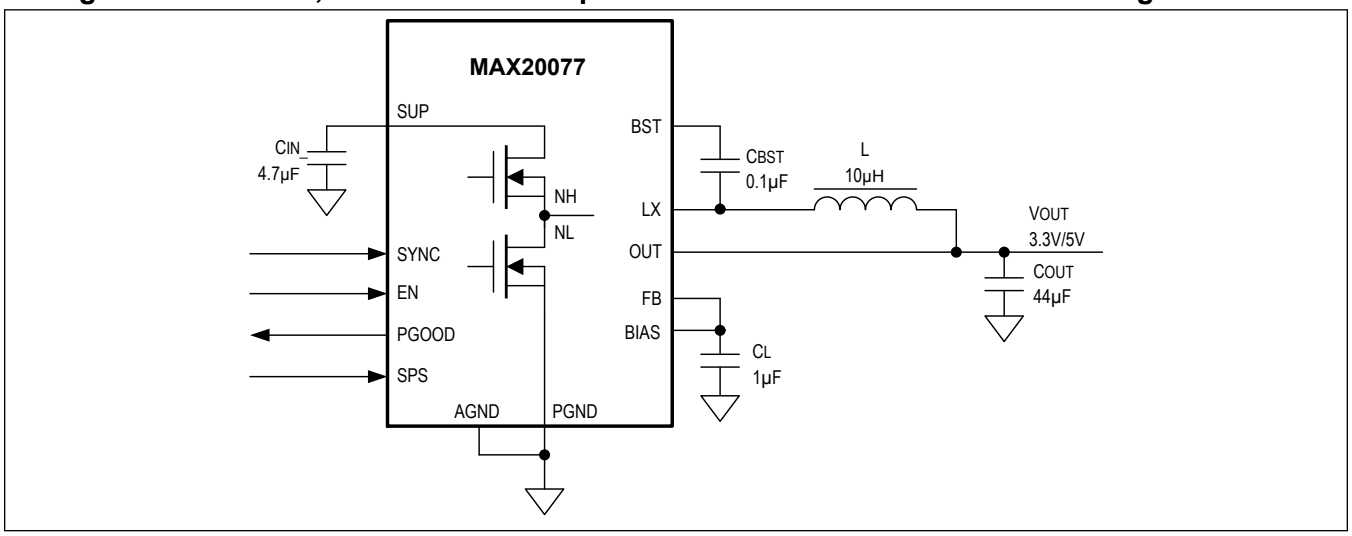


Typical Application Circuits (continued)

MAX20077ATCC/VY+ Configuration: 2.1MHz, 1V-3V Variable Output in 12-Pin Side-Wettable TDFN Package



Configuration: 400kHz, 5V/3.3V Fixed Output in 12-Pin Side-Wettable TDFN Package



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION	IOUT (A)
MAX20077ATCA/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, fixed 5V output or 3V to 10V external resistor-divider	2.5
MAX20077ATCB/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, fixed 3.3V output or 3V to 10V external resistor-divider	2.5
MAX20077ATCB2/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, fixed 3.3V output or 3V to 10V external resistor-divider; higher current limit	2.5
MAX20077ATCC/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, 1V to 3V external resistor-divider	2.0
MAX20077ATCD/VY+	-40°C to +125°C	12 SWTDFN	400kHz, fixed 5V output or 3V to 10V external resistor-divider	2.5
MAX20077ATCD2/VY+	-40°C to +125°C	12 SWTDFN	400kHz, fixed 5V output or 3V to 10V external resistor-divider; optimized for higher output capacitance	2.5
MAX20077ATCE/VY+	-40°C to +125°C	12 SWTDFN	400kHz, fixed 3.3V output or 3V to 10V external resistor-divider	2.5
MAX20077ATCE2/VY+	-40°C to +125°C	12 SWTDFN	400kHz, fixed 3.3V output or 3V to 10V external resistor-divider; optimized for higher output capacitance	2.5
MAX25277ATCA/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, fixed 5.147V output or 3V to 10V external resistor-divider	2.5
MAX25277ATCB/VY+	-40°C to +125°C	12 SWTDFN	2.1MHz, fixed 3.395V output or 3V to 10V external resistor-divider	2.5

Note: *All parts are OTP versions, no metal mask differences.*

/V Denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package. SW = Side-wettable TDFN package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	3/18	Updated *Package Information* and *Electrical Characteristics* tables; updated *Input Capacitor*, *Inductor Selection*, *Output Capacitor*, and *PCB Layout Guidelines* sections; updated *Figure 3* and *Figure 5* captions and added TOC21–TOC22 in the *Typical Operating Characteristics* section	2–4, 7, 11–16
1.5		Corrected typo in the *Ordering Information* table	16
2	5/18	Added the MAX25277 to data sheet title; updated *Absolute Maximum Ratings*; added *Recommended Operating Conditions* section; updated *Electrical Characteristics* table; updated *Detailed Description* and *Output Capacitor* sections, added the MAX20077ATCD2/VY+, removed future product status from MAX20077ATCE2/VY+, and future produc status to MAX25277ATCA/VY+ in the *Ordering Information* table	2–4, 9, 10, 12, 16
3	6/18	Updated LX Continuous RMS Current in *Absolute Maximum Ratings*, removed MAX20077ATCD2/VY+ and MAX200771TCE2/VY+ from High-Side Current-Limit Threshold in *Electrical Characteristics* table, removed future product status from MAX20077ATCE2/VY+ and added future product status to MAX25277 in *Ordering Information* table	2, 3, 17
4	7/18	Updated *General Description*, *Benefits and Features*, and *Detailed Description* sections, updated *Electrical Characteristics* table, updated Table 1 and Table 2, updated Figure 2 caption, added MAX20077ATCB2/VY+ and MAX25277ATCB/VY+ to the *Ordering Information* table	1, 3, 4, 10, 12–14, 17
5	10/18	Removed future-product status from MAX20077ATCB2/VY+, MAX25277ATCA/VY+, and MAX25277ATCB/VY+ in the *Ordering Information* table	17
6	6/19	Updated *General Description*, *Electrical Characteristics*, and *Detailed Description* sections	1, 3, 10
7	8/22	Updated *Detailed Description* and *Applications Information* sections	12, 15