QUAD DIFFERENTIAL PECL DRIVERS

FEATURES

- **Functional Replacements for the Agere BDG1A, BPNGA and BDGLA**
- **Pin-Equivalent to the General-Trade 26LS31 Device**
- **2.0 ns Maximum Propagation Delays**
- **0.15 ns Output Skew Typical Between Pairs**
- **Capable of Driving 50-Ω Loads**
- **5.0-V or 3.3-V Supply Operation**
- **TB5D1M Includes Surge Protection on Differential Outputs**
- **TB5D2H No Line Loading When V_{CC} = 0**
- **Third State Output Capability**
- **-40C to 85C Operating Temp Range**
- **ESD Protection HBM > 3 kV and CDM > 2 kV**
- **Available in Gull-Wing SOIC (JEDEC MS-013, DW) and SOIC (D) Packages**

APPLICATIONS

- **Digital Data or Clock Transmission Over Balanced Transmission Lines**

DESCRIPTION

These quad differential drivers are TTL input to pseudo-ECL differential output used for digital data transmission over balanced transmission lines.

The TB5D1M device is a pin and functional replacement for the Agere systems BDG1A and BPNGA quad differential drivers. The TB5D1M has a built-in lightning protection circuit to absorb large transitions on the transmission lines without destroying the device. When the circuit is powered down it loads the transmission line, because of the protection circuit.

The TB5D2H device is a pin and functional replacement for the Agere systems BDG1A and BDGLA quad differential drivers. Upon power down the TB5D2H output circuit appears as an open circuit and does not load the transmission line.

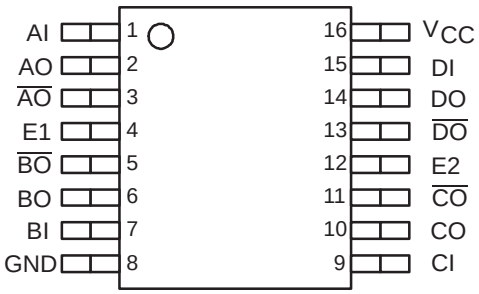
Both drivers feature a 3-state output with a third-state level of less than 0.1 V.

The packaging options available for these quad differential line drivers include a 16-pin SOIC gull-wing (DW) and a 16-pin SOIC (D) package.

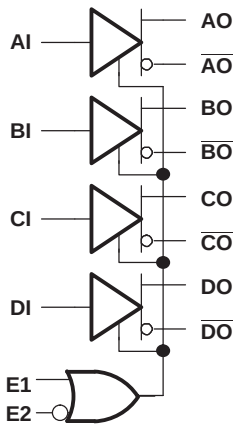
Both drivers are characterized for operation from -40C to 85C

The logic inputs of this device include internal pull-up resistors of approximately 40 kΩ that are connected to V_{CC} to ensure a logical high level input if the inputs are open circuited.

DW AND D PACKAGE
(TOP VIEW)



FUNCTIONAL DIAGRAM



ENABLE TRUTH TABLE

E1	E2	Condition
0	0	Active
1	0	Active
0	1	Disabled
1	1	Active

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH	STATUS
TB5D1MDW	TB5D1M	Gull-wing SOIC	NiPdAu	Production
TB5D1MD	TB5D1M	SOIC	NiPdAu	Production
TB5D2HDW	TB5D2H	Gull-wing SOIC	NiPdAu	Production
TB5D2HD	TB5D2H	SOIC	NiPdAu	Production

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \le 25°C$ POWER RATING	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT WITH NO AIR FLOW	DERATING FACTOR(1) ABOVE T_A = 25C	T_A = 85C POWER RATING
D	Low-K(2)	754 mW	132.6 C/W	7.54 mW/C	301 mW
	High-K(3)	1166 mW	85.8 C/W	11.7 mW/C	466 mW
DW	Low-K(2)	816 mW	122.5 C/W	8.17 mW/C	326 mW
	High-K(3)	1206 mW	82.9 C/W	12.1 mW/C	482 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the high-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNITS
θ_{JB}	Junction-to-board thermal resistance	D	51.4	C/W
		DW	56.6	C/W
θ_{JC}	Junction-to-case thermal resistance	D	45.7	C/W
		DW	49.2	C/W

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TB5D1M, TB5D2H
Supply voltage, V_{CC}			0 V to 6 V
Input voltage			- 0.3 V to (V_{CC} + 0.3 V)
ESD	Human Body Model(2)	All Pins	3 kV
	Charged-Device Model(3)	All Pins	2 kV
Continuous power dissipation			See Dissipation Rating Table
Storage temperature, T_{stg}			-65C to 130C
Junction temperature, T_J			130C
Lightning surge, TB5D1M only, see Figure 6		D Package	-80 V to 100 V
		DW Package	-100 V to 100 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	5.0-V nominal supply	4.5	5	5.5	V
	3.3-V nominal supply	3.0	3.3	3.6	V
Operating free-air temperature, T_A		-40		85	C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet, unless otherwise stated.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

parameter		test conditions	min	typ(1)	max	unit
I_{CC}	Supply current	V_{CC} = 4.5 V to 5.5 V, no loads			40	mA
		V_{CC} = 3.0 V to 3.6 V, no loads			40	
P_D	Power dissipation	V_{CC} = 4.5 V to 5.5 V, Figure 3 loads all outputs		290	360	mW
		V_{CC} = 3.0 V to 3.6 V, Figure 4 loads all outputs		280	360	
V_{OH}	Output high voltage	V_{CC} = 4.5 V to 5.5 V, Figure 3	V_{CC} - 1.8	V_{CC} - 1.3	V_{CC} - 0.8	V
V_{OL}	Output low voltage		V_{OH} - 1.4	V_{OH} - 1.2	V_{OH} - 0.7	V
V_{OD}	Differential output voltage $\|V_{OH} - V_{OL}\|$		0.7	1.2	1.4	V
V_{OH}	Output high voltage	V_{CC} = 3.0 V to 3.6 V, Figure 4	V_{CC} - 1.8	V_{CC} - 1.3	V_{CC} - 0.8	V
V_{OL}	Output low voltage		V_{OH} - 1.4	V_{OH} - 1.1	V_{OH} - 0.5	V
V_{OD}	Differential output voltage $\|V_{OH} - V_{OL}\|$		0.5	1.1	1.4	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	C_L= 5 pF, Figure 5		230	600	mV
V_{OZ}	Third-state output voltage	Figure 3 or Figure 4 load			0.1	V
V_{IL}	Low level input voltage(2)				0.8	V
V_{IH}	High level input voltage		2			V
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V, I_I = -5 mA			-1(3)	V
I_{OS}	Output short-circuit current(4)	V_{CC} = 5.5 V, V_O = 0 V			-250(3)	mA
		V_{CC} = 5.5 V, V_{OD} = 0 V			10(3)	
I_{IL}	Input low current, enable or data	V_{CC} = 5.5 V, V_I = 0.4 V			-400(3)	A
I_{IH}	Input high current, enable or data	V_{CC} = 5.5 V, V_I =2.7 V			20	A
	Input reverse current, enable or data	V_{CC} = 5.5 V, V_I =5.5 V			100	A
C_{IN}	Input capacitance			5		pF

(1) All typical values are at 25C and with a 3.3-V or 5-V supply.
(2) The input level provides no noise immunity and should be tested only in a static, noise-free environment.
(3) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(4) Test must be performed one output at a time to prevent damage to the device. No test circuit attached.

THIRD STATE—A TB5D1M (or TB5D2H) driver produces pseudo-ECL levels, and has a third-state mode, which is different than a conventional TTL device. When a TB5D1M (or TB5D2H) driver is placed in the third state, the base of the output transistors is pulled low, bringing the outputs below the active-low level of standard PECL devices. [For example: The TB5D1M low output level is typically 2.7 V, while the third state output level is less than 0.1 V.] In a bidirectional, multipoint, bus application, the driver of one device, which is in its third state, may be back driven by another driver on the bus whose voltage in the low state is lower than the third-stated device. This could come about due to differences in the driver's independent power supplies. In this case, the device in the third state controls the line, thus clamping the line and reducing the signal swing. If the difference voltage between the independent driver power supplies is small, this consideration can be ignored. Again using the TB5D1M driver as an example, a typical supply voltage difference between separate drivers of > 2 V can exist without significantly affecting the amplitude of the signal.

SWITCHING CHARACTERISTICS, 5-V NOMINAL SUPPLY

over recommended operating conditions unless otherwise noted

parameter		test conditions	min	typ(1)	max	unit
t_{P1}	Propagation delay time, input high to output(2)	C_L = 5 pF, See Figure 1 and Figure 3		1.2	2	ns
t_{P2}	Propagation delay time, input low to output(2)			1.2	2	
Δt_P	Capacitive delay			0.01	0.03	ns/pF
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	C_L = 5 pF, See Figure 2 and Figure 3		7	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7	12	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			5	12	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			4	12	
t_{skew1}	Output skew, $\lvert t_{P1} - t_{P2} \rvert$	C_L = 5 pF, See Figure 1 and Figure 3		0.15	0.3	ns
t_{shew2}	Output skew, $\lvert t_{PHH} - t_{PHL} \rvert$, $\lvert t_{PLH} - t_{PLL} \rvert$			0.15	1.1	
$t_{skew(pp)}$	Part-to-part skew(3)			0.1	1	
Δt_{skew}	Output skew, difference between drivers(4)				0.3	
t_{TLH}	Rise time (20% - 80%)	C_L = 5 pF, See Figure 1 and Figure 3		0.7	2	ns
t_{THL}	Fall time (80% - 20%)			0.7	2	

(1) All typical values are at 25C and with a 5-V supply.
(2) Parameters t_{P1} and t_{P2} are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 1).
(3) $t_{skew(pp)}$ is the magnitude of the difference in differential propagation delay times, t_{P1} or t_{P2}, between any specified outputs of two devices when both devices operate with the same supply voltage, at the same temperature, and have identical packages and test circuits.
(4) Δt_{skew} is the magnitude of the difference in differential skew t_{skew1} between any specified outputs of a single device.

SWITCHING CHARACTERISTICS, 3.3-V NOMINAL SUPPLY

over recommended operating conditions unless otherwise noted

parameter		test conditions	min	typ(1)	max	unit
t_{P1}	Propagation delay time, input high to output(2)	C_L = 5 pF, See Figure 1 and Figure 4		1.2	3.5	ns
t_{P2}	Propagation delay time, input low to output(2)			1.2	3.5	
Δt_P	Capacitive delay			0.01	0.03	ns/pF
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	C_L = 5 pF, See Figure 2 and Figure 4		8	12	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	12	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			5	12	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	12	
t_{skew1}	Output skew, $\lvert t_{P1} - t_{P2} \rvert$	C_L = 5 pF, See Figure 1 and Figure 4		0.15	0.3	ns
t_{shew2}	Output skew, $\lvert t_{PHH} - t_{PHL} \rvert$, $\lvert t_{PLH} - t_{PLL} \rvert$			0.15	1.2	
$t_{skew(pp)}$	Part-to-part skew(3)			0.1	1	
Δt_{skew}	Output skew, difference between drivers(4)				0.3	
t_{TLH}	Rise time (20% - 80%)	C_L = 5 pF, See Figure 1 and Figure 4		0.7	2	ns
t_{THL}	Fall time (80% - 20%)			0.7	2	

(1) All typical values are at 25C and with a 3.3-V supply.
(2) Parameters t_{P1} and t_{P2} are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 1).
(3) $t_{skew(pp)}$ is the magnitude of the difference in differential propagation delay times, t_{P1} or t_{P2}, between any specified outputs of two devices when both devices operate with the same supply voltage, at the same temperature, and have identical packages and test circuits.
(4) Δt_{skew} is the magnitude of the difference in differential skew t_{skew1} between any specified outputs of a single device.

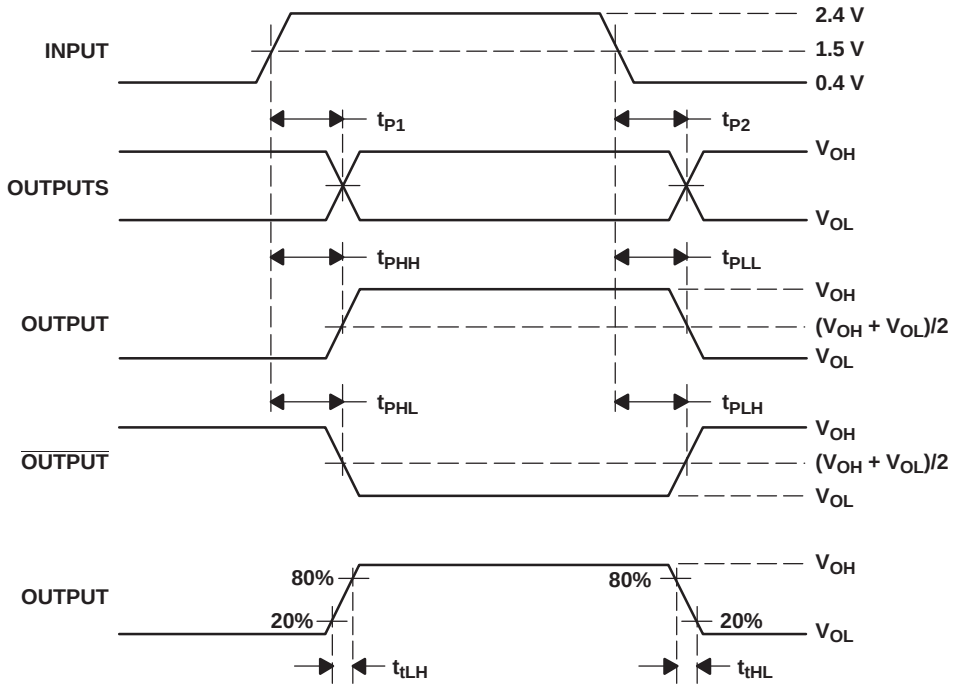
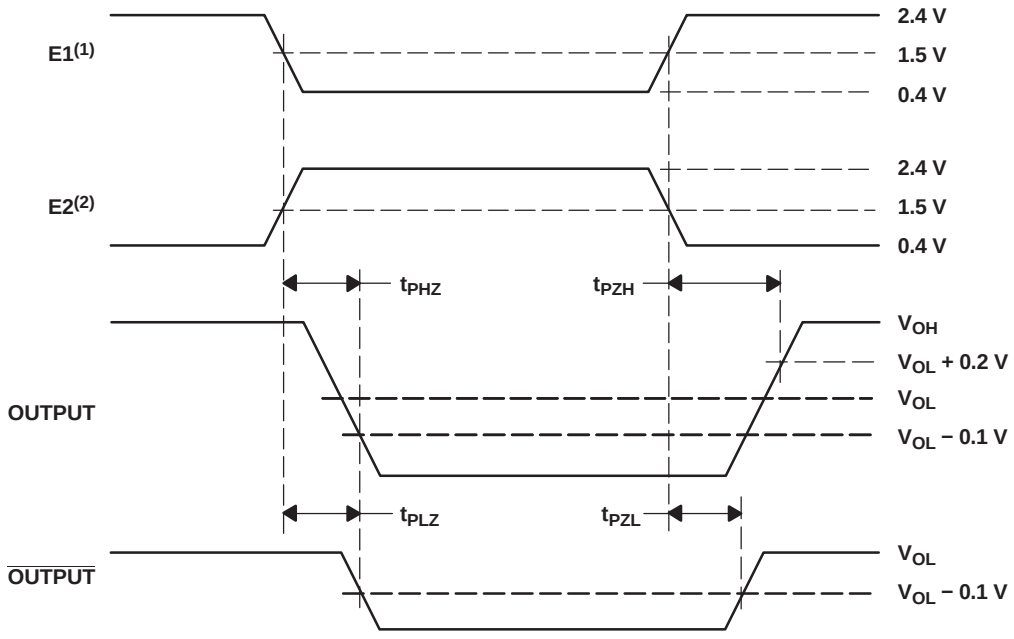


Figure 1. Propagation Delay Time Waveforms



(1) E2 = 1 while E1 changes state
(2) E1 = 0 while E2 changes state

NOTE: In the third state, both outputs (OUTPUT and $\overline{\text{OUTPUT}}$) are 0.1 V (max).

Figure 2. Enable and Disable Delay Time Waveforms

TEST CONDITIONS

Parametric values specified under the Electrical Characteristics and Switching Characteristics sections are measured with the following output load circuit.

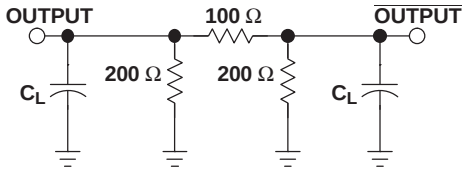


Figure 3. Driver Test Circuits, 5-V Nominal Supplies

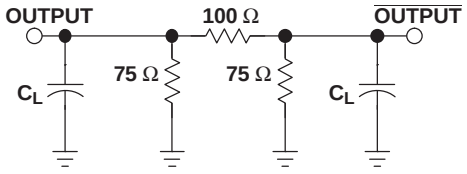
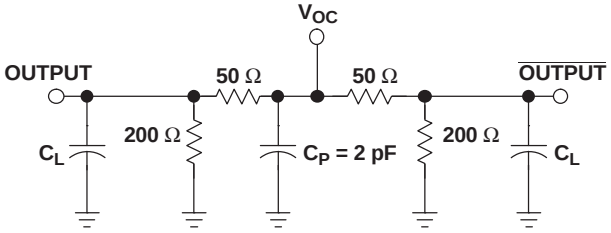
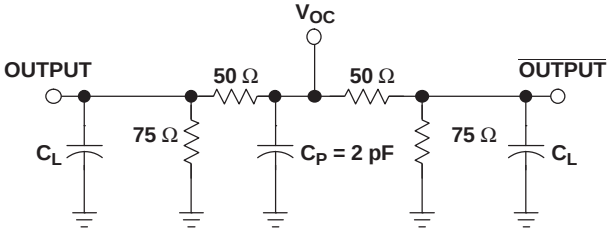


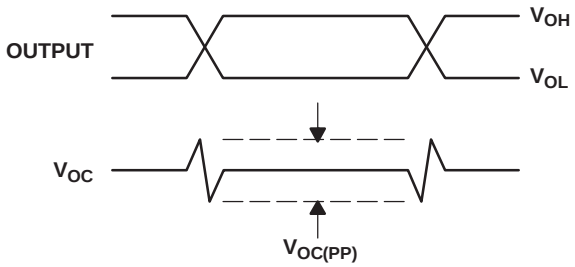
Figure 4. Driver Test Circuits, 3.3-V Nominal Supplies



Note: $V_{OC(PP)}$ load circuit for 5-V nominal supplies.

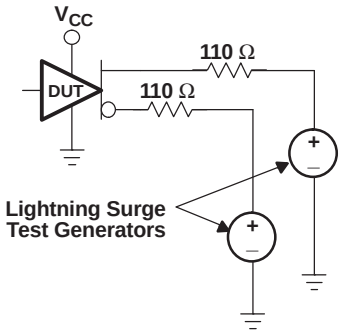


Note: $V_{OC(PP)}$ load circuit for 3.3-V nominal supplies.



Note: All input pulses are supplied by a generator having the following characteristics: t_r or t_f = 1 ns, pulse repetition rate (PRR) = 0.25 Mbps, pulse width = 500 ± 10 ns. C_P includes the instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 5. Test Circuits and Definitions for the Driver Common-Mode Output Voltage



Note: Surges may be applied simultaneously, but never in opposite polarities. Surge test pulses have $t_r = t_f = 2$ µs, pulse width = 7 µs (50% points), and period = 250 ms.

Figure 6. Lightning-Surge Testing Configuration for TB5D1M

TYPICAL CHARACTERISTICS

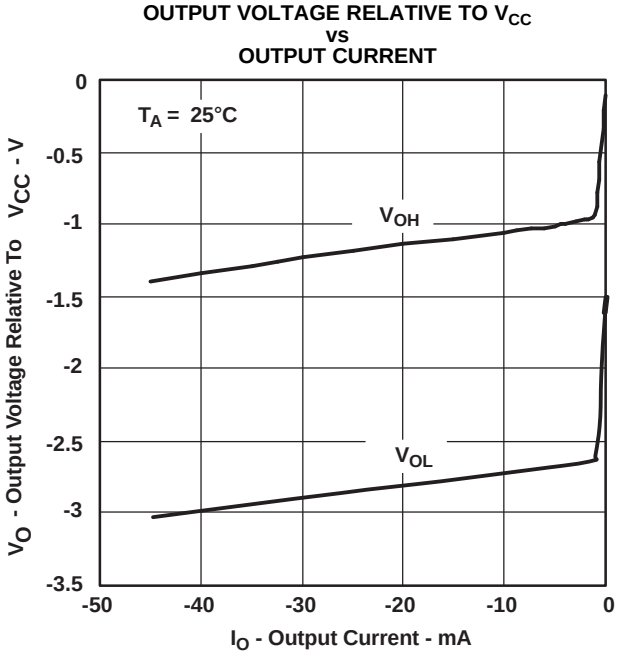


Figure 7.

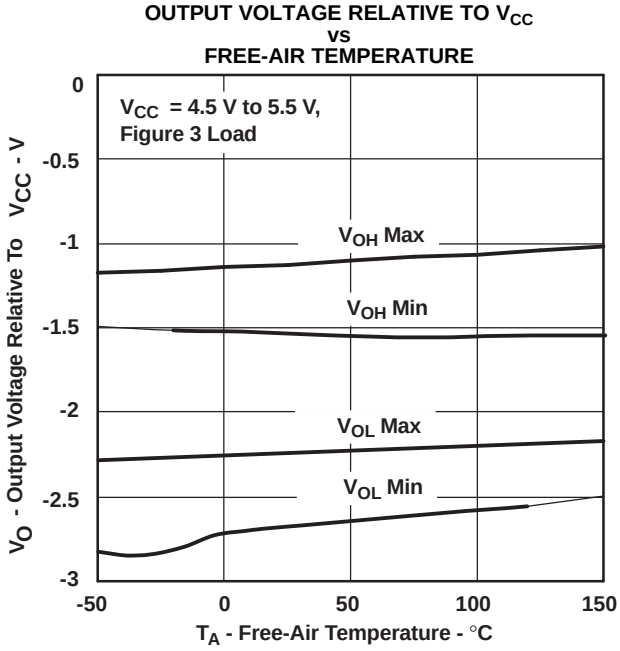


Figure 8.

TYPICAL CHARACTERISTICS (continued)

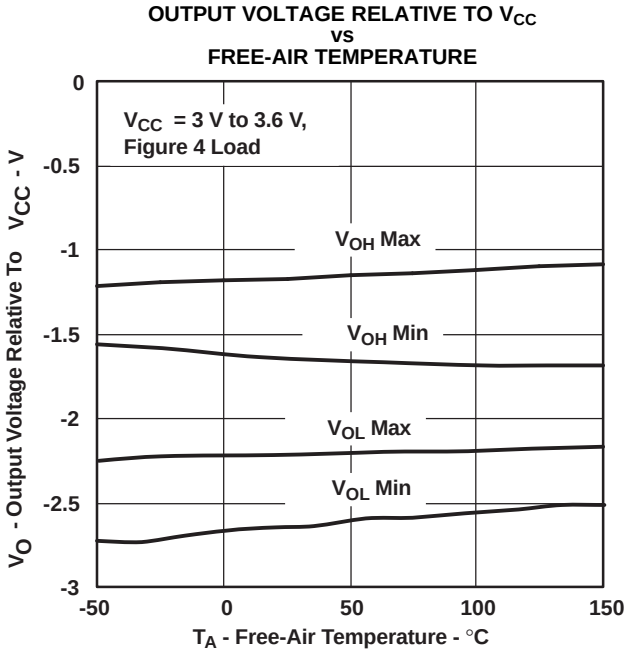


Figure 9.

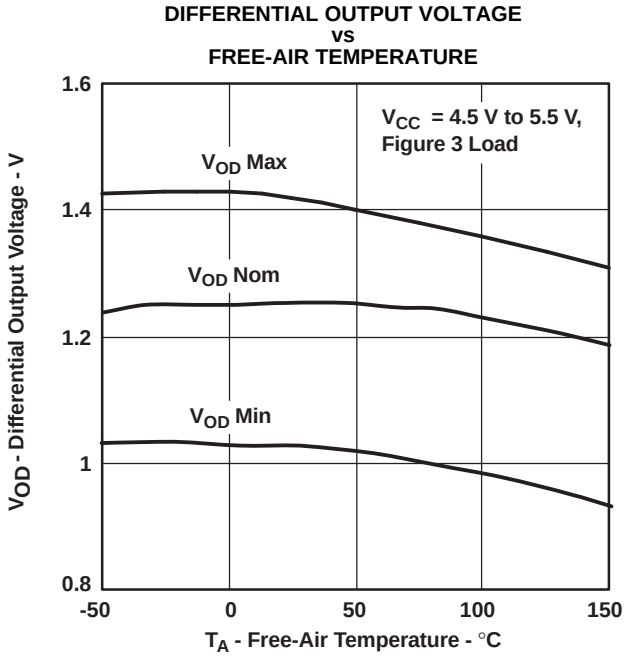


Figure 10.

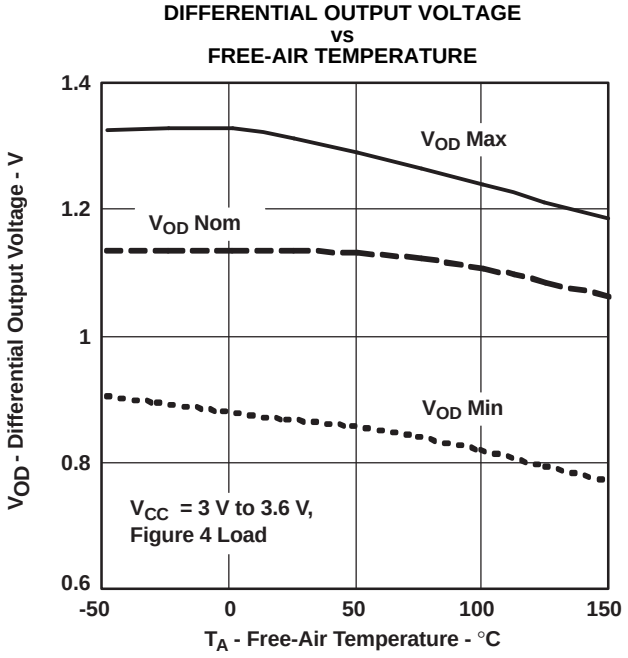


Figure 11.

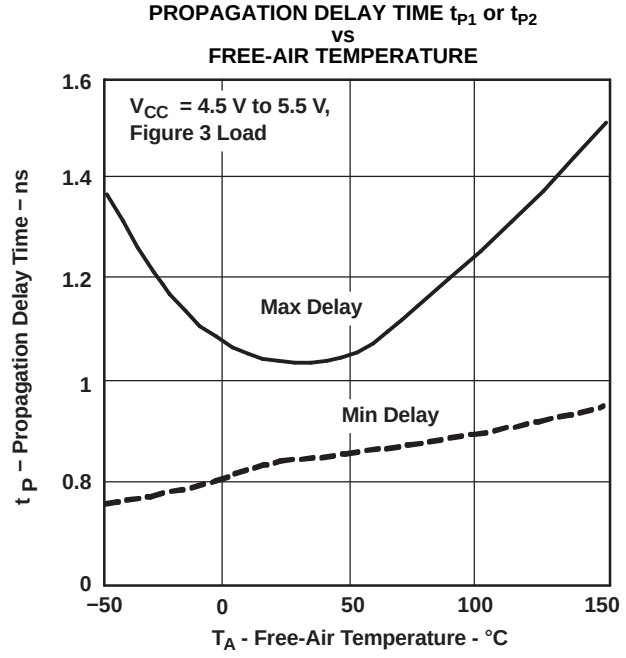


Figure 12.

TYPICAL CHARACTERISTICS (continued)

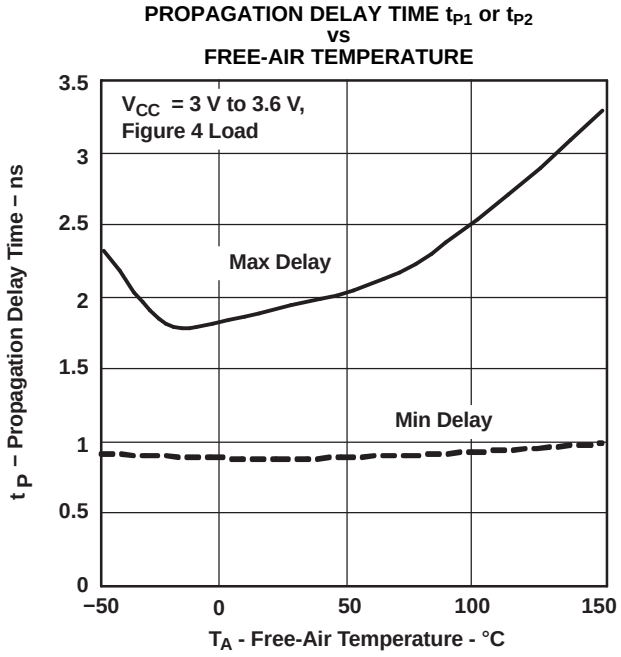


Figure 13.

APPLICATION INFORMATION

Power Dissipation

The power dissipation rating, often listed as the package dissipation rating, is a function of the ambient temperature, T_A, and the airflow around the device. This rating correlates with the device's maximum junction temperature, sometimes listed in the absolute maximum ratings tables. The maximum junction temperature accounts for the processes and materials used to fabricate and package the device, in addition to the desired life expectancy.

There are two common approaches to estimating the internal die junction temperature, T_J. In both of these methods, the device's internal power dissipation, P_D, needs to be calculated. This is done by totaling the supply power(s) to arrive at the system power dissipation:

$$\Sigma(V_{Sn} \times I_{Sn}) \quad (1)$$

and then subtracting the total power dissipation of the external load(s):

$$\Sigma(V_{Ln} \times I_{Ln}) \quad (2)$$

The first T_J calculation uses the power dissipation and ambient temperature, along with one parameter: θ_{JA}, the junction-to-ambient thermal resistance, in degrees Celsius per watt.

The product of P_D and θ_{JA} is the junction temperature rise above the ambient temperature. Therefore:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

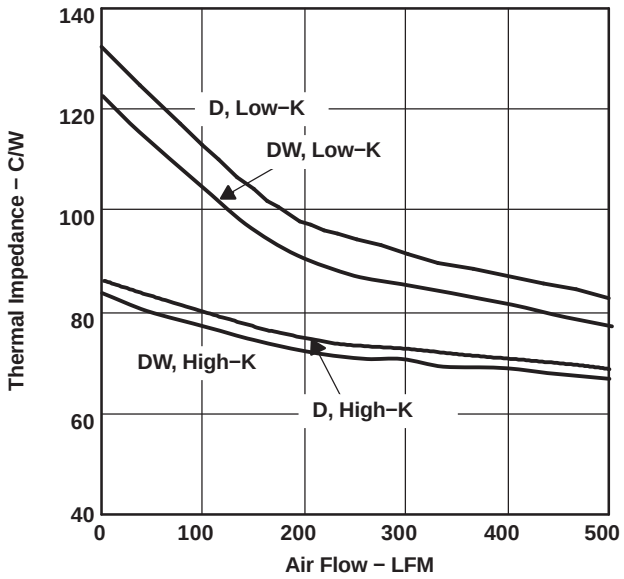


Figure 14. Thermal Impedance vs Air Flow

Note that θ_{JA} is highly dependent on the PCB on which the device is mounted, and on the airflow over the device and PCB. JEDEC/EIA has defined standardized test conditions for measuring θ_{JA}. Two commonly used conditions are the low-K and the high-K boards, covered by EIA/JESD51-3 and EIA/JESD51-7 respectively. Figure 14 shows the low-K and high-K values of θ_{JA} versus air flow for this device and its package options.

The standardized θ_{JA} values may not accurately represent the conditions under which the device is used. This can be due to adjacent devices acting as heat sources or heat sinks, to nonuniform airflow, or to the system PCB having significantly different thermal characteristics than the standardized test PCBs. The second method of system thermal analysis is more accurate. This calculation uses the power dissipation and ambient temperature, along with two device and two system-level parameters:

- θ_{JC}, the junction-to-case thermal resistance, in degrees Celsius per watt
- θ_{JB}, the junction-to-board thermal resistance, in degrees Celsius per watt
- θ_{CA}, the case-to-ambient thermal resistance, in degrees Celsius per watt
- θ_{BA}, the board-to-ambient thermal resistance, in degrees Celsius per watt.

In this analysis, there are two parallel paths, one through the case (package) to the ambient, and another through the device to the PCB to the ambient. The system-level junction-to-ambient thermal impedance, $\theta_{JA(S)}$, is the equivalent parallel impedance of the two parallel paths:

$$T_J = T_A + (P_D \times \theta_{JA(S)}) \quad (4)$$

where

$$\theta_{JA(S)} = \frac{(\theta_{JC} + \theta_{CA}) \times (\theta_{JB} + \theta_{BA})}{(\theta_{JC} + \theta_{CA} + \theta_{JB} + \theta_{BA})}$$

The device parameters θ_{JC} and θ_{JB} account for the internal structure of the device. The system-level parameters θ_{CA} and θ_{BA} take into account details of the PCB construction, adjacent electrical and mechanical components, and the environmental conditions including airflow. Finite element (FE), finite difference (FD), or computational fluid dynamics (CFD) programs can determine θ_{CA} and θ_{BA}. Details on using these programs are beyond the scope of this data sheet, but are available from the software manufacturers.

Load Circuits

The test load circuits shown in Figure 3 and Figure 4 are based on a recommended *pi* type of load circuit shown in Figure 15. The 100-Ω differential load resistor R_T at the receiver provide proper termination for the interconnecting transmission line, assuming it has a 100-Ω characteristic impedance. The two resistors R_S to ground at the driver end of the transmission line link provide dc current paths for the emitter follower output transistors. The two resistors to ground normally should not be placed at the receiver end, as they shunt the termination resistor, potentially creating an impedance mismatch with undesirable reflections.

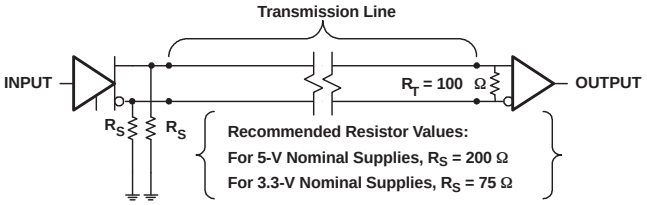


Figure 15. A Recommended *pi* Load Circuit

Another common load circuit, a *Y* load, is shown in Figure 16. The receiver-end line termination of R_T is provided by the series combination of the two RT/2 resistors, while the dc current path to ground is provided by the single resistor R_S. Recommended values, as a function of the nominal supply voltage range, are indicated in the figure.

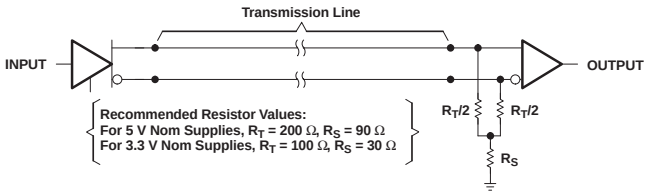


Figure 16. A Recommended *Y* Load Circuit

An additional load circuit, similar to one commonly used with ECL and PECL, is shown in Figure 17.

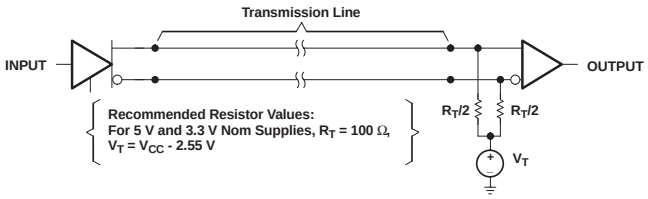


Figure 17. A Recommended PECL-Style Load Circuit

An important feature of all of these recommended load circuits is that they ensure that both of the emitter follower output transistors remain active (conducting current) at all times. When deviating from these recommended values, it is important to make sure that the low-side output transistor does not turn off. Failure to do so increases the t_{skew2} and $V_{OC(PP)}$ values, increasing the potential for electromagnetic radiation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TB5D1MD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MD.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MDE4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D1MDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D1M
TB5D2HD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HD.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HD1G4.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H
TB5D2HDW1G4.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5D2H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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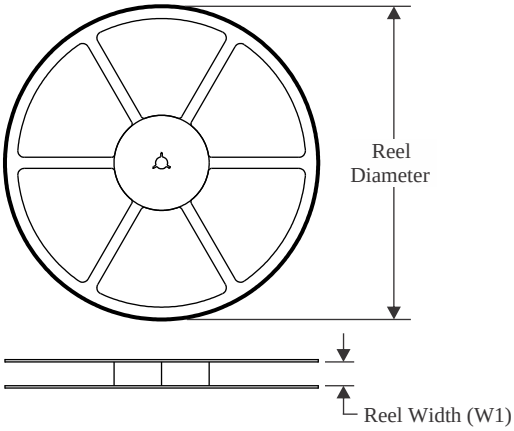
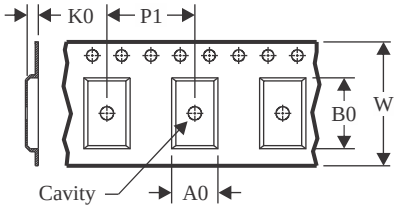
TAPE AND REEL INFORMATION

REEL DIMENSIONS

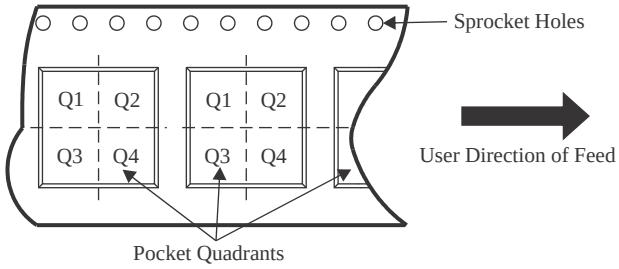


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

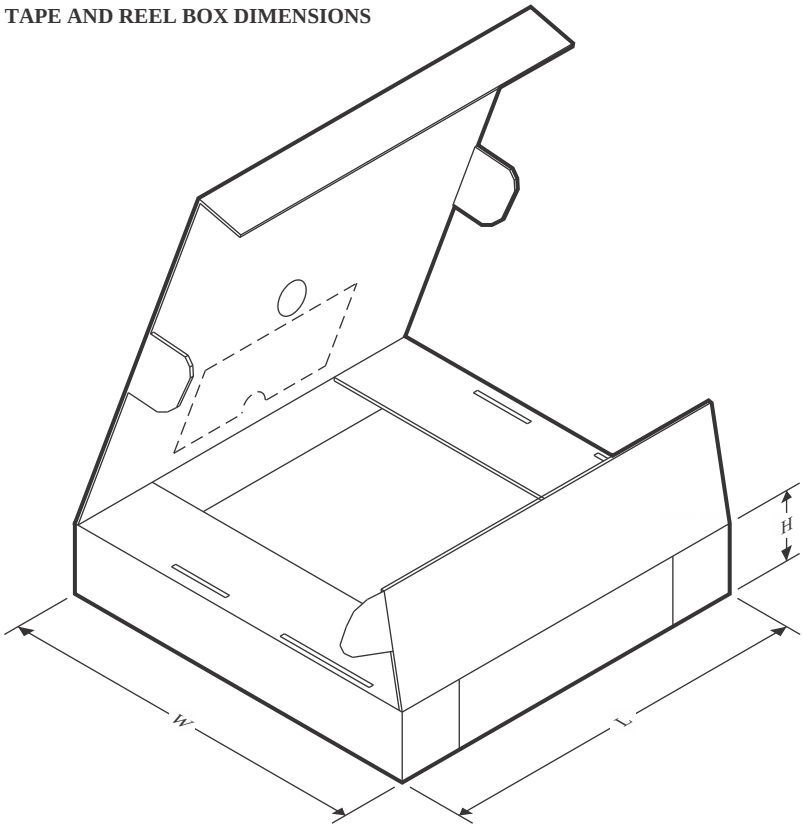
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TB5D1MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TB5D2HDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

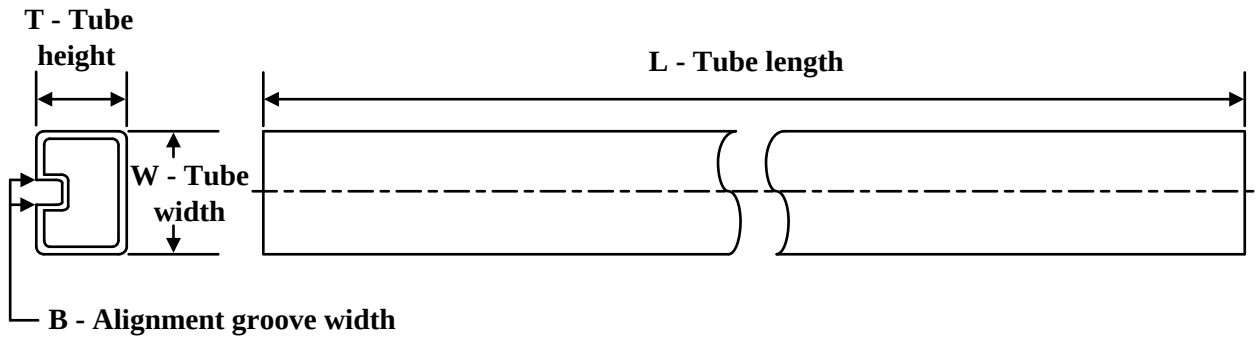
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TB5D1MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TB5D2HDR	SOIC	D	16	2500	350.0	350.0	43.0

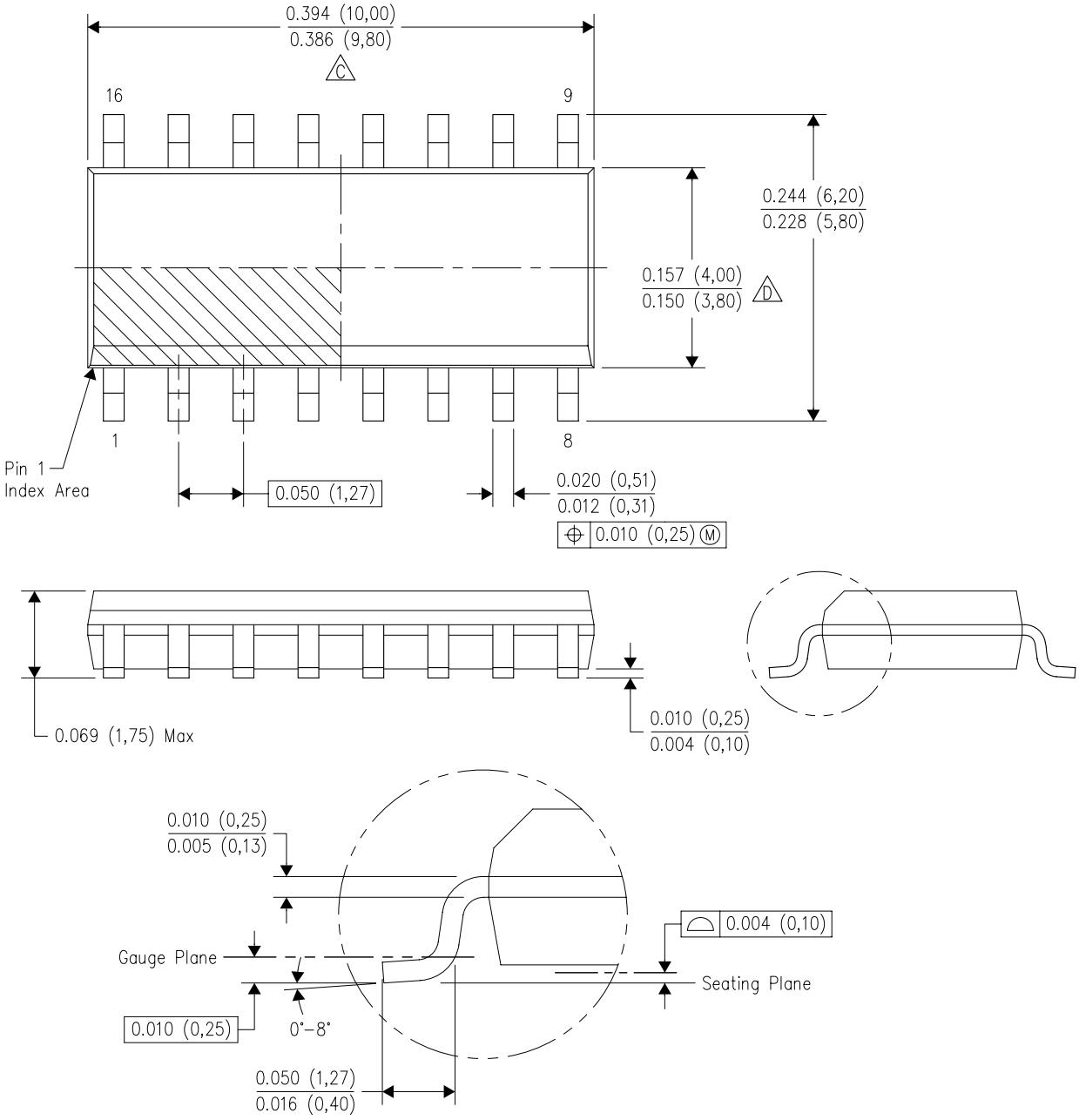
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TB5D1MD	D	SOIC	16	40	505.46	6.76	3810	4
TB5D1MD.B	D	SOIC	16	40	505.46	6.76	3810	4
TB5D1MDE4	D	SOIC	16	40	505.46	6.76	3810	4
TB5D1MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TB5D1MDW.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
TB5D2HD	D	SOIC	16	40	505.46	6.76	3810	4
TB5D2HD.B	D	SOIC	16	40	505.46	6.76	3810	4
TB5D2HD1G4.B	D	SOIC	16	40	505.46	6.76	3810	4
TB5D2HDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TB5D2HDW.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
TB5D2HDW1G4.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

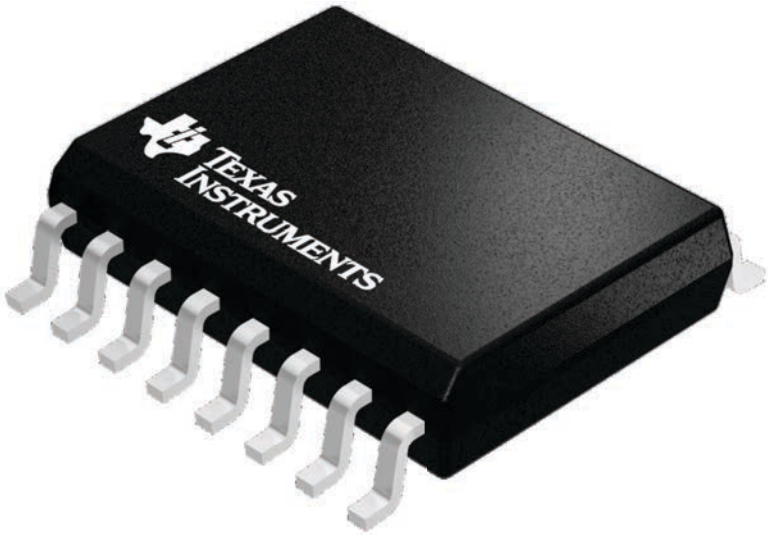
DW 16

SOIC - 2.65 mm max height

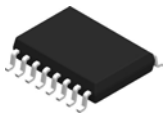
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

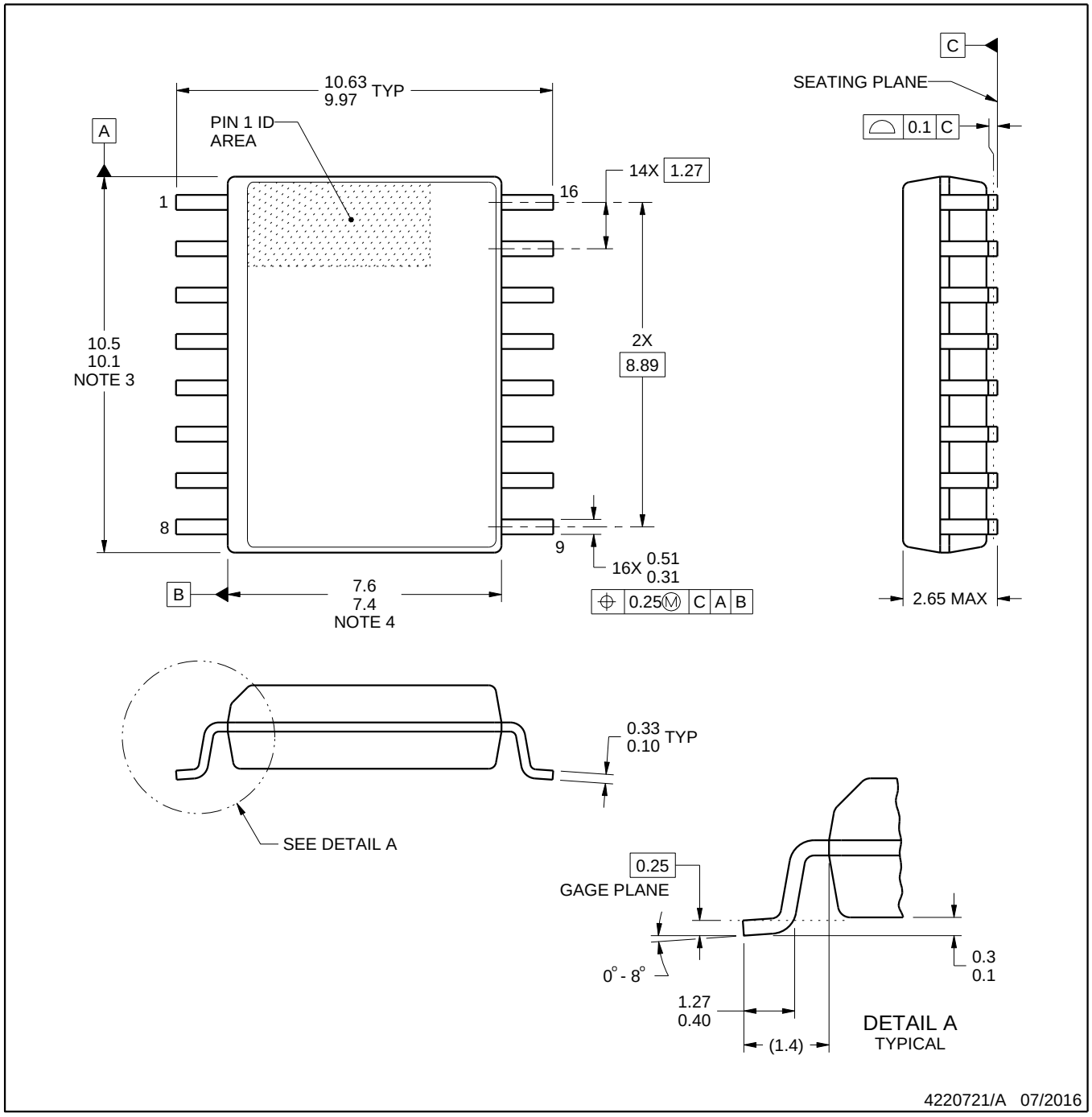


PACKAGE OUTLINE

DW0016A

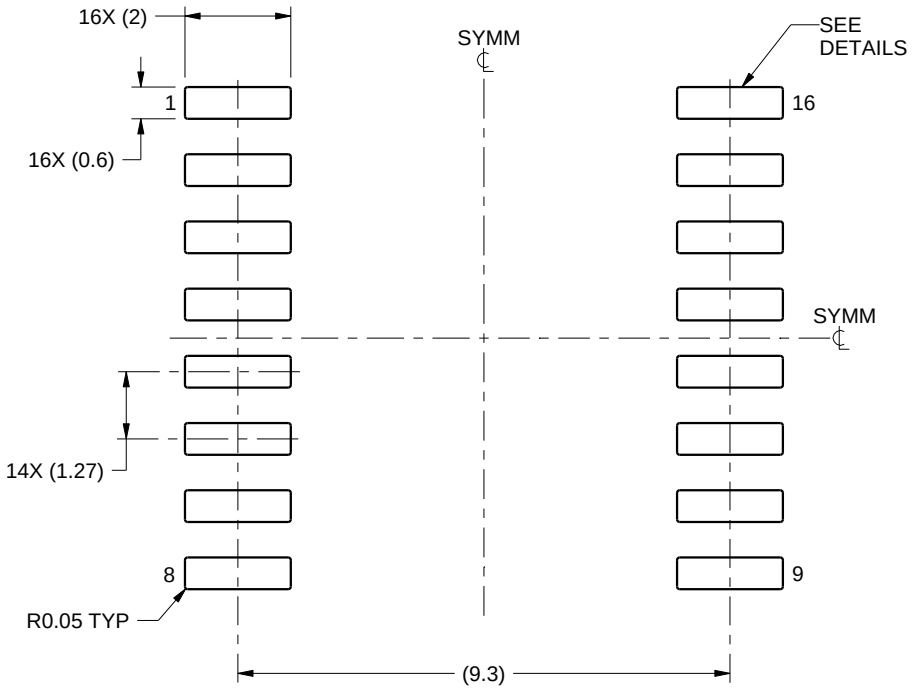
SOIC - 2.65 mm max height

SOIC

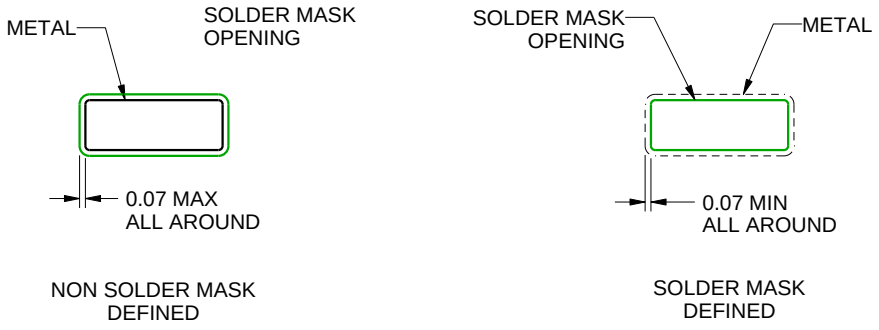


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

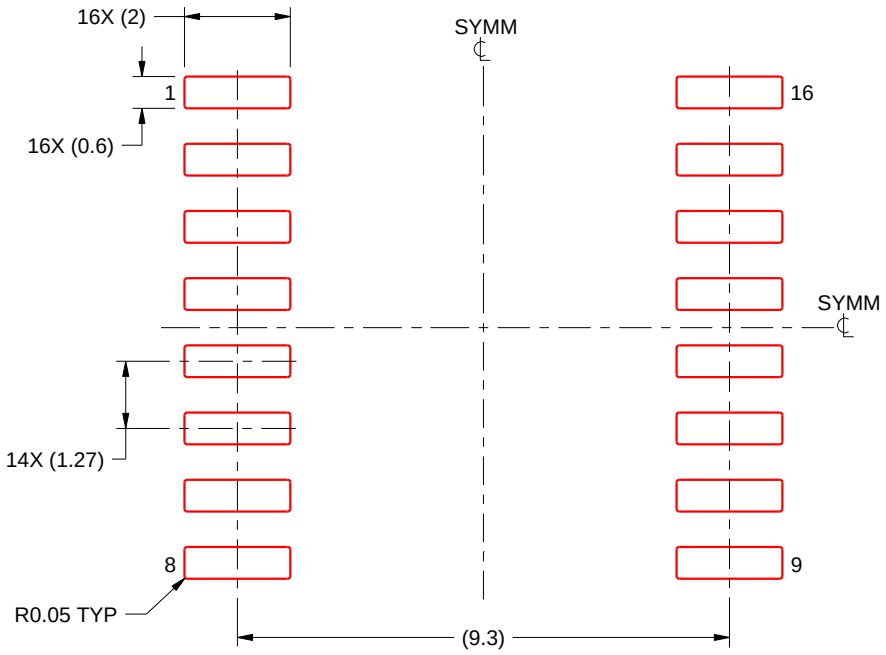


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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