

1.Description

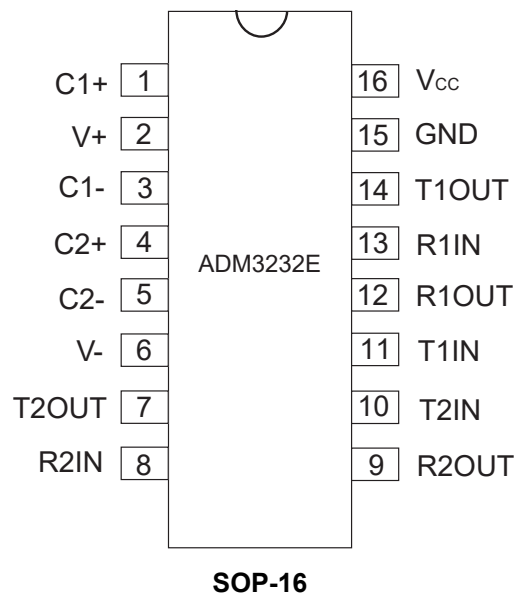
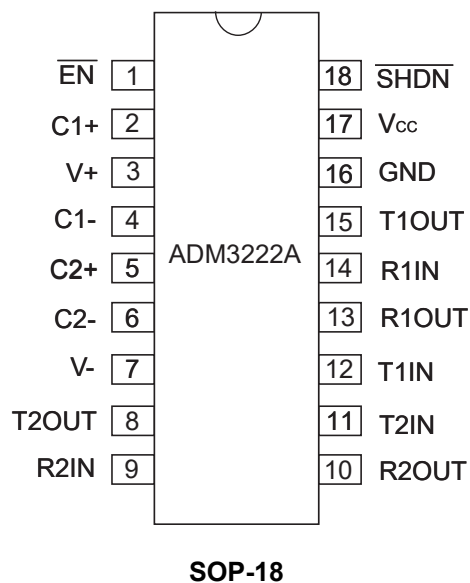
The ADM3222A/3232E series is an RS-232 transceiver solution intended for portable or handheld applications such as notebook or palmtop computers.

The ADM3222A/3232E series has a high-efficiency, charge-pump power supply that requires only 0.1 μ F capacitors in 3.3V operation. This charge pump allows the ADM3222A/3232E series to deliver true RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The ADM3222A/3232E are 2-driver/2-receiver devices. This series is ideal for portable or handheld applications such as notebook or palmtop computers.

2.Features

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Minimum 120Kbps Data Rate Under Full Load
- 1 μ A Low-Power Shutdown with Receivers Active (ADM3222A)
- Enhanced ESD Specifications:
 - ± 15 kV Human Body Model
 - ± 15 kV IEC1000-4-2 Air Discharge
 - ± 8 kV IEC1000-4-2 Contact Discharge

3.Pinning information





4. Selection Table

MODEL	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Shutdown	TTL 3-State	No. of Pins
ADM3222A	+3.0V to +5.5V	2	2	4	Yes	Yes	18
ADM3232E	+3.0V to +5.5V	2	2	4	No	No	16

5. Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Short-Circuit Duration

TxOUT Continuous

Storage Temperature -65°C to +150°C

Power Dissipation Per Package

18-pin SOP (derate 15.7mW/°C above +70°C) ... 1260mW

16-pin SOP (derate 13.57mW/°C above +70°C) .. 1086mW

V_{CC}-0.3V to +6.0V

V_+ (NOTE 1).....-0.3V to +7.0V

V_- (NOTE 1).....+0.3V to -7.0V

$V_+ + |V_-|$ (NOTE 1).....+13V

I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages

TxIN, EN -0.3V to +6.0V

RxIN ±15V

Output Voltages

TxOUT ±15V

RxOUT -0.3V to ($V_{CC} + 0.3V$)

NOTE 1: V_+ and V_- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.



6. Electrical Characteristics

Unless otherwise noted, the following specifications apply for $V_{CC}=+3.0V$ to $+5.0V$ with $T_{AMB}=T_{MIN}$ to T_{MAX}

Parameter	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS					
Supply Current	no load, $T_{AMB}=+25^{\circ}C$, $V_{CC}=3.3V$		1	3	mA
Shutdown Supply Current	SHDN=GND, $T_{AMB}=25^{\circ}C$, $V_{CC}=3.3V$		1	10	μA
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold Low	TxIN, EN, SHDN, Note2			0.8	V
Input Logic Threshold HIGH	$V_{CC}=3.3V$, Note2	2			V
	$V_{CC}=5V$, Note2	2.4			V
Input Leakage Current	TxIN, EN, SHDN $T_{AMB}=25^{\circ}C$		± 0.01	± 1	μA
Output Leakage Current	receivers disable		± 0.05	± 10	μA
Output Voltage LOW	$I_{OUT}=1.6mA$			0.4	V
Output Voltage HIGH	$I_{OUT}=-1mA$	$V_{CC}-0.6$	$V_{CC}-0.1$		V
DRIVER OUTPUTS					
Output Voltage Swing	3k Ω load to ground at all driver outputs $T_{AMB}=25^{\circ}C$	± 5	± 5.4		V
Output Resistance	$V_{CC}=V+=V-=0V$, $T_{OUT}=\pm 2V$	300			Ω
Output Short-Circuit Current	$V_{OUT}=0V$		± 35	± 60	mA
	$V_{OUT}=\pm 15V$		± 70	± 100	mA
Output Leakage Current	$V_{OUT}=\pm 12V$, $V_{CC}=0V$ to $5.5V$ drivers disabled			± 25	μA



7. Electrical Characteristics

Unless otherwise noted, the following specifications apply for $V_{CC}=3V$ to $5V$ with $T_{AMB}=T_{MIN}$ to T_{MAX} .

Typical Values apply at $V_{CC}=3.3V$ or $5V$ and $T_{AMB}=25^{\circ}C$

Parameter	Conditions	Min	Typ	Max	Units
RECEIVER INPUTS					
Input Voltage Range		-15		15	V
Input Threshold LOW	$V_{CC}=3.3V$	0.6	1.2		V
	$V_{CC}=5V$	0.8	1.5		V
Input Threshold HIGH	$V_{CC}=3.3V$		1.5	2.4	V
	$V_{CC}=5V$		1.8	2.4	V
Input Hysteresis			0.3		V
Input Resistance		3	5	7	k Ω
TIMING CHARACTERISTICS					
Maximum Data Rate	$R_L=3k\Omega$, $C_L=1000pF$, one driver switching	120	235		kbps
Driver Propagation Delay	t_{PHL} , $R_L=3K\Omega$, $C_L=1000pF$		1		μs
	t_{PLH} , $R_L=3K\Omega$, $C_L=1000pF$		1		μs
Receiver Propagation Delay	t_{PHL} , RxIN to RxOUT, $C_L=150pF$		0.3		μs
	t_{PLH} , RxIN to RxOUT, $C_L=150pF$		0.3		μs
Receiver Output Enable Time			200		ns
Receiver Output Disable Time			200		ns
Driver Skew	$ t_{PHL} - t_{PLH} $, $T_{AMB}=25^{\circ}C$		100	500	ns
Receiver Skew	$ t_{PHL} - t_{PLH} $		200	1000	ns
Transition-Region Slew Rate	$V_{CC}=3.3V$, $R_L=3K\Omega$, $T_{AMB}=25^{\circ}C$ measurements taken from -3.0V to +3.0V or +3.0V to -3.0V			30	V/ μs

NOTE 2: Driver input hysteresis is typically 250mV.



8. Typical Characteristic

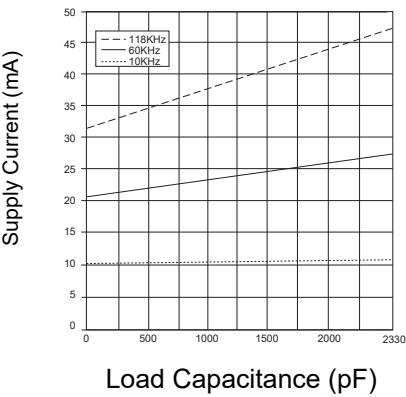


Figure 1: Supply Current VS. Load Capacitance when Transmitting Data for the ADM3222 and the ADM3232

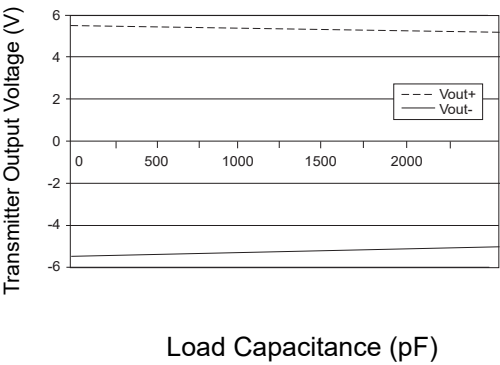


Figure 2: Transmitter Output Voltage VS. Load Capacitance for the ADM3222 and the ADM3232

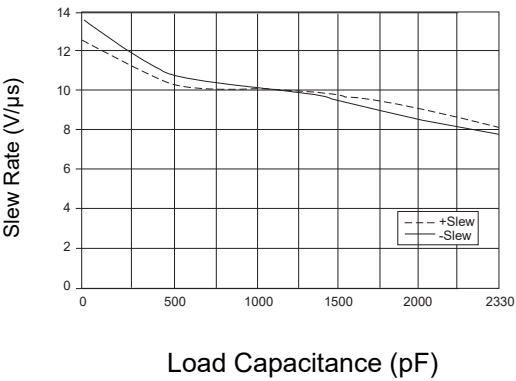


Figure 3: Slew Rate VS. Load Capacitance for the ADM3222 and the ADM3232



9.Pin Functions

Name	Pin Number		Function
	ADM3222A	ADM3222A	
$\overline{\text{EN}}$	1	-	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state)
C1+	2	1	Positive terminal of the voltage doubler charge-pump capacitor.
V+	3	2	+5.5V generated by the charge pump.
C1-	4	3	Negative terminal of the voltage doubler charge-pump capacitor.
C2+	5	4	Positive terminal of the inverting charge-pump capacitor.
C2-	6	5	Negative terminal of the inverting charge-pump capacitor.
V-	7	6	5.5V generated by the charge pump.
T1OUT	15	14	RS-232 driver output.
T2OUT	8	7	RS-232 driver output.
R1IN	14	13	RS-232 receiver input.
R2IN	9	8	RS-232 receiver input.
R1OUT	13	12	TTL CMOS receiver output.
R2OUT	10	9	TLC MOS receiver output.
T1IN	12	11	TTL CMOS driver input.
T2IN	11	10	TTL CMOS driver input.
GND	16	15	Ground.
V _{CC}	17	16	+3.0V to +5.5V supply voltage
$\overline{\text{SHDN}}$	18	-	Shutdown Control input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply.
N.C.	-	-	No Connect.



10. Typical Operating Circuits

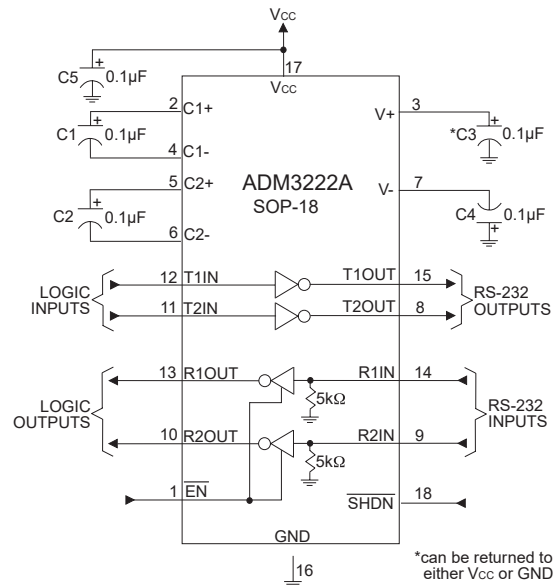


Figure 6. ADM3222A Typical Operating Circuits

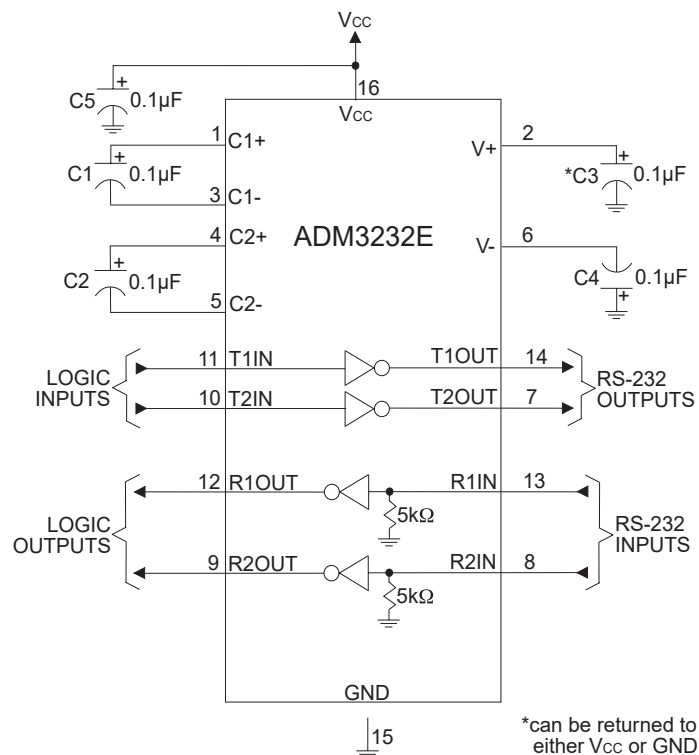


Figure 7. ADM3232E Typical Operating Circuit



11. Description

The ADM3222A/3232E transceivers meet the EIA/TIA-232 and V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The ADM3222A/3232E devices all feature ADM3222A proprietary on-board charge pump circuitry that generates $2 \times V_{CC}$ for RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.3V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The ADM3222A/3232E series have drivers that operate at a typical data rate of 235Kbps fully loaded. The and ADM3232E are 2-driver/2-receiver devices ideal for portable or hand-held applications.

The ADM3222A features a $1\mu A$ shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only $1\mu A$ supply current.

THEORY OF OPERATION

The ADM3222A/3232E series are made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. the Sipex proprietary charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm 5.0V$ EIA/TIA-232 levels inverted relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.5V$ with no load

and at least $\pm 5V$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of $\pm 3.7V$ with supply voltages as low as 2.7V.

The drivers typically can operate at a data rate of 235Kbps. The drivers can guarantee a data rate of 120Kbps fully loaded with $3K\Omega$ in parallel with 1000 pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of $30V/\mu s$ in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

The ADM3222A/3232E drivers can maintain high data rates up to 235Kbps fully loaded. Figure 8 shows a loopback test circuit used to test the RS-232 drivers. Figure 9 shows the test results of the loopback circuit with all drivers active at 120Kbps with RS-232 loads in parallel with 1000pF capacitors. Figure 10 shows the test results where one driver was active at 235Kbps and all drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.



The ADM3222A driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the ADM3222A device permits the outputs to be driven up to $\pm 12V$. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to V_{CC} or GND. In the shutdown mode, the supply current falls to less than $1\mu A$, where $\overline{SHDN} = LOW$. When the ADM3222A device is shut down, the device's driver outputs are disabled (tri-stated) and the

charge pumps are turned off with $V+$ pulled down to V_{CC} and $V-$ pulled to GND. The time required to exit shutdown is typically $100\mu s$. Connect \overline{SHDN} to VCC if the shutdown mode is not used. \overline{SHDN} has no effect on RxOUT or RxOUTB. As they become active, the two driver outputs go to opposite RS-232 levels where one driver input is HIGH and the other LOW. Note that the drivers are enabled only when the magnitude of $V-$ exceeds approximately 3V



12. Test Circuit

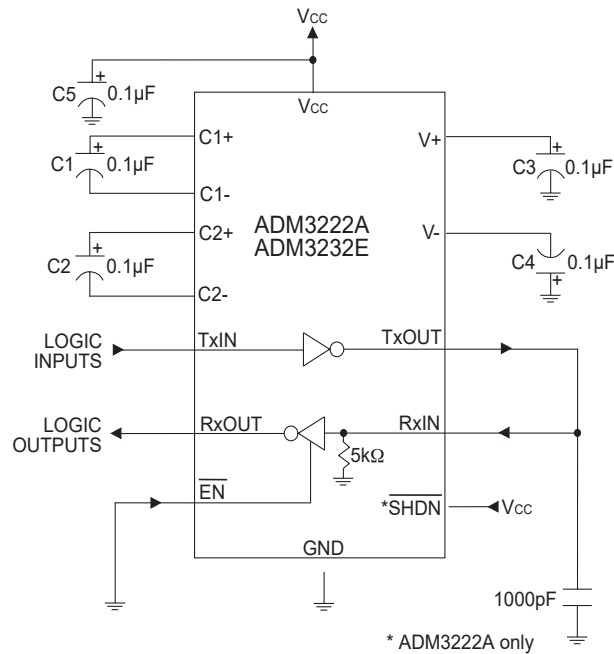


Figure 8. ADM3222A/3232E Driver Loopback Test Circuit

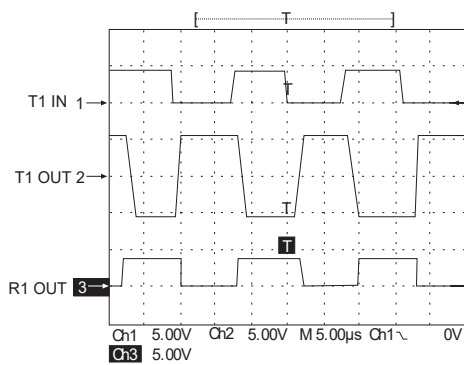


Figure 9. Driver Loopback Test Results at 120kbps

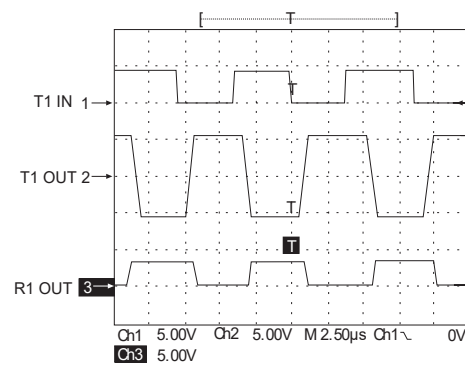


Figure 10. Driver Loopback Test Results at 235kbps



13.Receivers

Receivers

The receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. All receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control EN = HIGH. In the shutdown mode, the receivers can be active or inactive. EN has no effect on TxOUT. The truth table logic of the ADM3222A/3232E driver and receiver outputs can be found in Table 2.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump uses a unique approach compared to older less-efficient designs. The

SHDN	EN	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. Truth Table Logic for Shutdown and Enable Control

charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. In most circumstances, decoupling the power supply can be achieved adequately using a 0.1μF bypass capacitor at C5 (refer to Figures 6 and 7). In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pumps operate in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pumps are enabled. If the output voltage exceed a magnitude of 5.5V, the charge pumps are disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2 — Since C_2^+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now 2 times V_{CC}



Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3 . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2+ is at V_{CC} , the voltage potential across C_2 is 2 times V_{CC} .

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4 , the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both $V+$ and $V-$ are separately generated from V_{CC} ; in a no-load condition $V+$ and $V-$ will be symmetrical. Older charge pump approaches that generate $V-$ from $V+$ will show a decrease in the magnitude of $V-$ compared to $V+$ due to the inherent inefficiencies in the design. The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

ESD Tolerance

The ADM3222A/3232E series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ± 15 kV without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's



potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 17. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage.

The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown

on Figure 18. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method. With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

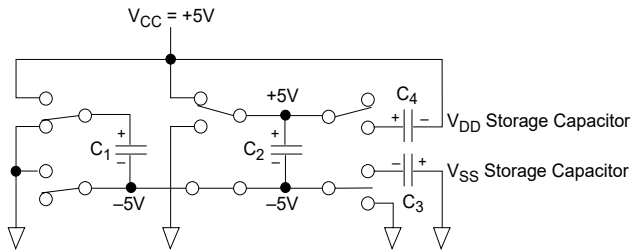


Figure 12. Charge Pump — Phase 1

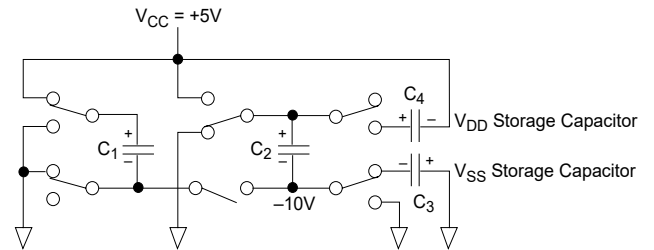


Figure 13. Charge Pump — Phase 2

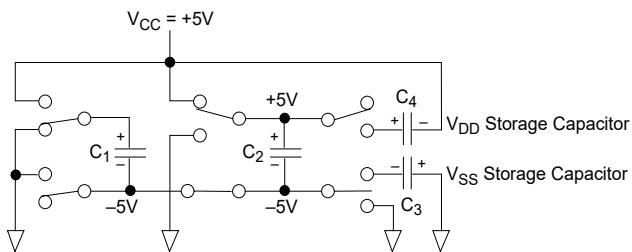


Figure 15. Charge Pump — Phase 3

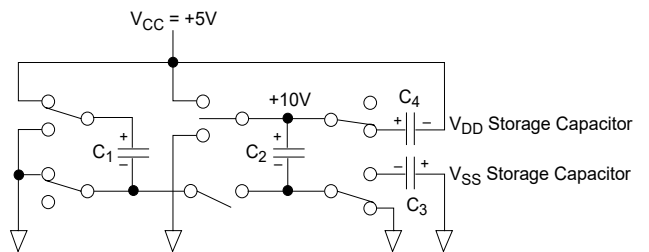


Figure 16. Charge Pump — Phase 4

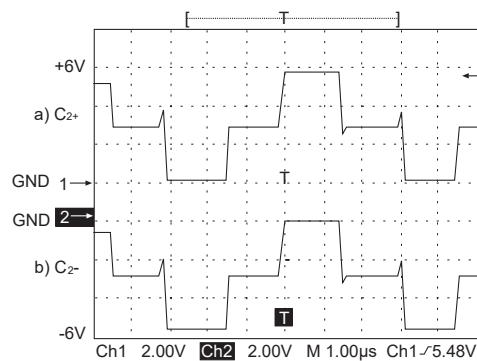


Figure 14. Charge Pump Waveforms

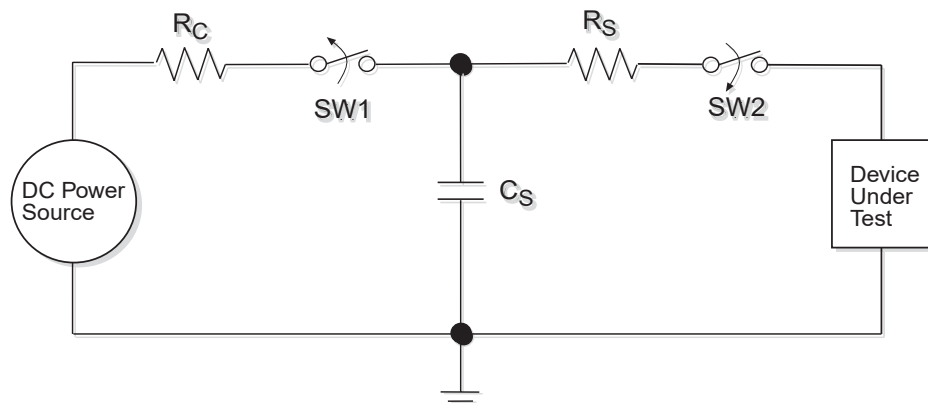


Figure 17. ESD Test Circuit for Human Body Model

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 17 and 18 represent the typical ESD testing circuits used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

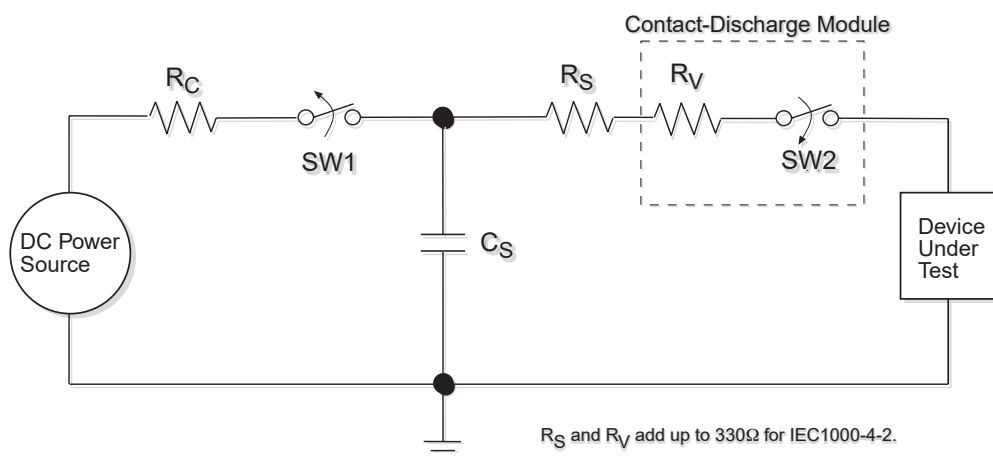


Figure 18. ESD Test Circuit for IEC1000-4-



For the Human Body Model, the current limiting resistor (R_s) and the source capacitor(C_s) are 1.5k Ω an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_s) and the source capacitor (C_s) are 330 Ω an 150pF, respectively. The higher C_s value and lower R_s value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

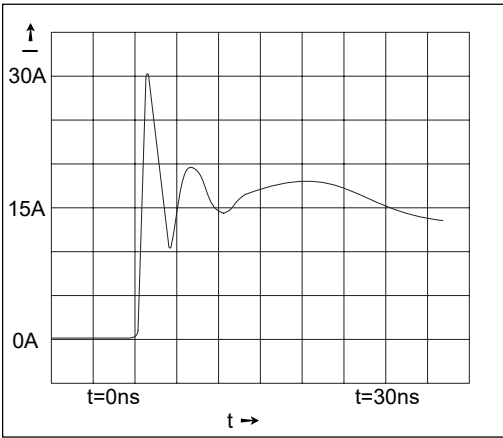


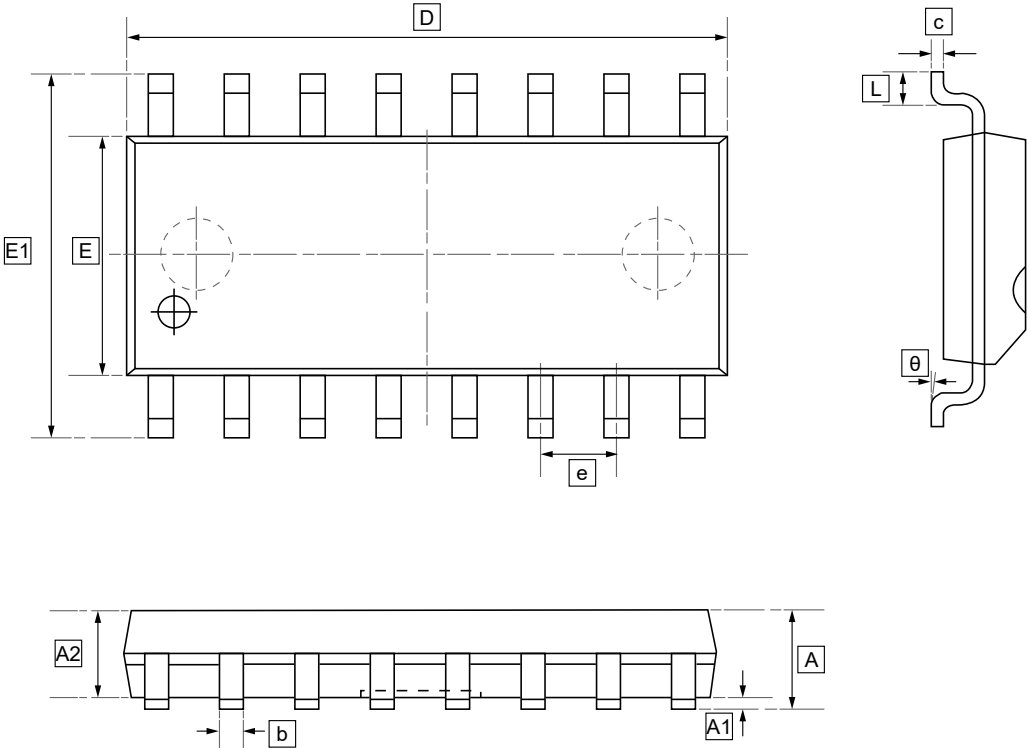
Figure 19. ESD Test Waveform for IEC1000-4-2

Device Pin	Human Body	IEC1000-4-2		
Tested	Model	Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 3. Transceiver ESD Tolerance Levels



14.1SOP-16 Package Outline Dimensions

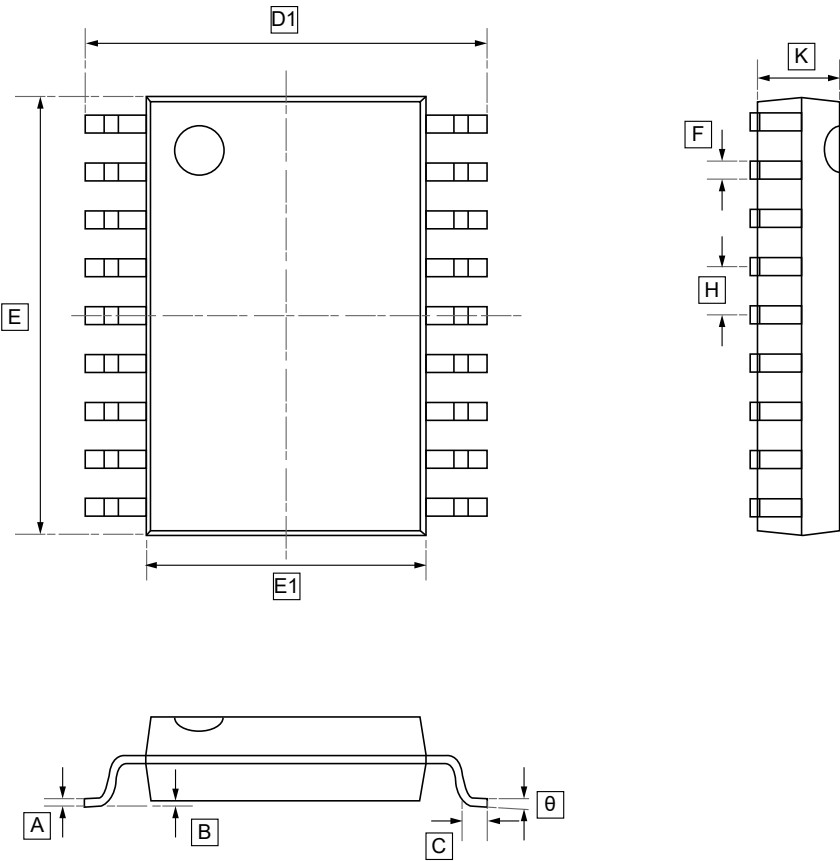


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0	1.350	0.330	0.170	9.800	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	10.200	4.000	6.200	BSC	1.270	8°



14.2SOP-18 Package Outline Dimensions

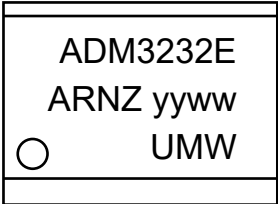


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D1	E	E1	H	F	K	θ
Min	0.15	0.00	0.62	10.40	11.50	7.30	1.22	0.40	2.20	0°
Max	0.25	0.15		10.80	11.70	7.40	1.32	0.50	2.40	5°



15.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW ADM3222ARWZ	SOP-18	2000	Tape and reel
UMW ADM3232EARNZ	SOP-16	2500	Tape and reel



16.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

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