SN74LV4T125-EP Single Power Supply Quadruple Buffer Translator GATE With 3-State Output CMOS Logic Level Shifter

1 Features

- Wide operating range of 1.8V to 5.5V
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- 5.5V tolerant input pins
- Supports standard pinouts
- Up to 150Mbps with 5V or 3.3V V_{CC}
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

3 Description

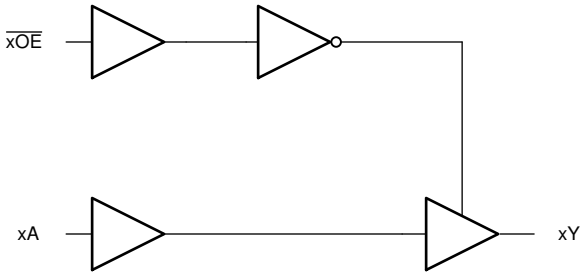
The SN74LV4T125-EP contains four independent buffers with 3-state outputs and extended voltage operation to allow for level translation. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a high impedance (Hi-Z) state by applying a HIGH on the $\overline{OE}$ pin. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example, 1.2V input to 1.8V output or 1.8V input to 3.3V output). In addition, the 5V tolerant input pins enable down translation (for example, 3.3V to 2.5V output).

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)	BODY SIZE (NOM)(4)
SN74LV4T125-EP	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.4 mm

(1) See, Additional Product Selection
(2) For more information, see Section 12.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.
(4) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Additional Product Selection....2
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....4
6.4 Thermal Information....5
6.5 Electrical Characteristics....5
6.6 Switching Characteristics....6
6.7 Noise Characteristics....7
6.8 Typical Characteristics....7
7 Parameter Measurement Information....10
8 Detailed Description....11
8.1 Overview....11
8.2 Functional Block Diagram....11
8.3 Feature Description....11
8.4 Device Functional Modes....14
9 Applications and Implementation....15
9.1 Application Information....15
9.2 Typical Application....15
9.3 Power Supply Recommendations....16
9.4 Layout....16
10 Device and Documentation Support....17
10.1 Receiving Notification of Documentation Updates....17
10.2 Support Resources....17
10.3 Trademarks....17
10.4 Electrostatic Discharge Caution....17
10.5 Glossary....17
11 Revision History....17
12 Mechanical, Packaging, and Orderable Information....17

4 Additional Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T34	DCK, DBV, DRL	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV, DRL	Single Buffer Gate with 3-state Output
SN74LV4T125-EP	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

Copyright © 2024 Texas Instruments Incorporated

5 Pin Configuration and Functions

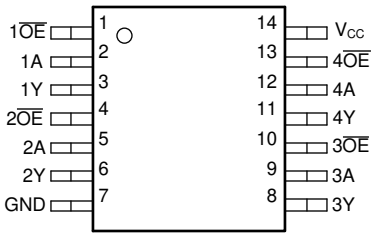


Figure 5-1. PW Package, 14-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1$\overline{OE}$	1	I	Channel 1, output enable, active low
1A	2	I	Channel 1, input A
1Y	3	O	Channel 1, output Y
2$\overline{OE}$	4	I	Channel 2, output enable, active low
2A	5	I	Channel 2, input A
2Y	6	O	Channel 2, output Y
GND	7	G	Ground
3Y	8	O	Channel 3, output Y
3A	9	I	Channel 3, input A
3$\overline{OE}$	10	I	Channel 3, output enable, active low
4Y	11	O	Channel 4, output Y
4A	12	I	Channel 4, input A
4$\overline{OE}$	13	I	Channel 4, output enable, active low
V_{CC}	14	P	Positive supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

Copyright © 2024 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} +0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 2V	1.1		V
		V_{CC} = 2.25V to 2.75V	1.28		
		V_{CC} = 3V to 3.6V	1.45		
		V_{CC} = 4.5V to 5.5V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V to 2V		0.5	V
		V_{CC} = 2.25V to 2.75V		0.65	
		V_{CC} = 3V to 3.6V		0.75	
		V_{CC} = 4.5V to 5.5V		0.85	
I_O	Output current	V_{CC} = 1.6V to 2V		±3	mA
		V_{CC} = 2.25V to 2.75V		±7	
		V_{CC} = 3.3V to 5.0V		±15	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.6V to 5.0V		20	ns/V
T_A	Operating free-air temperature		-55	125	°C

Copyright © 2024 Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		SN74LV4T125-EP-EP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -50µA	1.65V to 5.5V	V_{CC}-0.1			V_{CC}-0.1			V
	I_{OH} = -2mA	1.65V to 2V	1.28	1.7 (1)		1.21			
	I_{OH} = -3mA	2.25V to 2.75V	2	2.4(1)		1.93			
	I_{OH} = -5.5mA	3V to 3.6V	2.6	3.08(1)		2.49			
	I_{OH} = -8mA	4.5V to 5.5V	4.1	4.65(1)		3.95			
V_{OL}	I_{OL} = 50µA	1.65V to 5.5V			0.1			0.1	V
	I_{OL} = 2mA	1.65V to 2V		0.1(1)	0.2			0.25	
	I_{OL} = 3mA	2.25V to 2.75V		0.1(1)	0.15			0.2	
	I_{OL} = 5.5mA	3V to 3.6V		0.2(1)	0.2			0.25	
	I_{OL} = 8mA	4.5V to 5.5V		0.3(1)	0.3			0.35	
I_I	V_I = 0V or V_{CC}	0V to 5.5V			±0.1			±1	µA
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5V	5.5V			±0.25			±2.5	µA
I_{CC}	V_I = 0V or V_{CC}, I_O = 0; open on loading	1.65V to 5.5V			2			20	µA
ΔI_{CC}	One input at 0.3V or 3.4V, other inputs at 0 or V_{CC}, I_O = 0	5.5V			1.35			1.5	mA
	One input at 0.3V or 1.1V, other inputs at 0 or V_{CC}, I_O = 0	1.8V			10			20	µA
C_I	V_I = V_{CC} or GND	5V		4	10			10	pF
C_O	V_O = V_{CC} or GND	5V		3					pF
C_{PD}	No load, F = 1MHz	5V		14					pF

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)

Copyright © 2024 Texas Instruments Incorporated

6.6 Switching Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	MIN	TYP	MAX	UNIT
t_{PHL}	A	Y	C_L = 15pF	1.8V		15.6	40.1	ns
t_{PLH}	A	Y	C_L = 15pF	1.8V		11.8	40.1	ns
t_{PHZ}	OE	Y	C_L = 15pF	1.8V		13.0	20.9	ns
t_{PLZ}	OE	Y	C_L = 15pF	1.8V		11.7	18.5	ns
t_{PZH}	OE	Y	C_L = 15pF	1.8V		17.4	33.3	ns
t_{PZL}	OE	Y	C_L = 15pF	1.8V		16.8	32.3	ns
t_{PHL}	A	Y	C_L = 50pF	1.8V		21.0	46.7	ns
t_{PLH}	A	Y	C_L = 50pF	1.8V		16.1	46.7	ns
t_{PHZ}	OE	Y	C_L = 50pF	1.8V		19.7	28.2	ns
t_{PLZ}	OE	Y	C_L = 50pF	1.8V		18.6	25.9	ns
t_{PZH}	OE	Y	C_L = 50pF	1.8V		19.9	37.1	ns
t_{PZL}	OE	Y	C_L = 50pF	1.8V		19.1	35.8	ns
t_{PHL}	A	Y	C_L = 15pF	2.5V		10.6	24.0	ns
t_{PLH}	A	Y	C_L = 15pF	2.5V		7.1	24.0	ns
t_{PHZ}	OE	Y	C_L = 15pF	2.5V		8.2	12.6	ns
t_{PLZ}	OE	Y	C_L = 15pF	2.5V		7.4	11.1	ns
t_{PZH}	OE	Y	C_L = 15pF	2.5V		10.4	19.8	ns
t_{PZL}	OE	Y	C_L = 15pF	2.5V		9.9	19.0	ns
t_{PHL}	A	Y	C_L = 50pF	2.5V		13.5	25.4	ns
t_{PLH}	A	Y	C_L = 50pF	2.5V		10.1	25.4	ns
t_{PHZ}	OE	Y	C_L = 50pF	2.5V		13.1	18.5	ns
t_{PLZ}	OE	Y	C_L = 50pF	2.5V		12.0	16.4	ns
t_{PZH}	OE	Y	C_L = 50pF	2.5V		12.0	22.5	ns
t_{PZL}	OE	Y	C_L = 50pF	2.5V		11.1	21.5	ns
t_{PHL}	A	Y	C_L = 15pF	3.3V		7.9	15.2	ns
t_{PLH}	A	Y	C_L = 15pF	3.3V		5.4	13.8	ns
t_{PHZ}	OE	Y	C_L = 15pF	3.3V		6.0	9.9	ns
t_{PLZ}	OE	Y	C_L = 15pF	3.3V		5.3	8.2	ns
t_{PZH}	OE	Y	C_L = 15pF	3.3V		7.9	14.1	ns
t_{PZL}	OE	Y	C_L = 15pF	3.3V		7.4	13.5	ns
t_{PHL}	A	Y	C_L = 50pF	3.3V		10.2	18.3	ns
t_{PLH}	A	Y	C_L = 50pF	3.3V		7.8	16.0	ns
t_{PHZ}	OE	Y	C_L = 50pF	3.3V		9.7	15.1	ns
t_{PLZ}	OE	Y	C_L = 50pF	3.3V		9.2	12.9	ns
t_{PZH}	OE	Y	C_L = 50pF	3.3V		9.1	16.4	ns
t_{PZL}	OE	Y	C_L = 50pF	3.3V		8.3	15.3	ns
tsk(o)	OE	Y	C_L = 50pF	3.3V			1.5	ns
t_{PHL}	A	Y	C_L = 15pF	5V		5.3	10.2	ns
t_{PLH}	A	Y	C_L = 15pF	5V		4.2	9.9	ns
t_{PHZ}	OE	Y	C_L = 15pF	5V		4.6	7.5	ns
t_{PLZ}	OE	Y	C_L = 15pF	5V		4.2	6.1	ns
t_{PZH}	OE	Y	C_L = 15pF	5V		5.6	9.6	ns
t_{PZL}	OE	Y	C_L = 15pF	5V		5.1	8.9	ns

Copyright © 2024 Texas Instruments Incorporated

6.6 Switching Characteristics (continued)

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	MIN	TYP	MAX	UNIT
t_{PHL}	A	Y	C_L = 50pF	5V		7.1	12.5	ns
t_{PLH}	A	Y	C_L = 50pF	5V		5.8	11.5	ns
t_{PHZ}	OE	Y	C_L = 50pF	5V		6.9	10.9	ns
t_{PLZ}	OE	Y	C_L = 50pF	5V		6.8	9.1	ns
t_{PZH}	OE	Y	C_L = 50pF	5V		6.6	11.0	ns
t_{PZL}	OE	Y	C_L = 50pF	5V		5.7	10.0	ns

6.7 Noise Characteristics

VCC = 5V, CL = 50pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	5		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

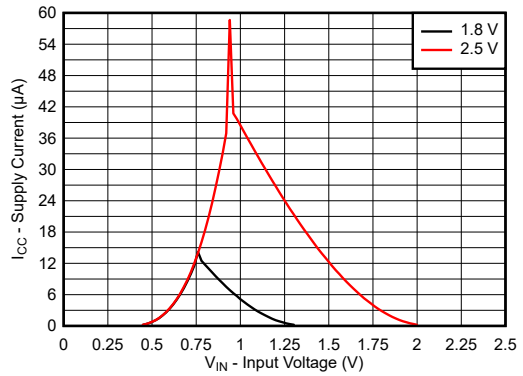


Figure 6-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

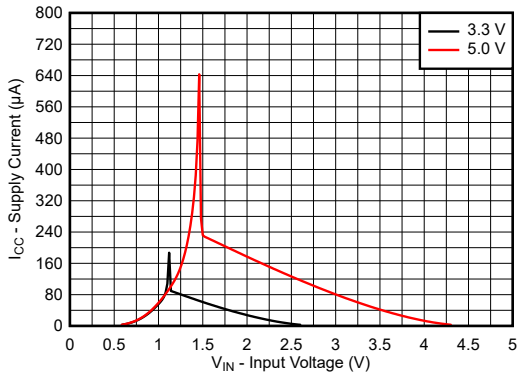


Figure 6-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

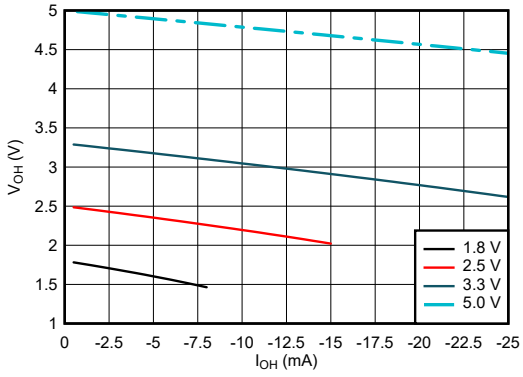


Figure 6-3. Output Voltage vs Current in HIGH State

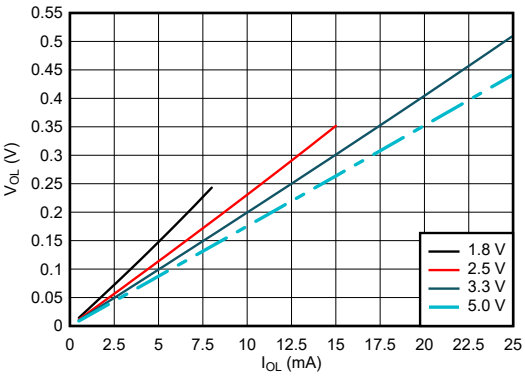


Figure 6-4. Output Voltage vs Current in LOW State

Copyright © 2024 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

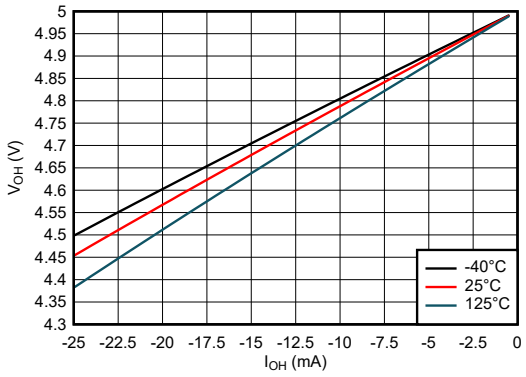


Figure 6-5. Output Voltage vs Current in HIGH State; 5V Supply

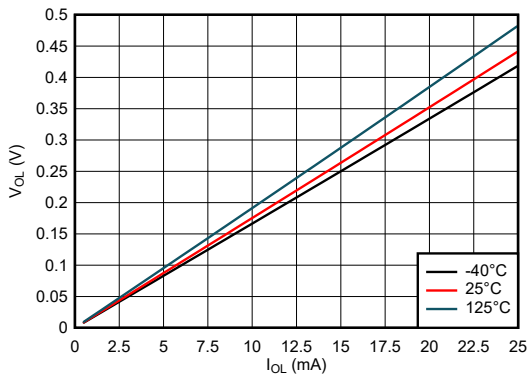


Figure 6-6. Output Voltage vs Current in LOW State; 5V Supply

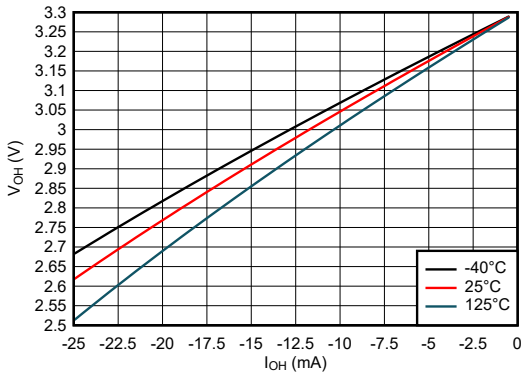


Figure 6-7. Output Voltage vs Current in HIGH State; 3.3V Supply

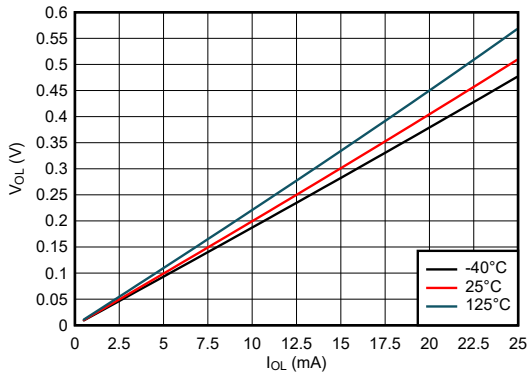


Figure 6-8. Output Voltage vs Current in LOW State; 3.3V Supply

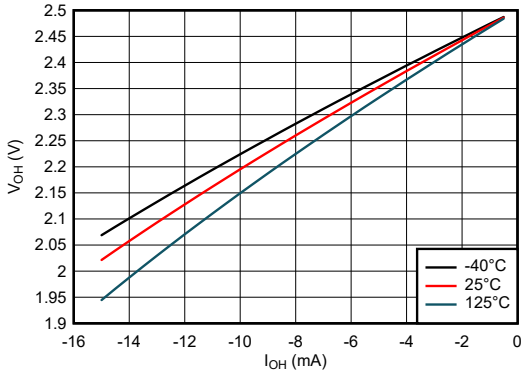


Figure 6-9. Output Voltage vs Current in HIGH State; 2.5V Supply

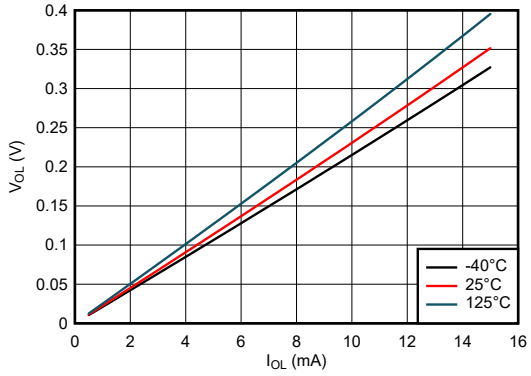


Figure 6-10. Output Voltage vs Current in LOW State; 2.5V Supply

Copyright © 2024 Texas Instruments Incorporated

6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

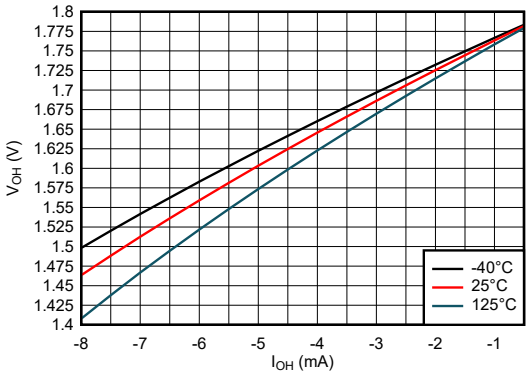


Figure 6-11. Output Voltage vs Current in HIGH State; 1.8V Supply

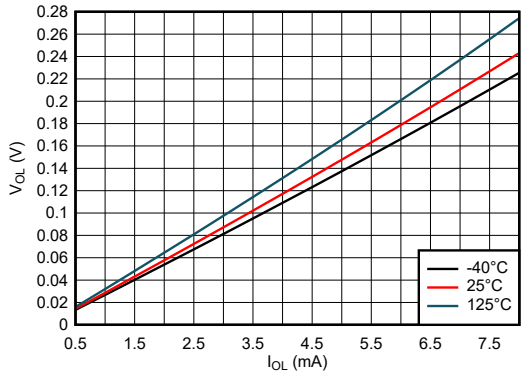
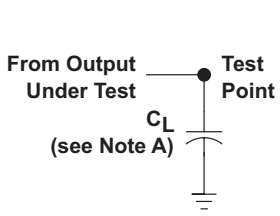


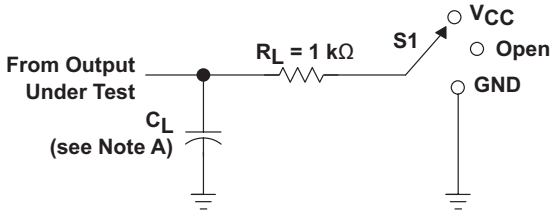
Figure 6-12. Output Voltage vs Current in LOW State; 1.8V Supply

Copyright © 2024 Texas Instruments Incorporated

7 Parameter Measurement Information

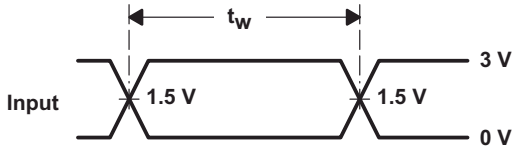


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

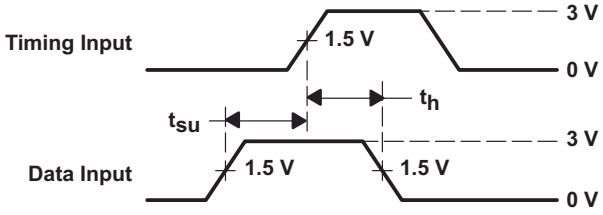


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

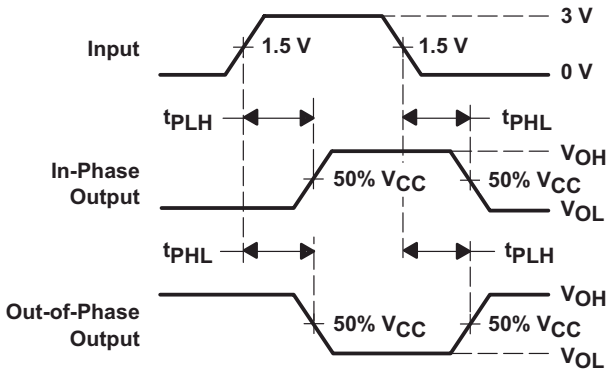
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



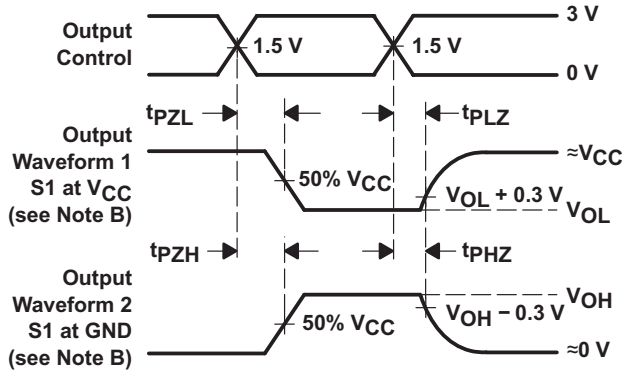
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

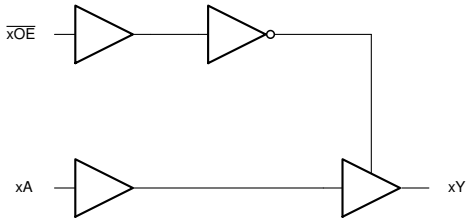
Copyright © 2024 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74LV4T125-EP contains four independent buffers with 3-state outputs and extended voltage operation to allow for level translation. Each buffer performs the Boolean function Y = A in positive logic. The outputs can be put into a Hi-Z state by applying a High on the $\overline{OE}$ pin. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as depicted in Figure 8-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Copyright © 2024 Texas Instruments Incorporated

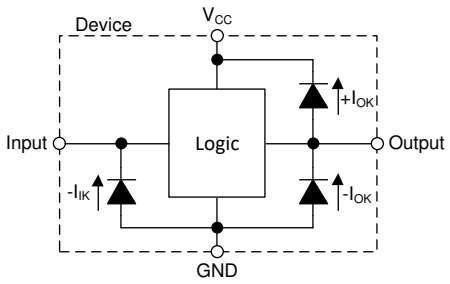


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.3 LVxT Enhanced Input Voltage

The SN74LV4T125-EP belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 8-2 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

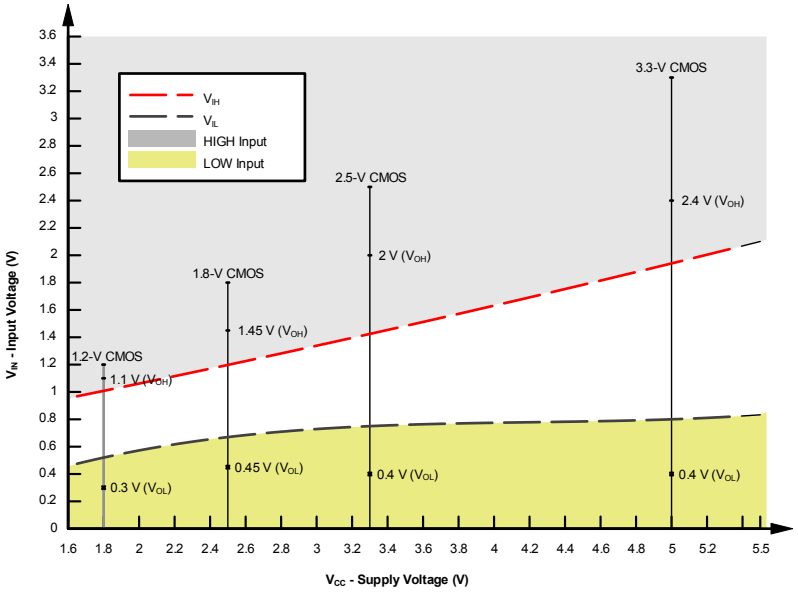


Figure 8-2. LVxT Input Voltage Levels

Copyright © 2024 Texas Instruments Incorporated

8.3.3.1 Down Translation

Signals can be translated down using the SN74LV4T125-EP. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 8-2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V V_{CC}. See Figure 8-3.

Down Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V V_{CC} – Inputs from 3.3V and 5.0V
- 3.3V V_{CC} – Inputs from 5.0V

8.3.3.2 Up Translation

Input signals can be up translated using the SN74LV4T125-EP. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a $V_{IH(MIN)}$ of 3.5V. For the SN74LV4T125-EP, $V_{IH(MIN)}$ with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

As shown in Figure 8-3, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 1.2V
- 2.5V V_{CC} – Inputs from 1.8V
- 3.3V V_{CC} – Inputs from 1.8V and 2.5V
- 5.0V V_{CC} – Inputs from 2.5V and 3.3V

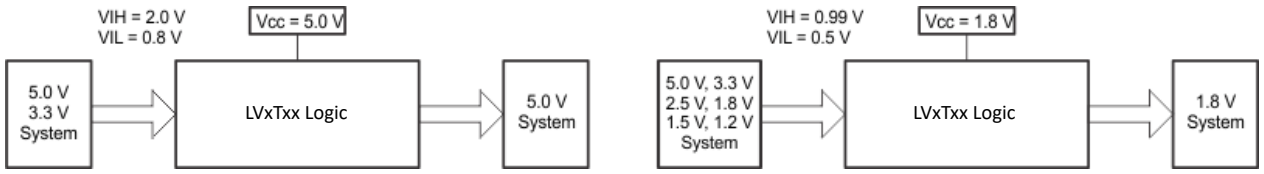


Figure 8-3. LVxT Up and Down Translation Example

Copyright © 2024 Texas Instruments Incorporated

8.4 Device Functional Modes

Function Table lists the functional modes of the SN74LV4T125-EP.

Table 8-1. Function Table

INPUTS(1)		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

Copyright © 2024 Texas Instruments Incorporated

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, a buffer with a 3-state output is used to disable a data signal as shown in Figure 9-1. The remaining three buffers can be used for signal conditioning in other places in the system, or the inputs can be grounded and the channels left unused.

9.2 Typical Application

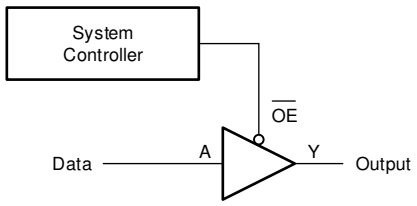


Figure 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. The input threshold levels are lowered to allow for up translation. At 5V the device has equivalent TTL input levels.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV4T125-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. Doing this will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.3 Application Curves

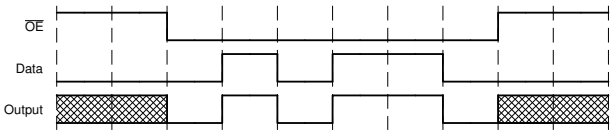


Figure 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF is recommended. If there are multiple V_{CC} pins, then 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 9-3 are the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

9.4.2 Layout Example

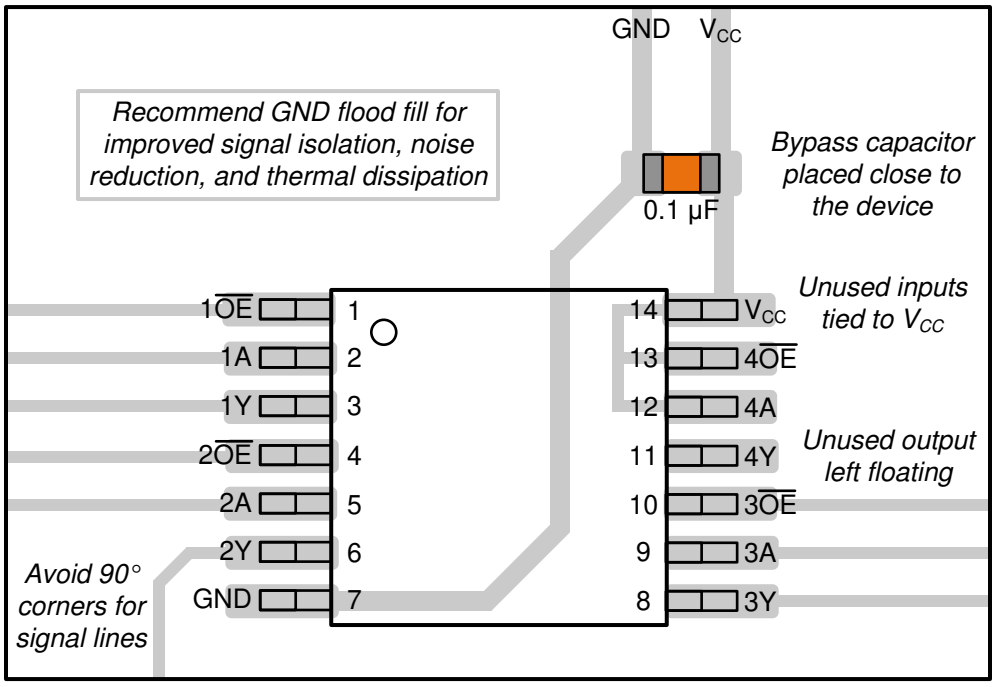


Figure 9-3. Example Layout for the SN74LV4T125-EP

Copyright © 2024 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVSION	NOTES
January 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4T125PWREP	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	L4125EP
SN74LV4T125PWREP.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	L4125EP
V62/24608-01XE	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	L4125EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4T125-EP :

- Catalog : SN74LV4T125

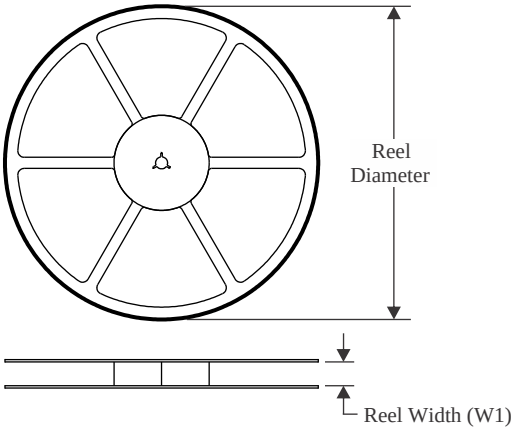
- Automotive : SN74LV4T125-Q1

NOTE: Qualified Version Definitions:

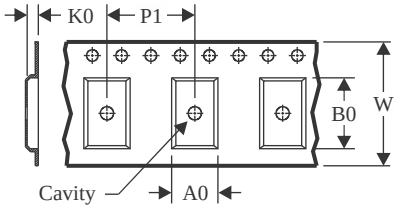
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

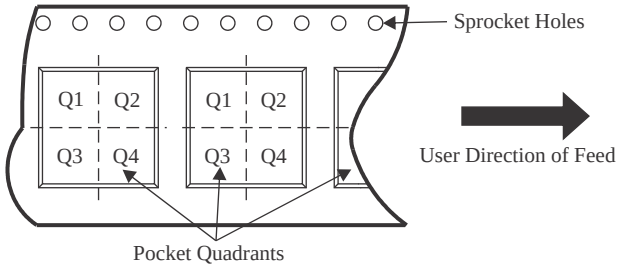


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

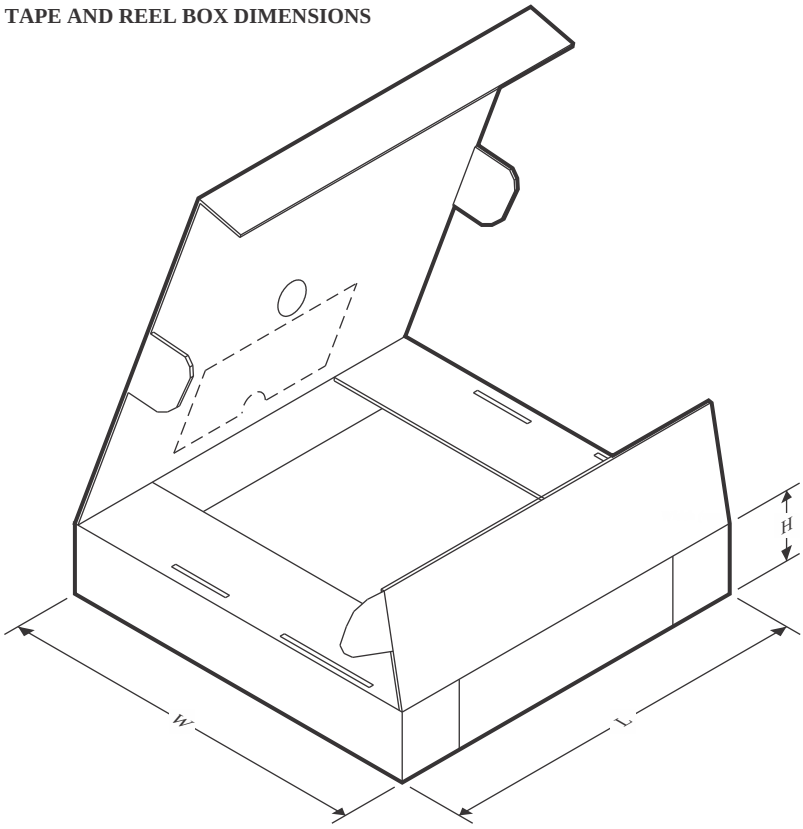
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4T125PWREP	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

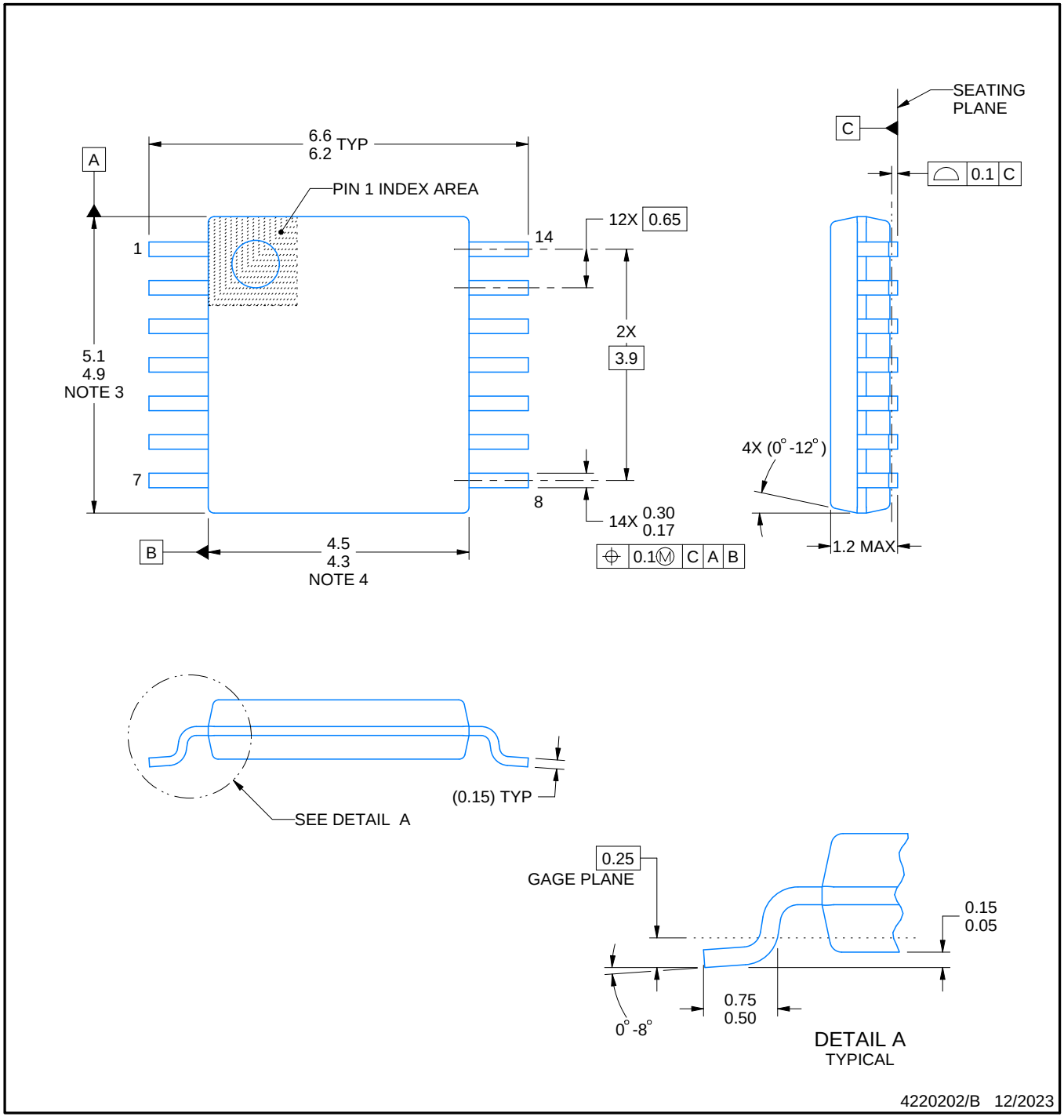
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4T125PWREP	TSSOP	PW	14	3000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0014A

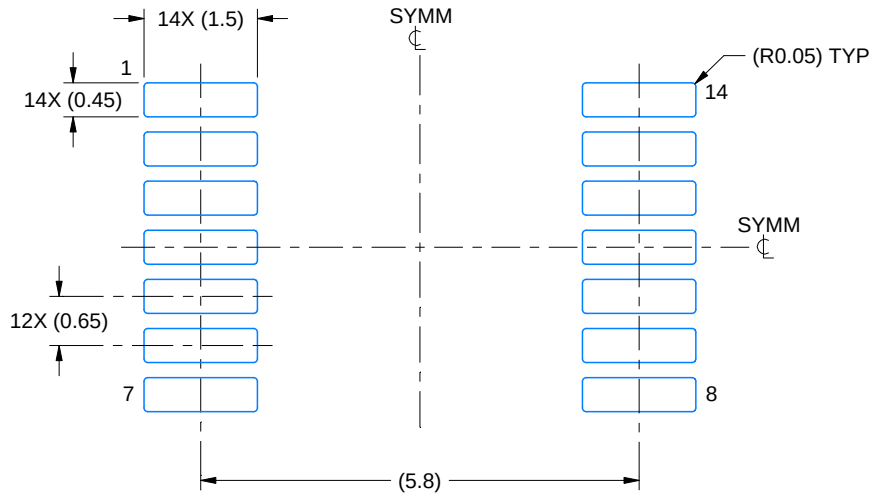
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

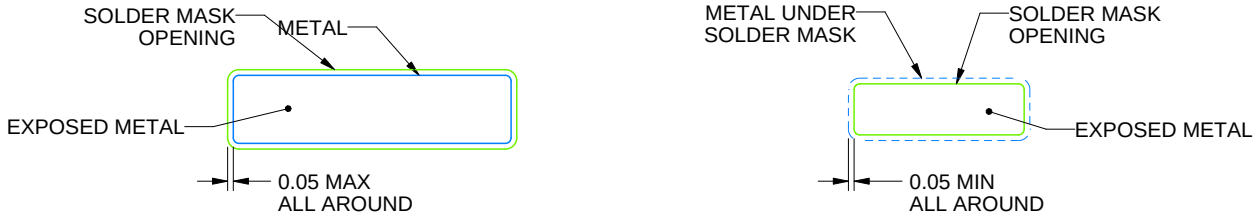


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

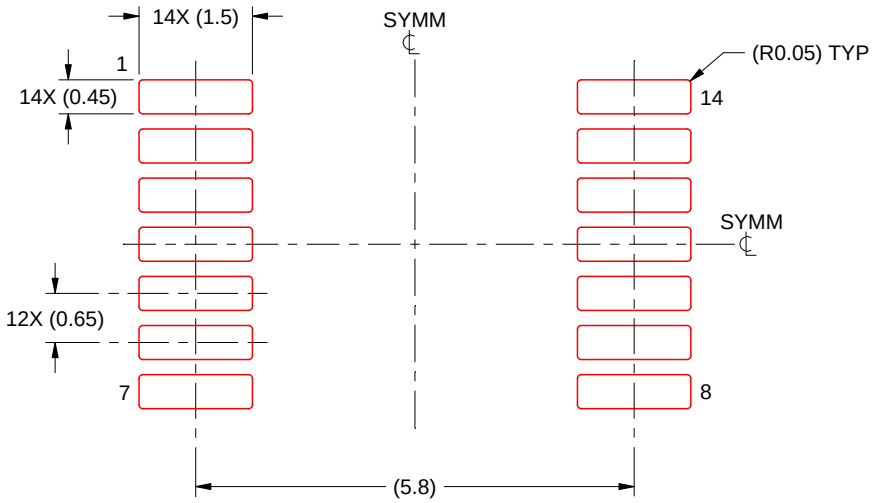


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated