DATA SHEET

CLA4609-086LF: Surface-Mount Limiter Diode

Applications

- Low-loss, high-power limiters
- Receiver protectors

Features

- Low thermal resistance: 25 °C/W
- Typical threshold level: +36 dBm
- Low capacitance: 0.6 pF
- Low-profile, ultra-miniature QFN (3-pin, 2 x 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

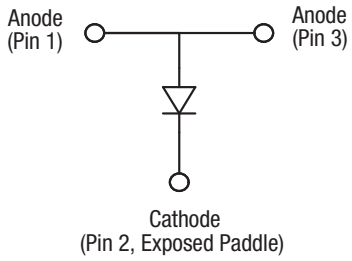


Figure 1. CLA4609-086LF Block Diagram

Description

The CLA4609-086LF is a surface-mountable, low-capacitance, dual parallel, shunt-connected, PIN limiter diode for high power applications from 10 MHz to 6 GHz.

Maximum resistance at 100 mA is 1.5 Ω and maximum capacitance at 30 V is 0.6 pF. The combination of low junction capacitance, low parasitic inductance, low thermal resistance, and nominal 20 um I-region width, makes the CLA4609-086LF useful in large signal limiter applications. The threshold level is +36 dBm, typical.

A block diagram of the CLA4609-086LF is shown in Figure 1.

Electrical and Mechanical Specifications

The absolute maximum ratings of the CLA4609-086LF are provided in Table 1. Electrical specifications are provided in Table 2, and typical RF performance at T = 25 °C is shown in Table 3.

Typical performance characteristics are shown in Figure 2.

Figure 3 shows the power de-rating curve for the limiter. The temperature is referenced to the bottom of the package.

Table 1. CLA4609-086LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
Reverse voltage	V_R		250	V
Forward current @ 25 °C	I_F		1.5	A
CW power dissipation @ 85 °C	P_D		2.5	W
Peak pulse power dissipation @ 85 °C (10% duty cycle)			25	W
Storage temperature	T_{STG}	-65	+200	°C
Junction temperature	T_J		175	°C
Operating temperature	T_A	-55	+150	°C

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 2. CLA4609-086LF Electrical Specifications[1]
(T_A = +25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reverse current	I_R	V_R = 250 V			10	uA
Capacitance	C_T	f = 1 MHz, V_R = 30 V			0.6	pF
Series inductance	L_S			0.3		nH
Resistance	R_S	f = 500 MHz, I_F = 10 mA			1.5	Ω
Carrier lifetime	T_L	I_F = 10 mA		1.1		us
I region width	W			20		um
CW thermal resistance	θ_{JC}	Junction-to-case		25		°C/W
Peak thermal resistance	θ_P	Single 0.1 us pulse width, junction-to-case (0.1% duty cycle)		0.1		°C/W

1 Performance is guaranteed only under the conditions listed in this table.

Table 3. Typical Performance @ 25 °C

Part Number	Insertion Loss @ -10 dBm (dB)	Input Power for 1 dB Loss (dBm)	Maximum CW Input power (W)	Maximum Pulsed Input Power (dBm)	Output @ Maximum Pulsed Input (dBm)	Recovery Time (ns)
CLA4609-086LF	0.3	+36	16 (42 dBm)	+72	+52	5

Notes:
Insertion loss for CLA4609-086LF @ 2.3 GHz.
Limiter power results @ 2.3 GHz for shunt connected, single limiter diode and DC return in 50 Ω line.
Pulsed power measurements taken at 0.1 us pulse width, pulse frequency = 10 kHz, and 0.1% duty cycle.
Maximum CW input power @ 25 °C heat sink. Derate linearly to 0 W @ 175 °C.
Recovery time represents the transition time from the high-loss state to the low-loss state following the removal of a high-power input. It is defined as the time from the end of the high-power pulse to the time when insertion loss has returned to within 3 dB of the quiescent (low power) state.

Typical Performance Characteristics (TA = 25 °C, Unless Otherwise Noted)

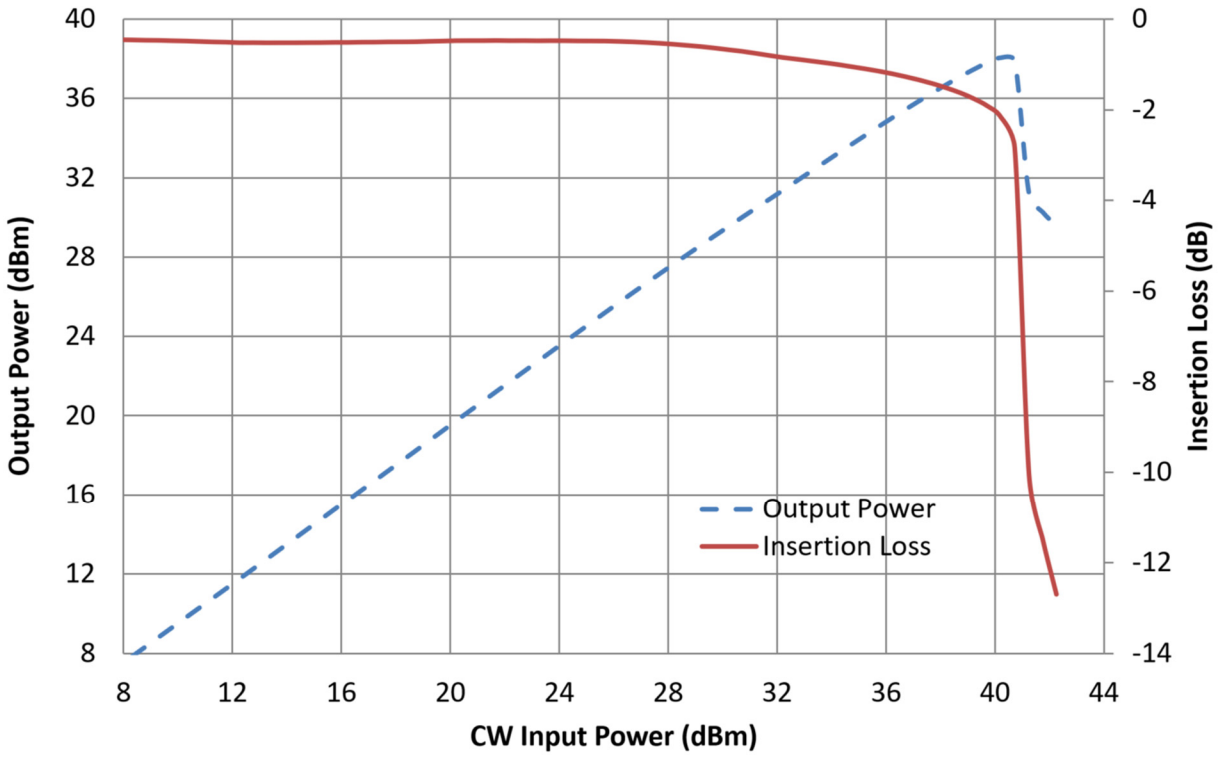


Figure 2. Output Power and Insertion Loss vs Input Power (f = 2.3 GHz)

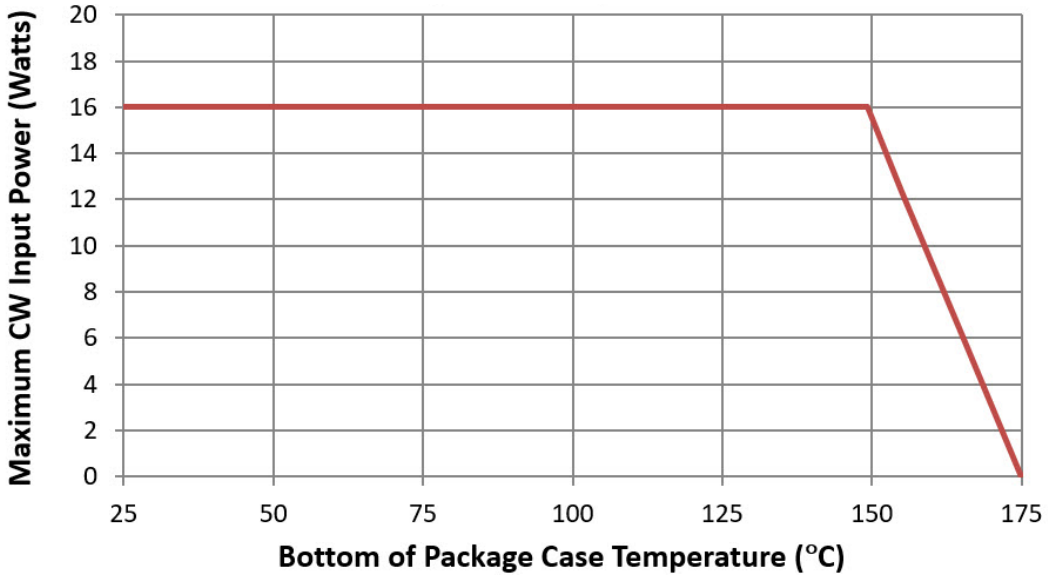


Figure 3. CLA4609-086LF Max CW Power In vs Bottom of Package Case Temperature

Functional Description

The PIN limiter diode can be described as an incident power controlled, RF variable resistor. When there is no large input signal present, the impedance of the limiter diode is at its maximum, which produces minimum insertion loss, typically less than 0.3 dB. The presence of a large input signal temporarily forces the impedance of the diode to a much lower value, which produces an impedance mismatch that reflects most of the input signal power back towards its source.

During the limiting process, a DC current is generated by the PIN limiter diode. The current is not the result of rectification, but is the result of charge carriers being forced into the I layer by the forward alternations of the large input signal. A complete path must be provided for this current or the diode is not capable of limiting. Therefore, an RF choke or similar structure must be provided to complete the path for DC current flow.

The DC block capacitors shown in Figure 4 are optional; they protect the limiter diode from external DC voltage that may be present in the source or load circuits.

A cross section of the suggested printed circuit board design is shown in Figure 5. The via shown in this view is critical, both for electrical performance and for thermal performance. It is recommended that several vias should be placed under the entire footprint of the exposed paddle (pin 2) to minimize both electrical inductance to the system ground and thermal resistance to the system heat sink.

For more information about the operation of limiter diodes, refer to the Skyworks Application Note, *PIN Limiter Diodes in Receiver Protectors*, document number 200480.

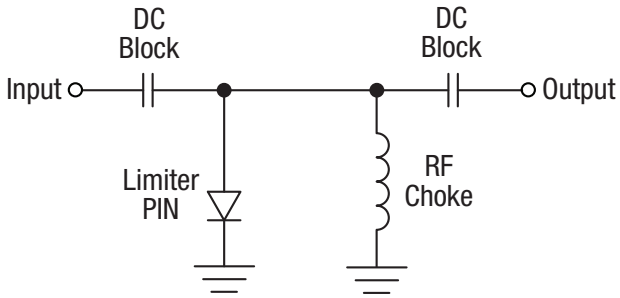


Figure 4. Single Stage Limiter Circuit

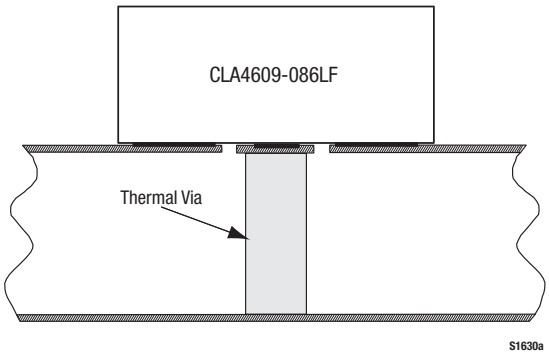


Figure 5. Cross-Section View of Suggested Printed Circuit Board

High-Power Limiter Design Application

The CLA4609-086LF PIN limiter diode is designed for shunt applications in receiver protection power limiter circuits. Compared to other surface mount packages, the design of the QFN package produces lower thermal resistance and reduces the effects of the parasitic inductance of the anode bond wires.

A cross-sectional view of the CLA4609-086LF PIN limiter diode is shown below. The cathode of the die is soldered directly to the top of the exposed paddle. This paddle is composed of copper, so its thermal resistance is very low.

The copper ground paddle minimizes the total thermal resistance between the I layer, which is the location where most heat is generated under normal operation, and the surface to which the package is mounted. Minimal thermal resistance between the I layer and the external environment minimizes junction temperature.

The electrically equivalent circuit of the CLA4609-086LF PIN limiter diode is shown in Figure 7. The inductances of pins 1 and 2, as well as the inductances of the bond wires are in series with the input and output transmission lines of the external circuit rather than the portion of the circuit that contains the shunt PIN limiter diode.

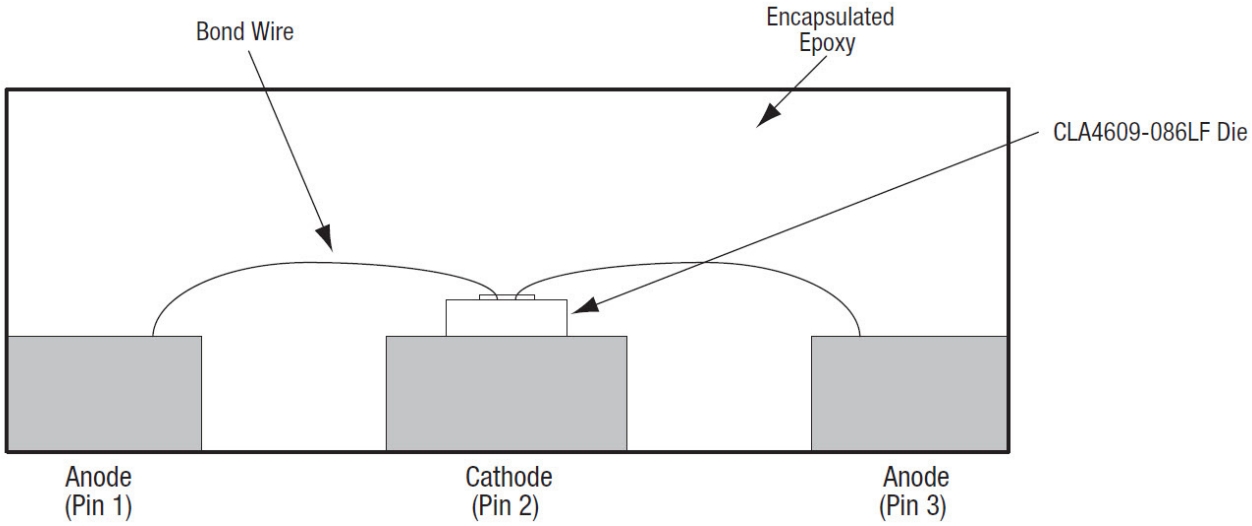


Figure 6. Cross-Section View of the CLA4609-086LF

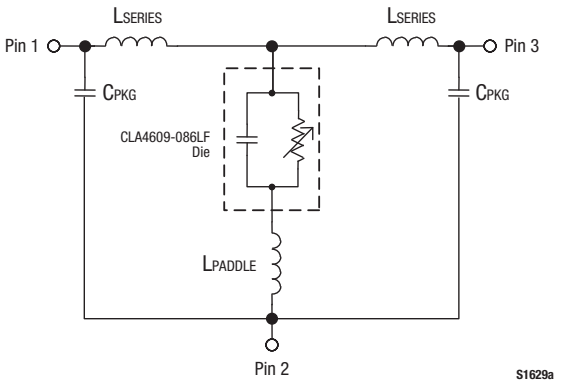


Figure 7. CLA4609-086LF Electrically Equivalent Circuit

Package Dimensions

The PCB layout footprint for the CLA4609-086LF is shown in Figure 8. Typical part markings are shown in Figure 9. Package dimensions are provided in Figure 10, and Figure 11 provides the tape and reel dimensions.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CLA4609-086LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

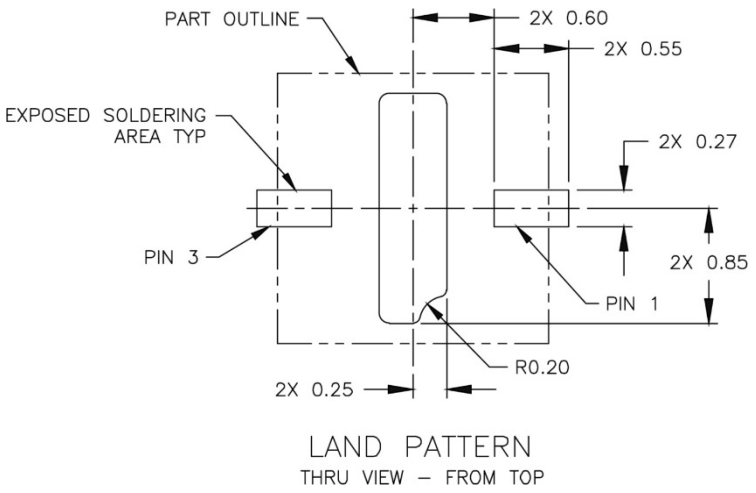


Figure 8. CLA4609-086LF PCB Layout Footprint

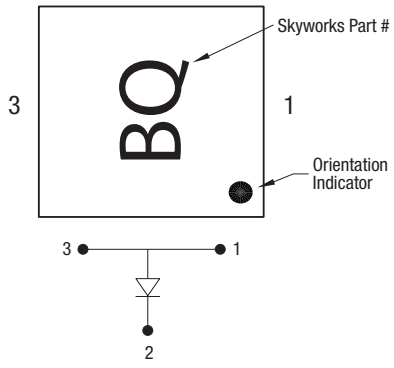
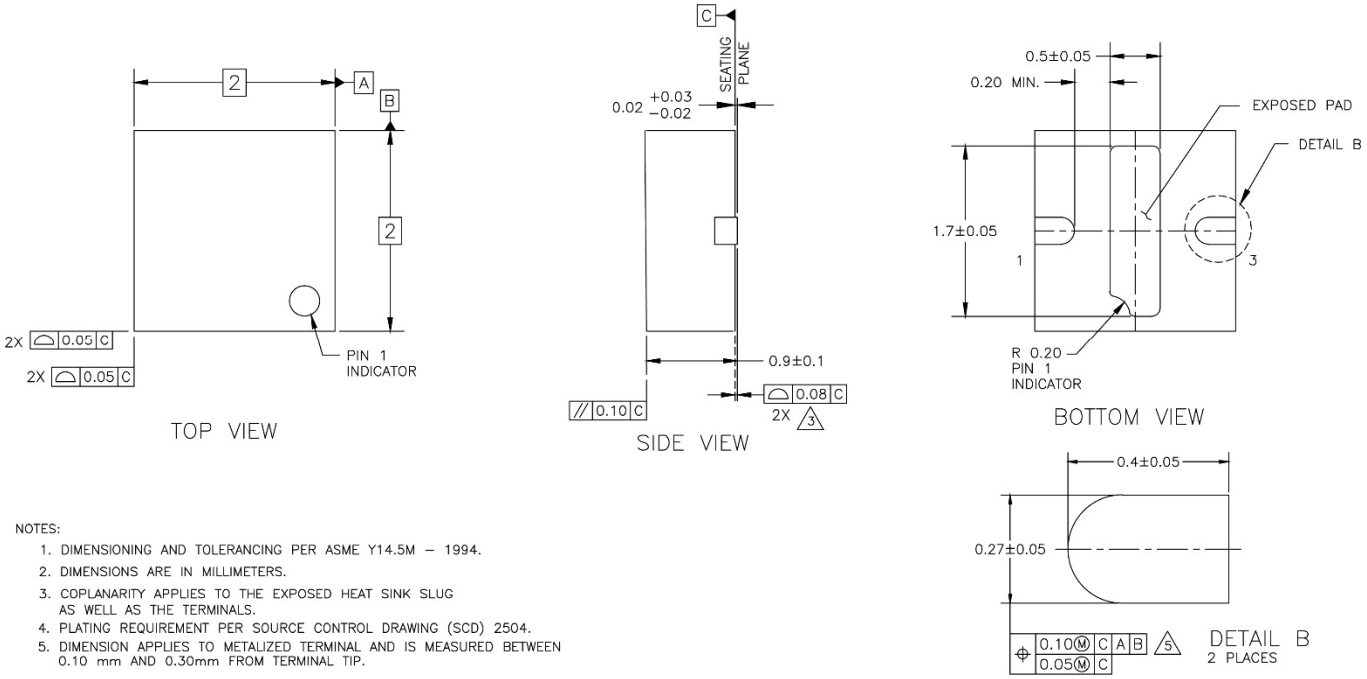


Figure 9. Typical Part Markings (Top View)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. PLATING REQUIREMENT PER SOURCE CONTROL DRAWING (SCD) 2504.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.10 mm AND 0.30mm FROM TERMINAL TIP.

Figure 10. CLA4609-086LF Package Dimensions

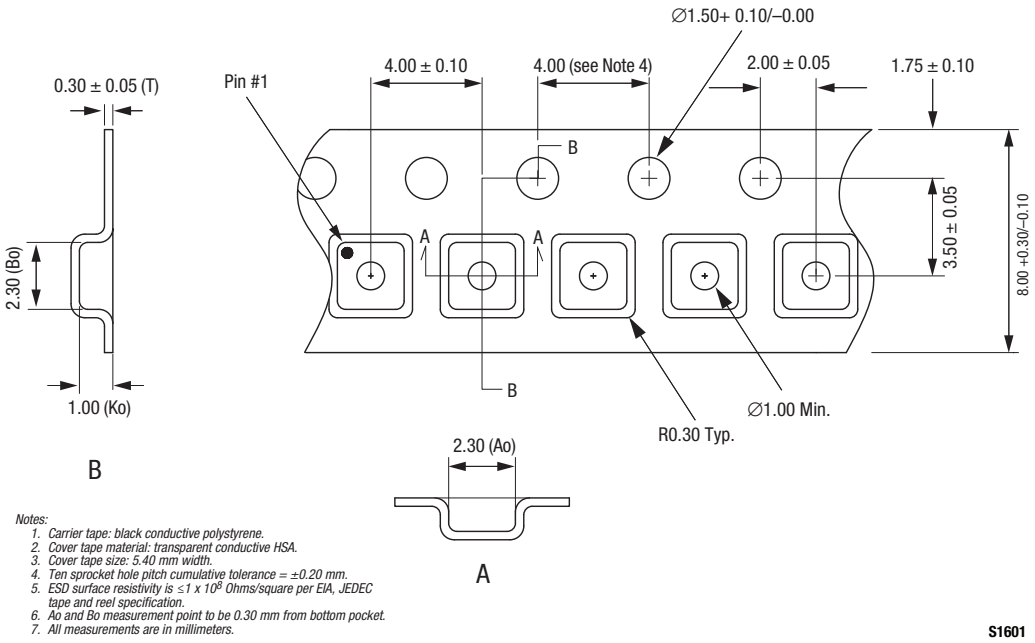


Figure 11. CLA4609-086LF Tape and Reel Dimensions

Ordering Information

Part Number	Product Description	Evaluation Board Part Number
CLA4609-086LF	Surface-Mount Limiter Diode	CLA4609-86-EVB