1.Description

The AD8606 dual rail-to-rail input and output, single supply amplifiers. They feature very low offset voltage, low input voltage and current noise, and wide signal bandwidth.

The combination of low offsets, low noise, very low input bias currents, and high speed makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for these amplifiers include optical control loops, portable and loop-powered instrumentation,and audio amplification for portable devices.

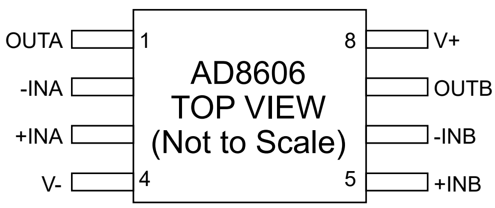
2.Features

- Low offset voltage: 65 μV maximum
- Low input bias currents: 1 pA maximum
- Low noise: 8 nV/√Hz
- Wide bandwidth: 10 MHZ
- High open-loop gain: 1000 V/mV
- Unity gain stable
- Single-supply operation: 2.7 V to 5.5 V
- 8-ball WLCSP for dual (AD8606)

3.Applications

- Photodiode amplification
- Battery-powered
- instrumentation Multipole
- filters
- Sensors
- Barcode scanners
- Audio

4.Pinning information



SOP-8

5.Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	6V
Input Voltage	GND to V_S
Differential input Voltage	6V
Qutput Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	
All Packages	−65°C to +150°C
Operating Temperature Range	
All Packages	−40°C to +125°C
Junction Temperature Range	
All Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

6.1Electrical Characteristics

V_S=5V, V_{CM}=V_S/2, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_S=3.5V, V_{CM}=3V		20	65	μV
		V_S=5V, V_{CM}=0V to 5V		80	300	μV
		−40°C<T_A<+125°C			750	μV
Input Bias Current	I_B			0.2	1	pA
		−40°C<T_A<+85°C			50	pA
		−40°C<T_A<+125°C			250	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C<T_A<+85°C			20	pA
		−40°C<T_A<+125°C			75	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V to 5V	85	100		dB
		−40°C<T_A<+125°C	75	90		dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ, V_O=0.5V to 4.5V	300	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C<T_A<+125°C		1	4.5	μV/°C
OUTPUT CHARACTERISTICS						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L=1mA	4.96	4.98		V
		I_L=10mA	4.7	4.79		V
		−40°C<T_A<+125°C	4.6			V
Output Voltage Low	V_{OL}	I_L=1mA		20	40	mV
		I_L=10mA		170	210	mV
		−40°C<T_A<+125°C			290	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Current	I_{OUT}			±80		mA
Closed-Loop Output Impedance	Z_{OUT}	f=1MHz, A_V=1		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S=2.7V to 5.5V	80	95		dB
		V_S=2.7V to 5.5V	75	92		dB
Supply Current/Amplifier	I_{SY}	−40°C<T_A<+125°C	70	90		dB
		I_{OUT}=0mA		1	1.2	mA
		−40°C<T_A<+125°C			1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L=2kΩ, C_L=16pF		5		V/μs
Settling Time	tS	To 0.01%,0V to 2V step,A_V=1		<1		μs
Unity Gain Bandwidth Product	GBP			10		MHz
Phase Margin	ΦM			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_np-p	f=0.1Hz to 10Hz		2.3	3.5	μVp-p
Voltage Noise Density	e_n	f=1kHz		8	12	nV/√Hz
		f=10kHz		6.5		nV/√Hz
Current Noise Density	i_n	f=1kHz		0.01		pA/√Hz

6.2Electrical Characteristics

V_S=2.7V, V_{CM}=V_S/2, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_S=3.5V, V_{CM}=3V		20	65	μV
		V_S=2.7V, V_{CM}=0V to 2.7V		80	300	μV
		−40°C<T_A<+125°C			750	μV
Input Bias Current	I_B			0.2	1	pA
		−40°C<T_A<+85°C			50	pA
		−40°C<T_A<+125°C			250	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C<T_A<+85°C			20	pA
		−40°C<T_A<+125°C			75	pA
Input Voltage Range	CMRR		0		2.7	V
Common-Mode Rejection Ratio		V_{CM}=0V to 2.7V	80	95		dB
		−40°C<T_A<+125°C	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ, V_O=0.5V to 2.2V	110	350		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C<T_A<+125°C		1	4.5	μV/°C
OUTPUT CHARACTERISTICS						
Common-Mode Input Capacitance	C_{COM}			8.8		pF
Differential Input Capacitance	C_{DIFF}			2.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L=1mA	2.6	2.66		V
		−40°C<T_A<+125°C	2.6			V
Output Voltage Low	V_{OL}	I_L=1mA		25	40	V
		−40°C<T_A<+125°C			50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Current	I_{OUT}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f=1MHz, A_V=1		1.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S=2.7V to 5.5V	80	95		dB
		V_S=2.7V to 5.5V	75	92		dB
Supply Current/Amplifier	I_{SY}	−40°C<T_A<+125°C	70	90		dB
		I_{OUT}=0mA		1.15	1.4	mA
		−40°C<T_A<+125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L=2kΩ, C_L=16pF		5		V/μs
Settling Time	tS	To 0.01%,0V to 2V step,A_V=1		<0.5		μs
Unity Gain Bandwidth Product	GBP			9		MHz
Phase Margin	ΦM			50		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_np-p	f=0.1Hz to 10Hz		2.3	3.5	μVp-p
Voltage Noise Density	e_n	f=1kHz		8	12	nV/√Hz
		f=10kHz		6.5		nV/√Hz
Current Noise Density	i_n	f=1kHz		0.01		pA/√Hz

7.1Typical Characteristic

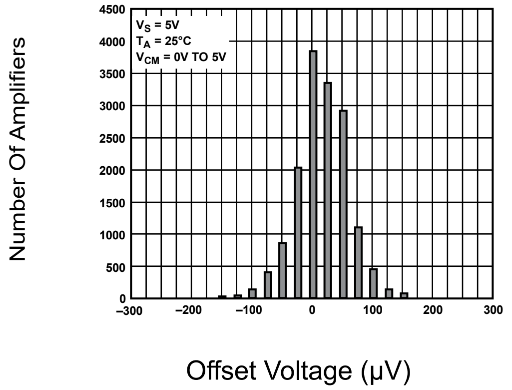


Figure 1: Input Offset Voltage Distribution

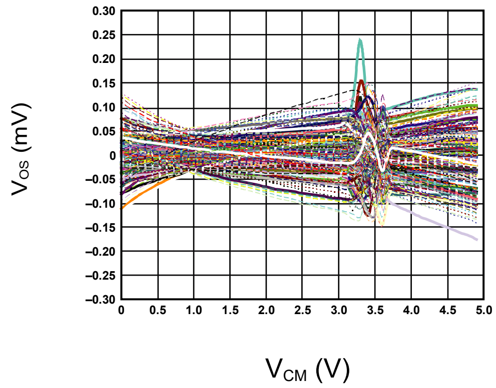


Figure 2: Input Offset Voltage vs.Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

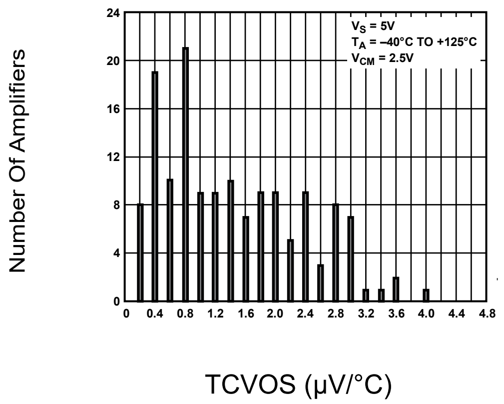


Figure 3: AD8608 Input Offset Voltage Drift Distribution

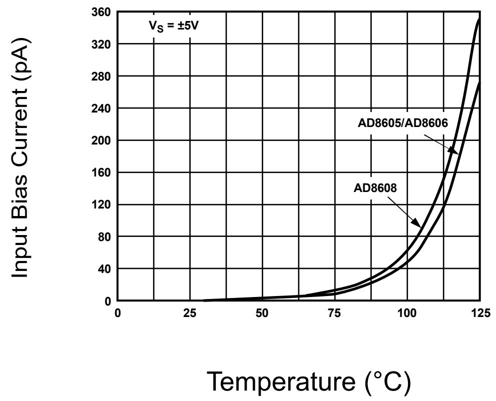


Figure 4: Input Bias Current vs. Temperature

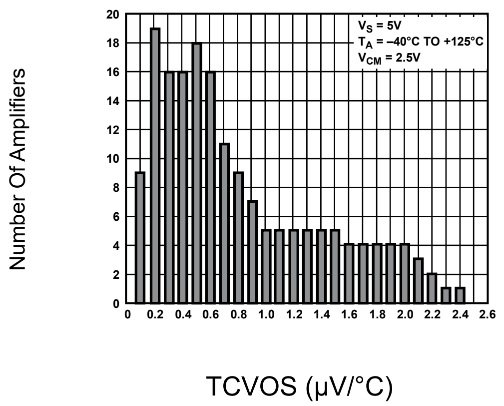


Figure 5: D8606 Input Offset Voltage Drift Distribution

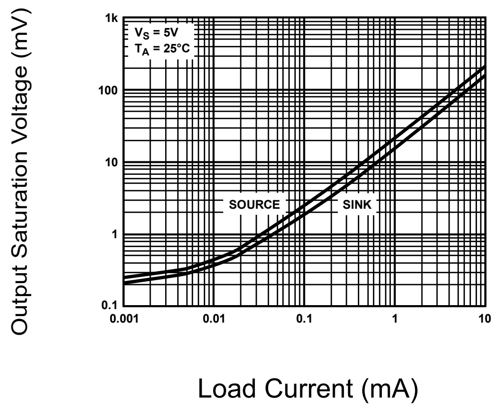


Figure 6: Output Saturation Voltage vs. Load Current

7.2Typical Characteristic

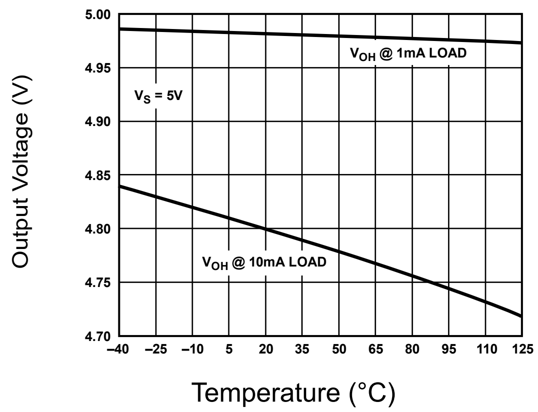


Figure 7: Output Voltage Swing High vs. Temperature

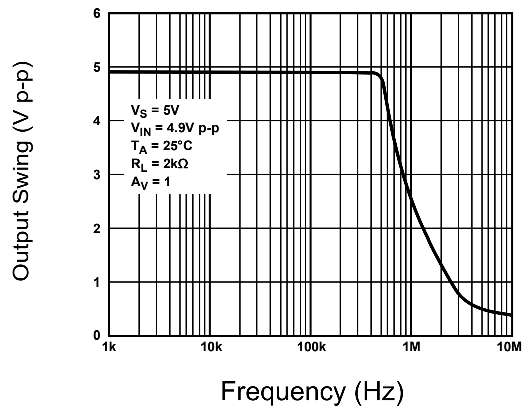


Figure 8: Closed-Loop Output Voltage Swing (FPBW)

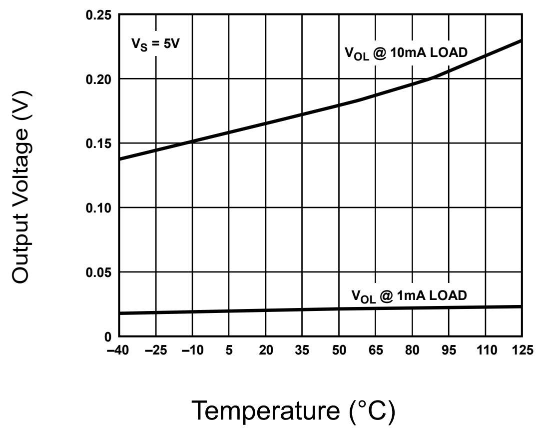


Figure 9: Output Voltage Swing Low vs. Temperature

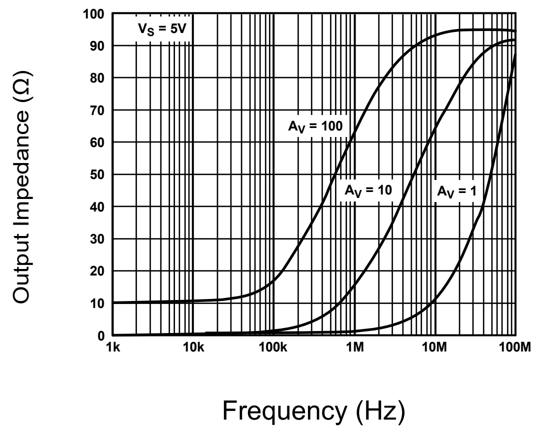


Figure 10: Output Impedance vs. Frequency

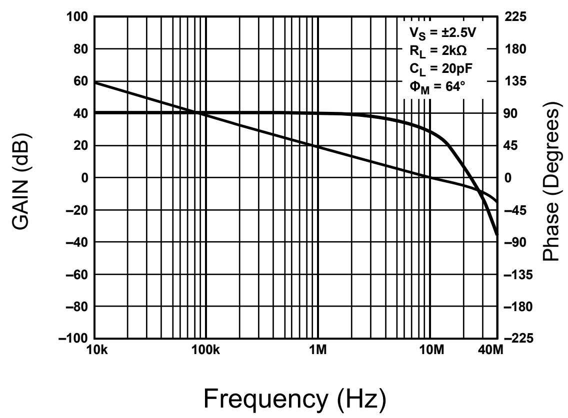


Figure 11: Open-Loop Gain and Phase vs. Frequency

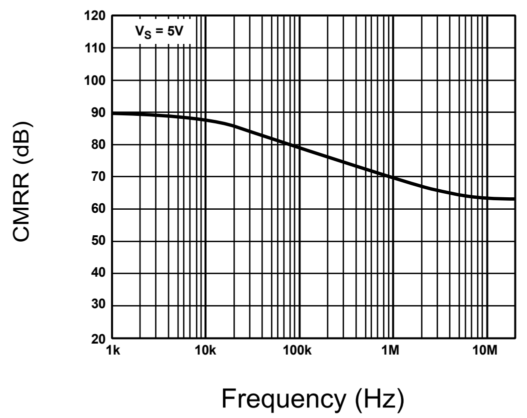


Figure 12: Common-Mode Rejection Ratio (CMRR) vs. Frequency

7.3Typical Characteristic

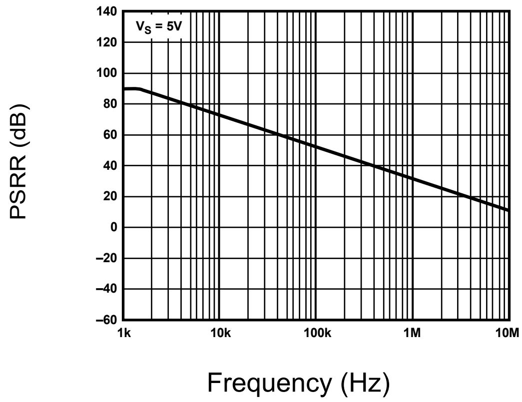


Figure 13: PSRR vs. Frequency

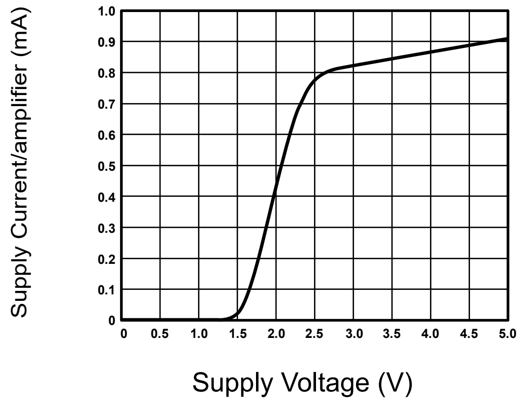


Figure 14: Supply Current/Amplifier vs. Supply Voltage

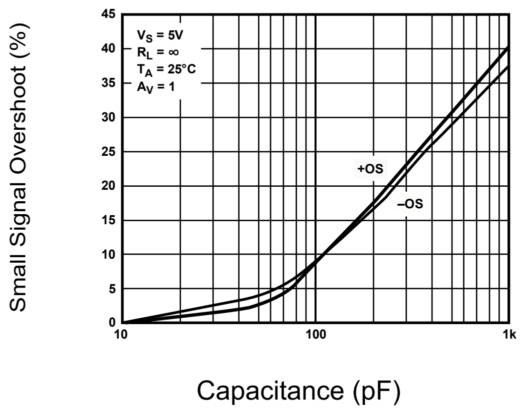


Figure 15: Small Signal Overshoot vs. Load Capacitance

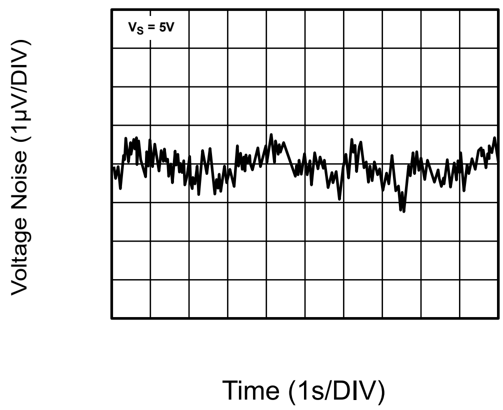


Figure 16: 0.1 Hz to 10 Hz Input Voltage Noise

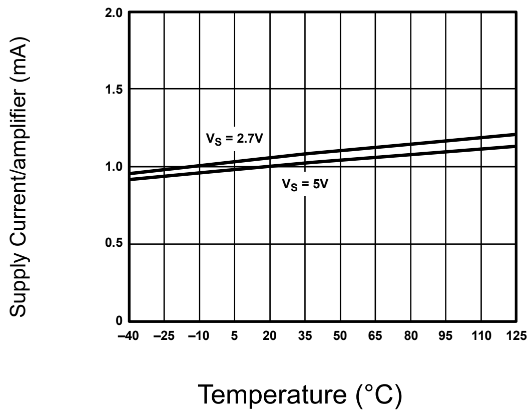


Figure 17: Supply Current/Amplifier vs. Temperature

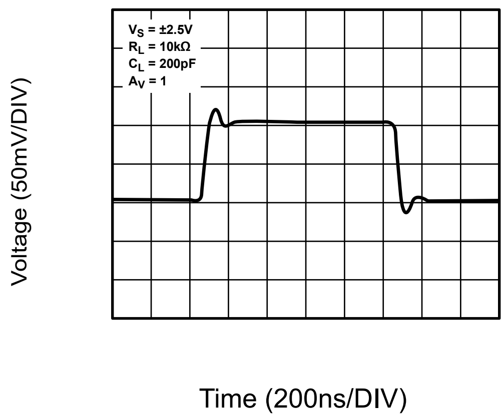


Figure 18: Small Signal Transient Response

7.4Typical Characteristic

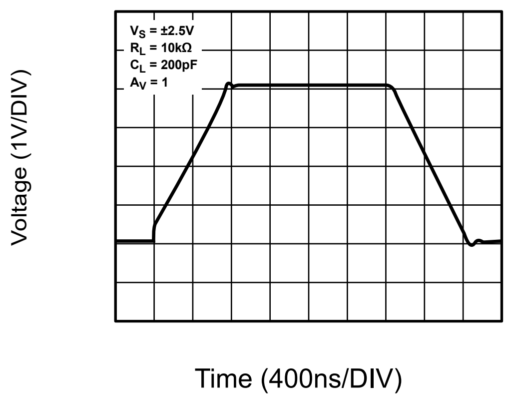


Figure 19: Large Signal Transient Response

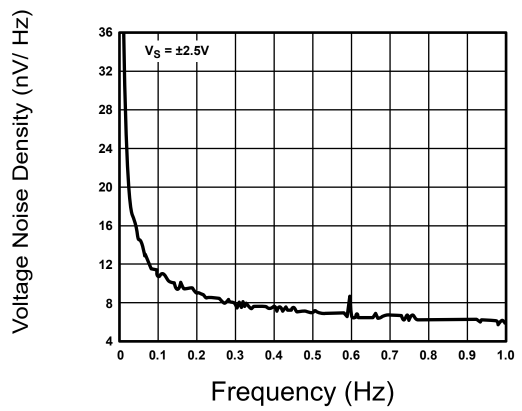


Figure 20: Voltage Noise Density vs. Frequency

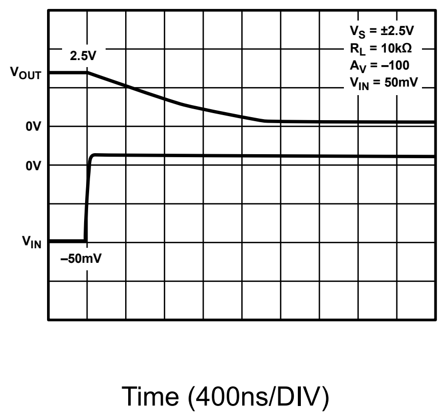


Figure 21: Positive Overload Recovery

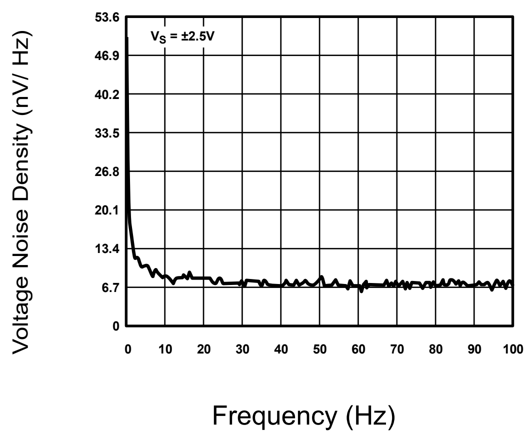


Figure 22: Voltage Noise Density vs. Frequency

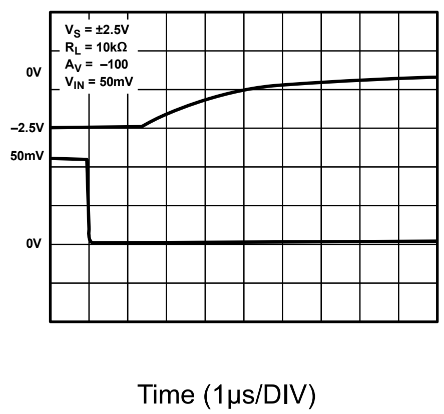


Figure 23: Negative Overload Recovery

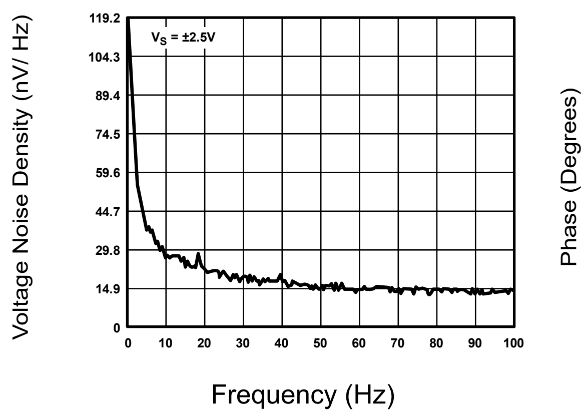


Figure 24: Voltage Noise Density vs. Frequency

7.5Typical Characteristic

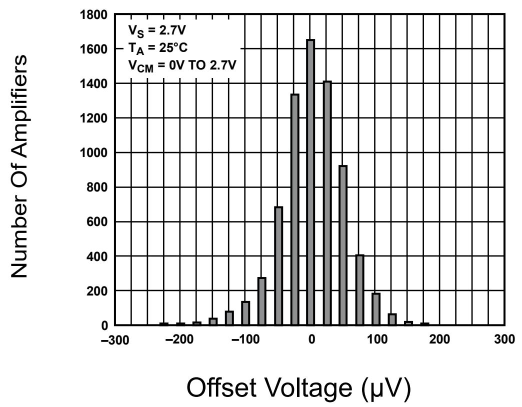


Figure 25: Input Offset Voltage Distribution

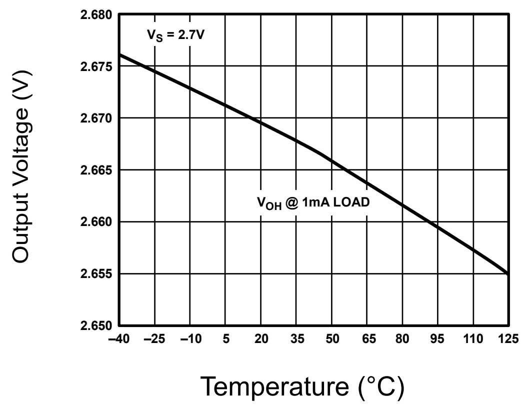


Figure 26: Output Voltage Swing High vs. Temperature

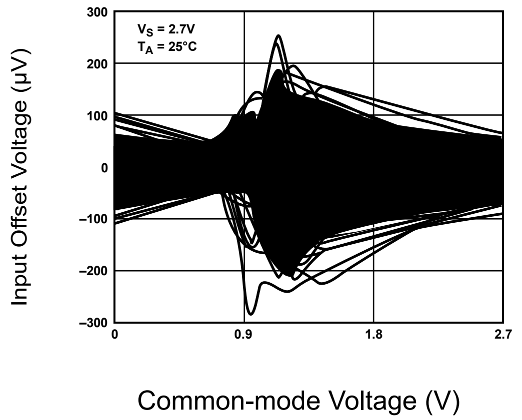


Figure 27: Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)

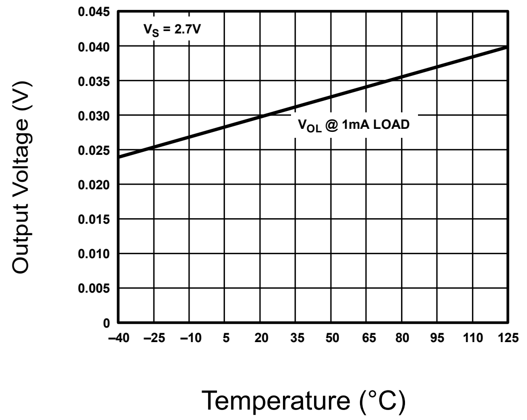


Figure 28: Output Voltage Swing Low vs. Temperature

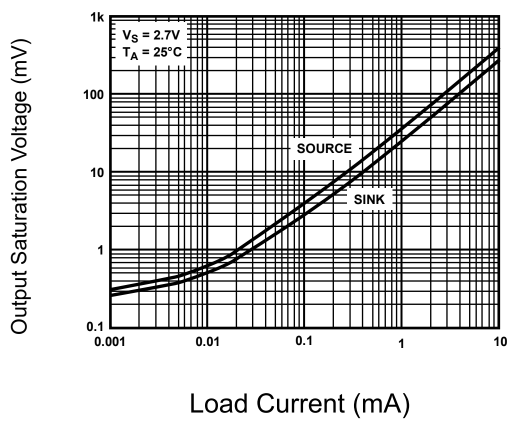


Figure 29: Output Saturation Voltage vs. Load Current

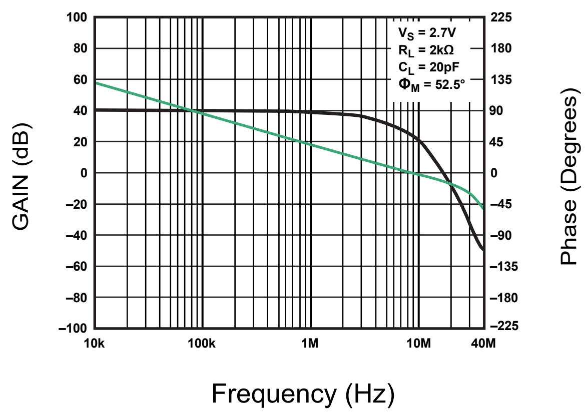


Figure 30: Open-Loop Gain and Phase vs. Frequency

7.6Typical Characteristic

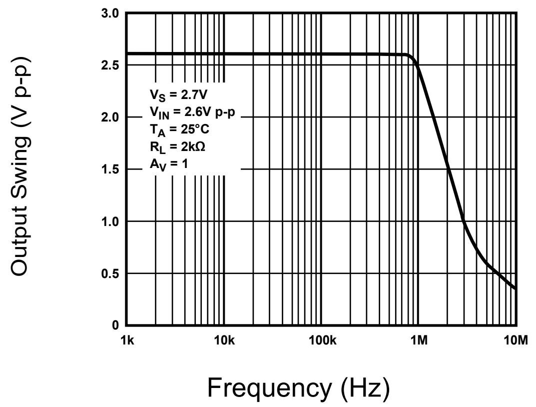


Figure 31: Closed-Loop Output Voltage Swing vs. Frequency (FPBW)

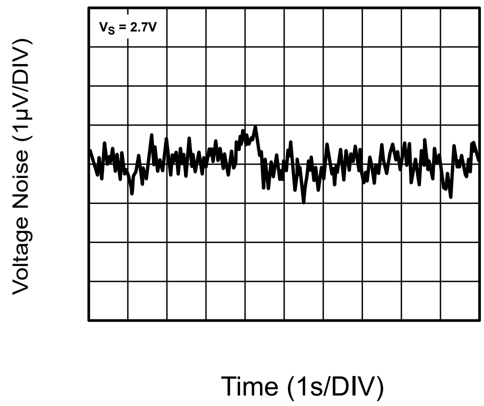


Figure 32: 0.1 Hz to 10 Hz Input Voltage Noise

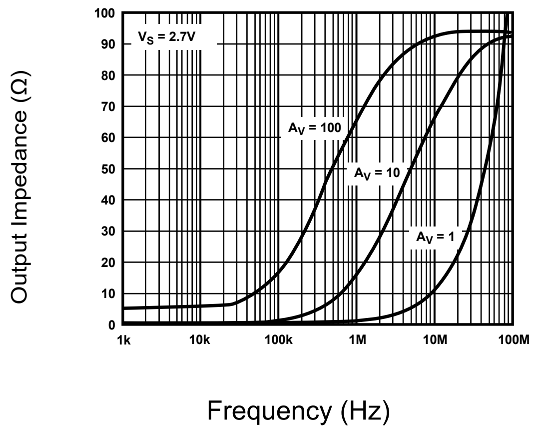


Figure 33: Output Impedance vs. Frequency

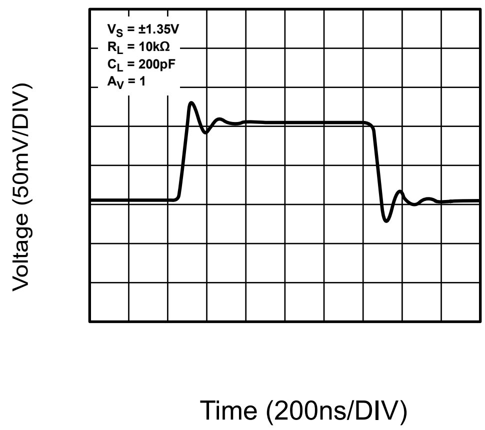


Figure 34: Small Signal Transient Response

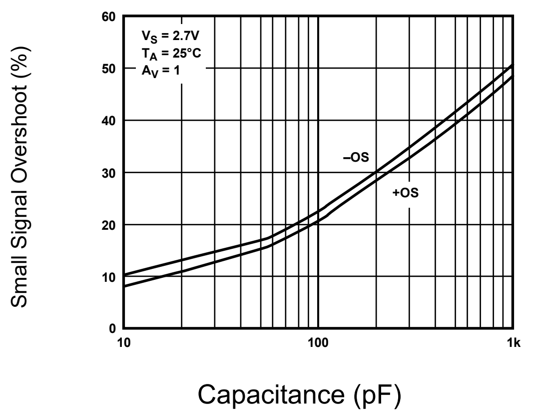


Figure 35: Small Signal Overshoot vs. Load Capacitance

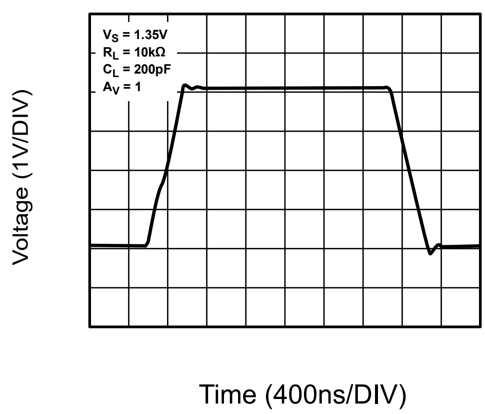


Figure 36: Large Signal Transient Response

7.7Typical Characteristic

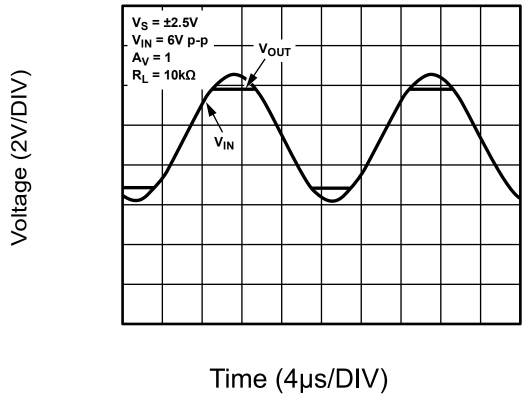


Figure 31: No Phase Reversal

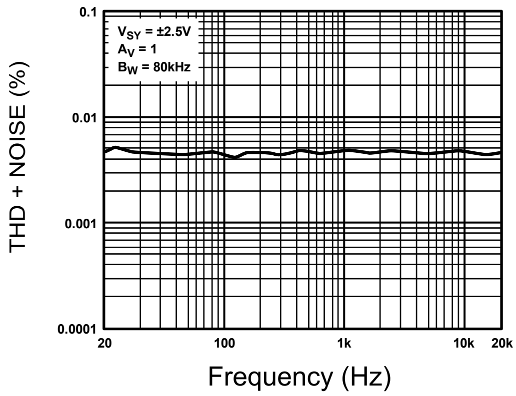


Figure 32: THD + Noise vs. Frequency

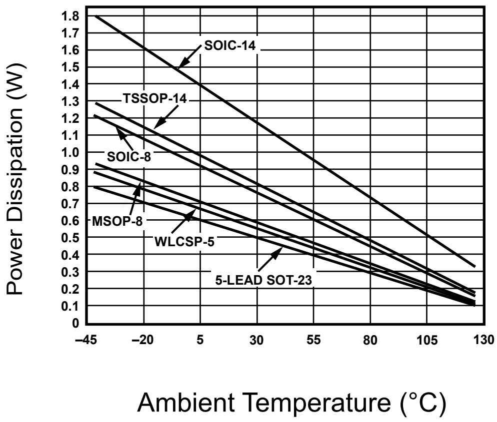
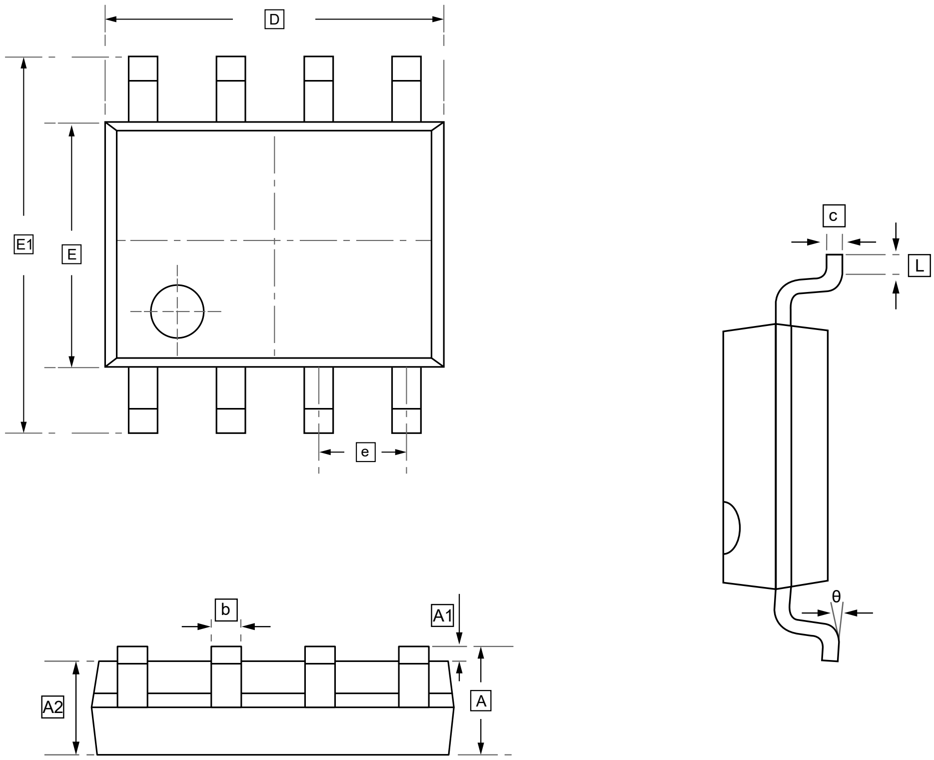


Figure 33: Maximum Power Dissipation vs. Ambient Temperature

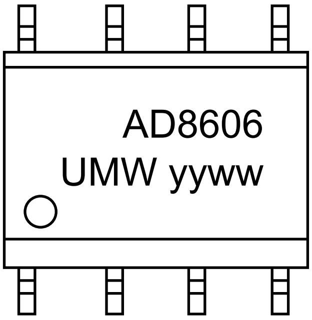
8.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AD8606ARZ	SOP-8	2500	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

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