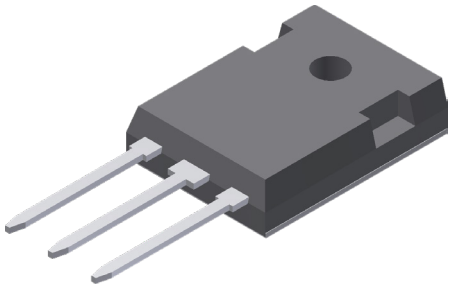
CLA50E1200HB

1200 V, 50 A High Efficiency Thyristor

RoHS



Features:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

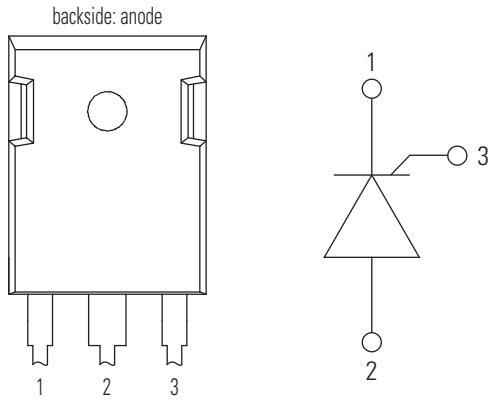
Applications:

- Line rectifying 50/60 Hz
- Soft start AC motor control
- Lighting and temperature control
- DC motor control
- Power converter
- AC power control

Package:

- RoHS compliant
- Epoxy meets UL 94V-0
- Industry standard TO-247 package

Pinout Diagram (TO-247-3L)



1: Cathode; **2:** Anode; **3:** Gate

Product Summary

Characteristic	Value	Unit
V_{RRM}	1200	V
I_{TAV}	50	A
V_T	1.27	V

Maximum Ratings

Symbol	Characteristics	Conditions		Value	Units
$I_{T(RMS)}$	RMS On-state Current (Half Sine Wave)	180° Sine; T_C = 125°C; T_{VJ} = 150°C		79	A
I_{TAV}	Average Forward Current			50	
$I_{R/D}$	Reverse Current, Drain Current	T_{VJ} = 25°C; $V_{R/D}$ = 1200 V		50	µA
		T_{VJ} = 125°C; $V_{R/D}$ = 1200 V		4	mA
I_{TSM}	Maximum Forward Surge Current	T_{VJ} = 45°C	t = 10 ms, 50 Hz sine, V_R = 0 V	650	A
			t = 8.3 ms, 60 Hz sine, V_R = 0 V	700	
		T_{VJ} = 150°C	t = 10 ms, 50 Hz sine, V_R = 0 V	555	
			t = 8.3 ms, 60 Hz sine, V_R = 0 V	595	
I^2t	I^2t Value for Fusing	T_{VJ} = 45°C	t = 10 ms, 50 Hz sine, V_R = 0 V	2.12	kA^2s
			t = 8.3 ms, 60 Hz sine, V_R = 0 V	2.04	
		T_{VJ} = 150°C	t = 10 ms, 50 Hz sine, V_R = 0 V	1.54	
			t = 8.3 ms, 60 Hz sine, V_R = 0 V	1.48	
V_{RSM}/V_{DSM}	Maximum Non-repetitive Reverse/Forward Blocking Voltage	T_{VJ} = 25°C		1300	V
V_{RRM}/V_{DRM}	Maximum Repetitive Reverse/ Forward Blocking Voltage	T_{VJ} = 25°C		1200	V
di/dt_{cr}	Critical Rate of Rise of On-state Current	t_p= 200 µs; f = 50 Hz; di_G/dt = 0.3 A/µs; I_G=0.3 A; T_{VJ} = 150°C; V=2/3 V_{DRM}	Repetitive, I_T = 150 A	150	A/µs
			Non-repetitive, I_T = 50 A	500	
dv/dt_{cr}	Critical Rate of Rise of Voltage	V = 2/3 V_{DRM}, R_{GK} = ∞, method 1 (linear voltage rise), T_{VJ} = 150 °C		1000	V/ µs
P_{GM}	Maximum Gate Power Dissipation	T_C = 150°C	t_p = 30 µs	10	W
			t_p = 300 µs	5	
P_{GAV}	Average Gate Power Dissipation	T_C = 150°C		0.5	W
P_{tot}	Total Power Dissipation	T_C = 25 °C		500	W
T_{STG}	Storage Temperature Range	–		–40 to 150	°C
T_{OP}	Operating Temperature Range	–		–40 to 125	°C
T_{VJ}	Virtual Junction Temperature Range	–		–40 to 150	°C

Thermal Characteristics

Symbol	Characteristics	Value			Units
		Min.	Typ.	Max.	
R_{thJC}	Thermal Resistance, Junction to Case	–	–	0.25	K/W
R_{thCH}	Thermal Resistance, Case to Heatsink	–	0.3	–	K/W

Electrical Characteristics

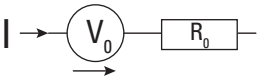
Symbol	Characteristics	Conditions		Value			Units
				Min.	Typ.	Max.	
I_{GT}	Gate Trigger Current	T_{VJ} = 25°C	V_D = 6 V	–	–	50	mA
		T_{VJ} = –40°C		–	–	80	
V_{GT}	Gate Trigger Voltage	T_{VJ} = 25°C	V_D = 6 V	–	–	1.5	V
		T_{VJ} = –40°C		–	–	1.6	
I_{GD}	Gate Non-trigger Current	V_D = 2/3 V_{DRM}, T_{VJ} = 150°C		–	–	3	mA
V_{GD}	Gate Non-trigger Voltage	V_D = 2/3 V_{DRM}, T_{VJ} = 150°C		–	–	0.2	V
V_T	Forward Voltage Drop	T_{VJ} = 25°C	I_T = 50 A	–	–	1.32	V
			I_T = 100 A	–	–	1.60	
		T_{VJ} = 125°C	I_T = 50 A	–	–	1.27	
			I_T = 100 A	–	–	1.65	
I_L	Latching Current	t_p = 10 µs; I_G = 0.3 A; di_G/dt = 0.3 A/µs; T_{VJ} = 25°C		–	–	125	mA
I_H	Holding Current	V_D = 6 V; R_{GK} = ∞; T_{VJ} = 25°C		–	–	115	mA
V_{T0}	Threshold Voltage [1]	T_{VJ} = 150°C		–	–	0.88	V
r_T	Slope Resistance [1]	T_{VJ} = 150°C		–	–	7.7	mΩ
C_J	Junction Capacitance	V_R = 400 V, f = 1 MHz		–	25	–	pF
t_{gd}	Gate Controlled Delay Time	V_D = 1/2 V_{DRM}; I_G = 0.3 A ; di_G/dt = 0.3 A/µs; T_{VJ} = 25°C		–	–	2	µs
t_q	Turn-off Time	V_R = 100 V; I_T = 50 A; V = 2/3 V_{DRM} ; di/dt = 10 A/µs; dv/dt = 20 V/µs; t_p = 200 µs; T_{VJ} = 125°C		–	200	–	µs

Note 1: For power loss calculation only

Package

Symbol	Characteristics	Conditions	Value			Units
			Min.	Typ.	Max.	
I_{RMS}	RMS Current	per terminal	–	–	70	A
M_D	Mounting Torque	–	0.8	–	1.2	Nm
F_C	Mounting force with clip	–	20	–	120	N
G	Weight	–	–	6	–	g

Equivalent Circuits for Simulation (T_{VJ} = 150°C)



Symbol	Characteristics	Value	Units
$V_{0\ max}$	Threshold Voltage	0.88	V
$R_{0\ max}$	Slope Resistance[1]	5.2	mΩ

Note 1: On die level

Characteristic Curves

Figure 1. Forward Characteristics

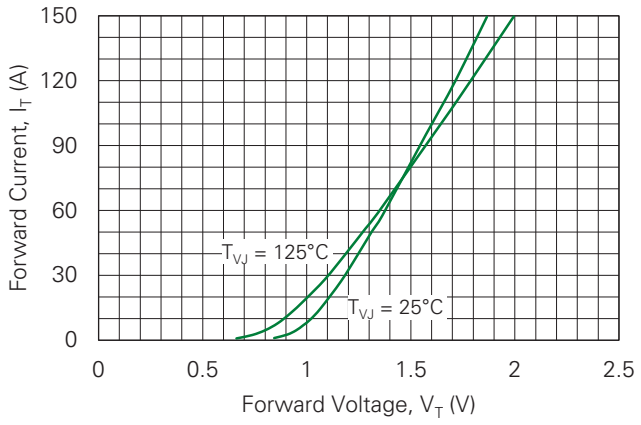


Figure 2. Surge Overload Current
I_{TSM}: Crest Value, t: duration

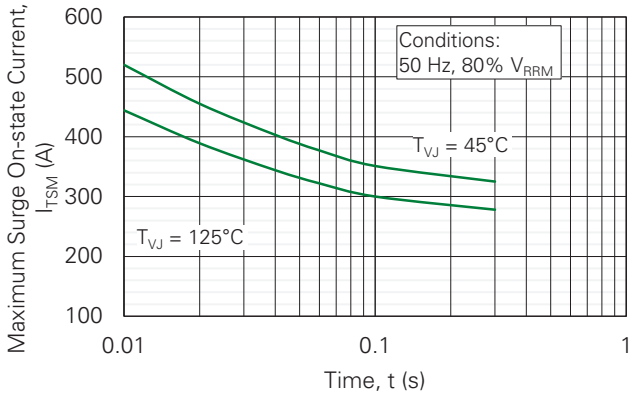


Figure 3. I^2t vs. Time (1-10 s)

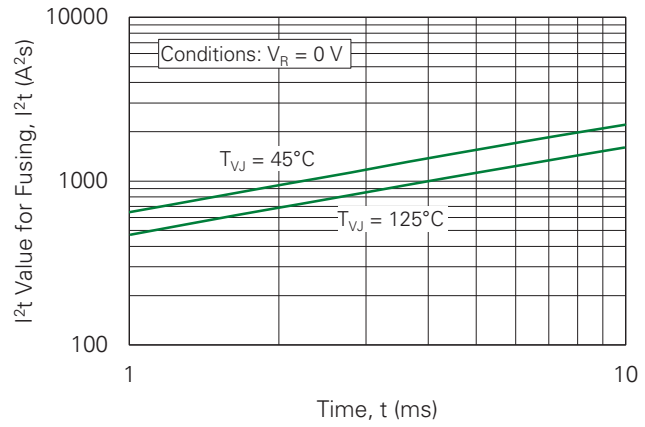


Figure 4. Gate Trigger Voltage vs. Gate Trigger Current

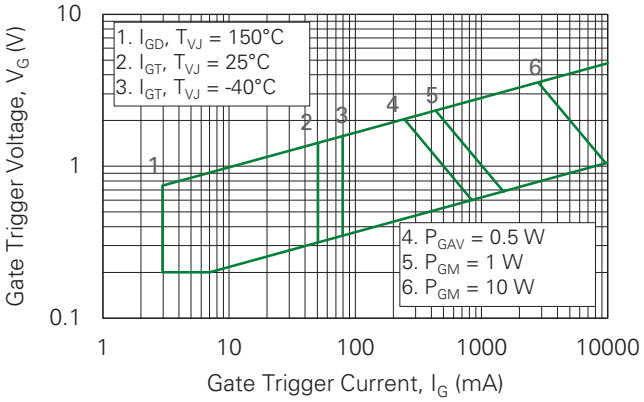


Figure 5. Gate Controlled Delay Time vs. Gate Trigger Current

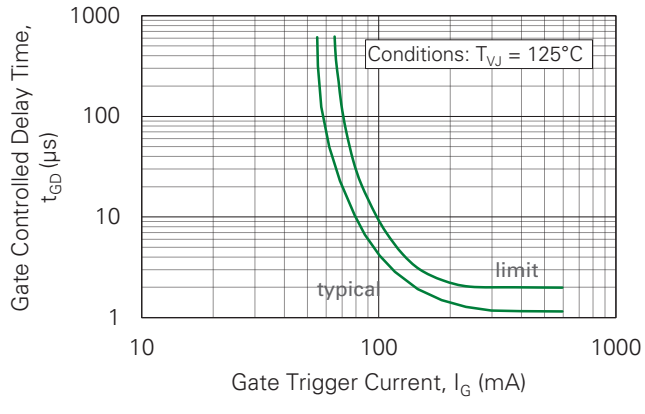


Figure 6. Max. Forward Current vs. Case Temperature

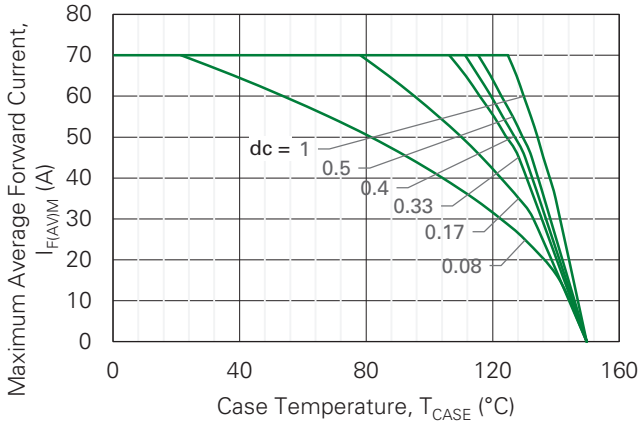


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Figure 7a. Power Dissipation vs. Direct Output Current

Figure 7b. Power Dissipation vs. Ambient Temperature

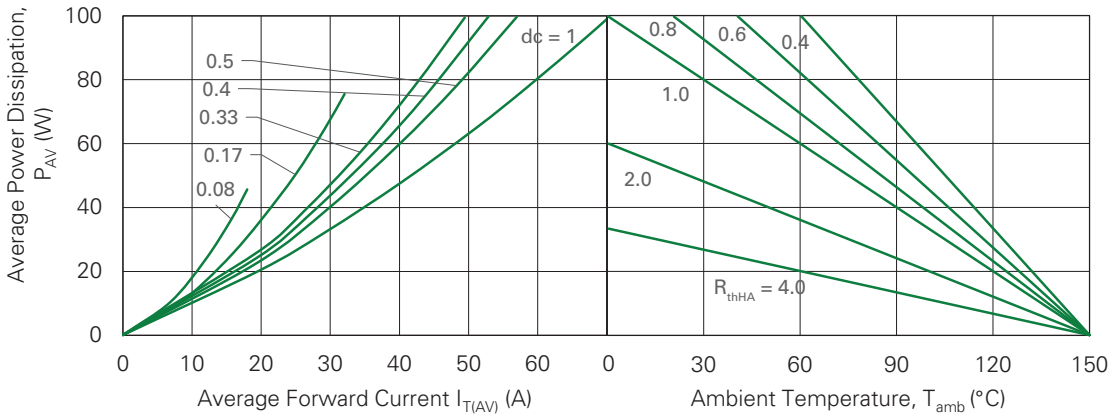
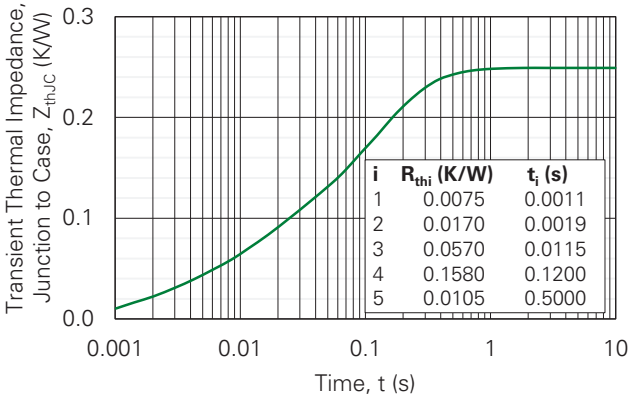
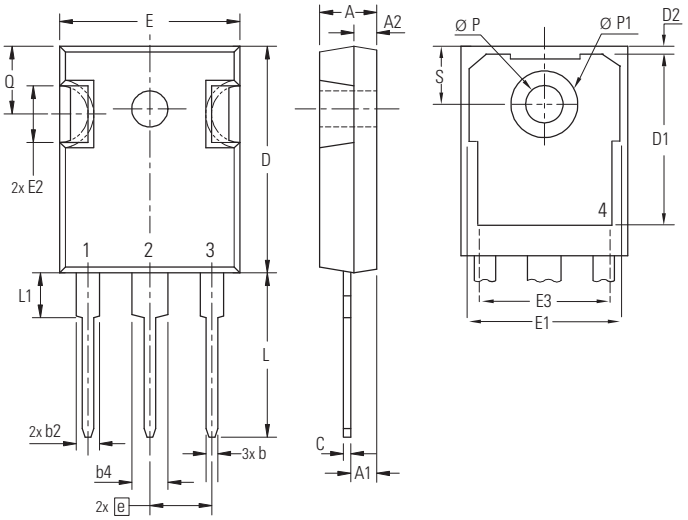


Figure 8. Transient Thermal Impedance, Junction to Case



i	R_{thi} (K/W)	t_i (s)
1	0.0075	0.0011
2	0.0170	0.0019
3	0.0570	0.0115
4	0.1580	0.1200
5	0.0105	0.5000

Part Outline Drawing (TO-247-3L)



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max
A	4.70	5.30	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.39	0.065	0.094
b4	2.59	3.43	0.102	0.135
C	0.38	0.89	0.015	0.035
D	20.79	21.45	0.819	0.845
D1	13.07	–	0.515	–
D2	0.51	1.35	0.020	0.053
e	5.45 BSC		0.215 BSC	
E	15.48	16.24	0.610	0.640
E1	13.45	–	0.530	–
E2	4.31	5.48	0.170	0.216
E3	–	13.43	–	0.529
L	19.80	20.30	0.780	0.800
L1	–	4.49	–	0.177
Q	5.38	6.19	0.212	0.244
S	6.14 BSC		0.242 BSC	
ØP	3.55	3.65	0.140	0.144
ØP1	–	7.39	–	0.29

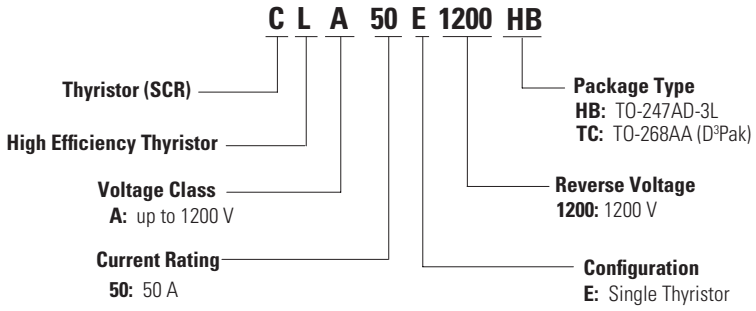
Product Selector

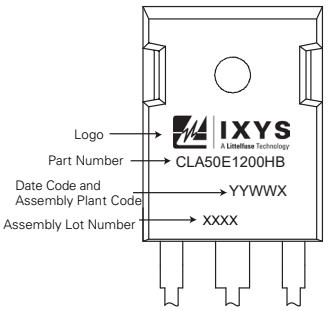
Part Number	Voltage Class	Package
CLA50E1200HB	1200 V	TO-247AD-3L
CLA50E1200TC	1200 V	TO-268AA (D^3PAK)

Packing Options

Part Number	Marking	Packing Mode	Quantity
CLA50E1200HB	CLA50E1200HB	Tube	30

Part Numbering and Marking





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