

## 2-W FILTERLESS MONO CLASS-D AUDIO POWER AMPLIFIER

### FEATURES

- Modulation Scheme Optimized to Operate Without a Filter
- 4 mm × 4 mm MicroStar Junior BGA and TSSOP Package Options
- 2 W Into a 4-Ω Speaker (THD+N<1%)
- <0.2% THD+N at 1.5 W, 1 kHz, Into a 4-Ω Load
- Extremely Efficient Third Generation 5-V Class-D Technology:
  - Low-Supply Current (No Filter): 4 mA
  - Low-Supply Current (Filter): 7.5 mA
  - Low-Shutdown Current: 0.05 µA
  - Low-Noise Floor: 40 µV<sub>RMS</sub> (No-Weighting Filter)
  - Maximum Efficiency Into 8 Ω, 75 - 85 %
  - 4 Internal Gain Settings: 6 to 23.5 dB
  - PSRR: -77 dB
- Integrated Depop Circuitry
- Short-Circuit Protection (Short to Battery, Ground, and Load)

### APPLICATIONS

- High-Efficiency For Extended Battery Run Time

### DESCRIPTION

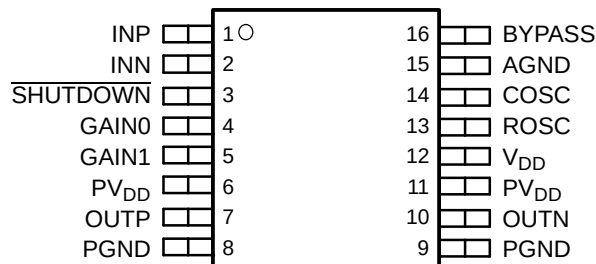
The TPA2000D1 is a 2-W mono bridge-tied-load (BTL) class-D amplifier designed to drive a speaker with at least 4-Ω impedance. The amplifier uses TI's third generation modulation technique, which results in improved efficiency and SNR. It also allows the device to be connected directly to the speaker without the use of the LC output filter commonly associated with class-D amplifiers (this results in EMI that must be shielded at the system level). These features make the device ideal for use in devices where high efficiency is needed to extend battery run time.

The gain of the amplifier is controlled by two input terminals, GAIN1 and GAIN0. This allows the amplifier to be configured for a gain of 6, 12, 18, and 23.5 dB. The differential input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

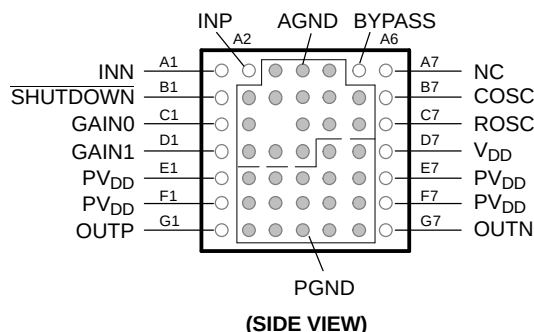
The class-D BTL amplifier includes depop circuitry to reduce the amount of turnon pop at power up and when cycling **SHUTDOWN**.

The TPA2000D1 is available in the 16-pin TSSOP and MicroStar Junior™ BGA packages that drive 2 W of continuous output power into a 4-Ω load. TPA2000D1 operates over an ambient temperature range of -40°C to 85°C.

PW PACKAGE  
(TOP VIEW)



MicroStar Junior™ (GQC) Package  
(TOP VIEW)



(SIDE VIEW)

NC – No internal connection, still requires a pad for the ball.

NOTE: The shaded terminals are used for thermal connections to the ground plane.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar Junior is a trademark of Texas Instruments.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

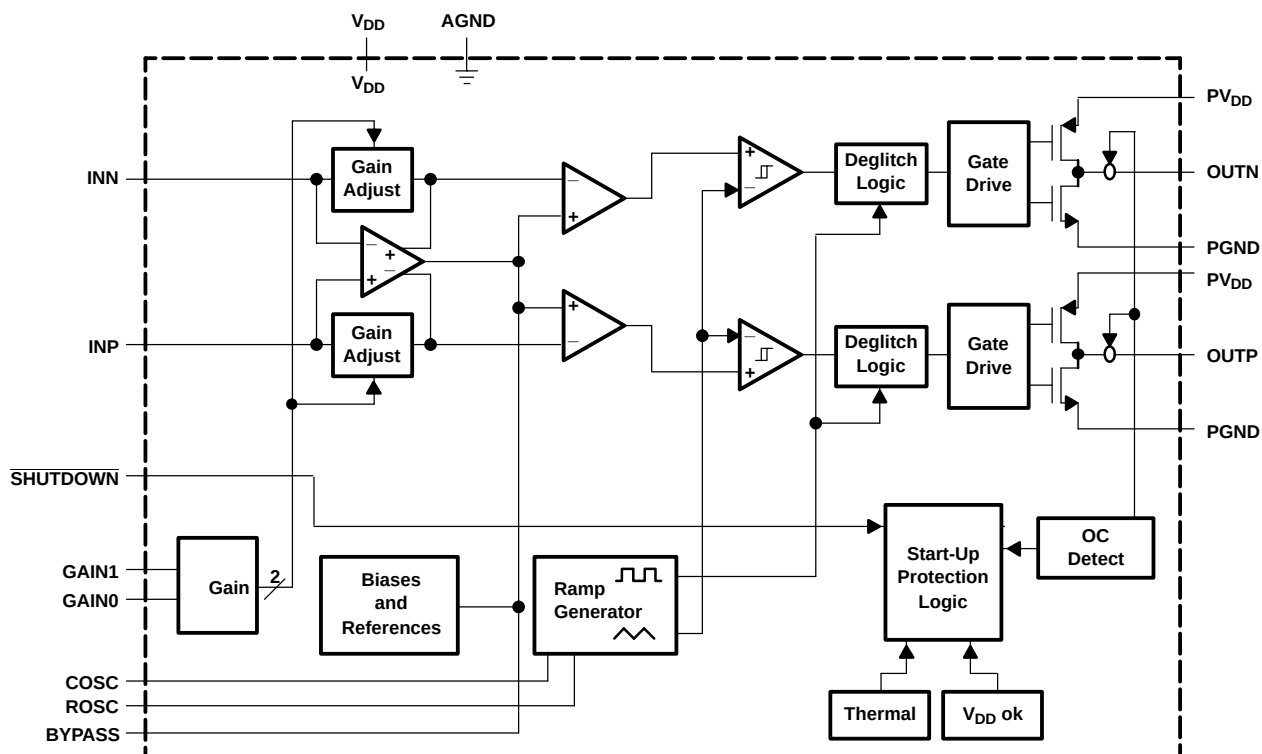
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### AVAILABLE OPTIONS

| $T_A$        | PACKAGED DEVICES          |                    |
|--------------|---------------------------|--------------------|
|              | TSSOP (PW) <sup>(1)</sup> | GQC <sup>(2)</sup> |
| 40°C to 85°C | TPA2000D1PW               | TPA2000D1GQCR      |

- (1) The PW package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2000D1PWR).
- (2) The GQC package is only available taped and reeled.

### FUNCTIONAL BLOCK DIAGRAM



## TERMINAL FUNCTIONS

| TERMINAL         |                                           |       | I/O | DESCRIPTION                                                                                                                                               |
|------------------|-------------------------------------------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME             | NO.                                       |       |     |                                                                                                                                                           |
|                  | GQC                                       | PW    |     |                                                                                                                                                           |
| AGND             | A3 - A5,<br>B2 - B6<br>C2 - C6<br>D2 - D4 | 15    | I   | Analog ground                                                                                                                                             |
| BYPASS           | A6                                        | 16    | I   | Connect capacitor to ground for BYPASS voltage filtering.                                                                                                 |
| COSC             | B7                                        | 14    | I   | Connect capacitor to ground to set oscillation frequency.                                                                                                 |
| GAIN0            | C1                                        | 4     | I   | Bit 0 of gain control (TTL logic level)                                                                                                                   |
| GAIN1            | D1                                        | 5     | I   | Bit 1 of gain control (TTL logic level)                                                                                                                   |
| INN              | A1                                        | 2     | I   | Negative differential input                                                                                                                               |
| INP              | A2                                        | 1     | I   | Positive differential input                                                                                                                               |
| OUTN             | G7                                        | 10    | O   | Negative BTL output                                                                                                                                       |
| OUTP             | G1                                        | 7     | O   | Positive BTL output                                                                                                                                       |
| PGND             | D5, D6<br>E2 - E6<br>F2 - F6<br>G2 - G6   | 8, 9  | I   | High-current grounds                                                                                                                                      |
| PV <sub>DD</sub> | E1, E7,<br>F1, F7                         | 6, 11 | I   | High-current power supplies                                                                                                                               |
| ROSC             | C7                                        | 13    | I   | Connect resistor to ground to set oscillation frequency.                                                                                                  |
| SHUTDOWN         | B1                                        | 3     | I   | Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal, and normal operation if a TTL logic high is placed on this terminal. |
| V <sub>DD</sub>  | D7                                        | 12    | I   | Analog power supply                                                                                                                                       |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| UNITS                                                         |                                    |                                  |
|---------------------------------------------------------------|------------------------------------|----------------------------------|
| Supply voltage                                                | V <sub>DD</sub> , PV <sub>DD</sub> | -0.3 V to 5.5 V                  |
| Input voltage, V <sub>i</sub>                                 |                                    | -0.3 V to V <sub>DD</sub> +0.3 V |
| Continuous total power dissipation                            |                                    | (See Dissipation Rating Table)   |
| Operating free-air temperature range, T <sub>A</sub>          |                                    | -40°C to 85°C                    |
| Operating junction temperature range, T <sub>J</sub>          |                                    | -40°C to 150°C                   |
| Storage temperature range, T <sub>stg</sub>                   |                                    | -65°C to 150°C                   |
| Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds |                                    | 260°C                            |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATING TABLE

| PACKAGE | T <sub>A</sub> ≤ 25°C | DERATING FACTOR | T <sub>A</sub> = 70°C | T <sub>A</sub> = 85°C |
|---------|-----------------------|-----------------|-----------------------|-----------------------|
| PW      | 774 mW                | 6.19 mW/°C      | 495 mW                | 402 mW                |
| GQC     | 2.61 W                | 20.9 mW/°C      | 1.67 W                | 1.36 W                |

**RECOMMENDED OPERATING CONDITIONS**

|                      |                                |                               | MIN | MAX | UNIT |
|----------------------|--------------------------------|-------------------------------|-----|-----|------|
| $V_{DD}$ , $PV_{DD}$ | Supply voltage                 |                               | 2.7 | 5.5 | V    |
| $V_{IH}$             | High-level input voltage       | GAIN0, GAIN1, <u>SHUTDOWN</u> | 2   |     | V    |
| $V_{IL}$             | Low-level input voltage        | GAIN0, GAIN1, <u>SHUTDOWN</u> |     | 0.7 | V    |
| $f_s$                | Switching frequency            |                               | 200 | 300 | kHz  |
| $T_A$                | Operating free-air temperature |                               | -40 | 85  | °C   |

**ELECTRICAL CHARACTERISTICS**at specified free-air temperature,  $PV_{DD} = V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER    | TEST CONDITIONS                                                                                 | MIN | TYP  | MAX | UNIT          |
|--------------|-------------------------------------------------------------------------------------------------|-----|------|-----|---------------|
| $ V_{OS} $   | Output offset voltage (measured differentially)<br>$V_I = 0\text{ V}$ , $A_V = \text{any gain}$ |     |      | 25  | mV            |
| PSRR         | Power supply rejection ratio<br>$PV_{DD} = 4.9\text{ V to }5.1\text{ V}$                        |     | -77  |     | dB            |
| $ I_{IH} $   | High-level input current<br>$PV_{DD} = 5.5$ , $V_I = PV_{DD}$                                   |     |      | 1   | $\mu\text{A}$ |
| $ I_{IL} $   | Low-level input current<br>$PV_{DD} = 5.5$ , $V_I = 0\text{ V}$                                 |     |      | 1   | $\mu\text{A}$ |
| $I_{DD}$     | Supply current, no filter (with or without speaker load)                                        |     | 4    | 6   | mA            |
| $I_{DD(SD)}$ | Supply current, shutdown mode<br>GAIN0, GAIN1, <u>SHUTDOWN</u> = 0 V                            |     | 0.05 | 20  | $\mu\text{A}$ |

**OPERATING CHARACTERISTICS** $PV_{DD} = V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 4\ \Omega$ , gain = 6 dB (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                                                                                                        | MIN | TYP   | MAX | UNIT               |
|-----------|------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|--------------------|
| $P_O$     | Output power<br>THD = 1%, $f = 1\text{ kHz}$                                                                           |     | 2     |     | W                  |
| THD + N   | Total harmonic distortion plus noise<br>$P_O = 1.5\text{ W}$ , $f = 20\text{ Hz to }20\text{ kHz}$                     |     | <0.2% |     |                    |
| $k_{SVR}$ | Supply ripple rejection ratio<br>$f = 1\text{ kHz}$ , $C_{BYP} = 1\ \mu\text{F}$                                       |     | -67   |     | dB                 |
| SNR       | Signal-to-noise ratio                                                                                                  |     | 95    |     | dB                 |
| $V_n$     | Output noise voltage (no-noise weighting filter)<br>$C_{BYP} = 1\ \mu\text{F}$ , $f = < 10\text{ Hz to }22\text{ kHz}$ |     | 40    |     | $\mu\text{V(rms)}$ |
| $Z_i$     | Input impedance                                                                                                        |     | >15   |     | k $\Omega$         |

**ELECTRICAL CHARACTERISTICS**at specified free-air temperature,  $PV_{DD} = V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER    | TEST CONDITIONS                                                                                 | MIN | TYP  | MAX | UNIT          |
|--------------|-------------------------------------------------------------------------------------------------|-----|------|-----|---------------|
| $ V_{OS} $   | Output offset voltage (measured differentially)<br>$V_I = 0\text{ V}$ , $A_V = \text{any gain}$ |     |      | 25  | mV            |
| PSRR         | Power supply rejection ratio<br>$PV_{DD} = 3.2\text{ V to }3.4\text{ V}$                        |     | -61  |     | dB            |
| $ I_{IH} $   | High-level input current<br>$PV_{DD} = 3.3$ , $V_I = PV_{DD}$                                   |     |      | 1   | $\mu\text{A}$ |
| $ I_{IL} $   | Low-level input current<br>$PV_{DD} = 3.3$ , $V_I = 0\text{ V}$                                 |     |      | 1   | $\mu\text{A}$ |
| $I_{DD}$     | Supply current, no filter (with or without speaker load)                                        |     | 4    | 6   | mA            |
| $I_{DD(SD)}$ | Supply current, shutdown mode                                                                   |     | 0.05 | 20  | $\mu\text{A}$ |

## OPERATING CHARACTERISTICS

$P_{V_{DD}} = V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 4\ \Omega$ , gain = 6 dB (unless otherwise noted)

| PARAMETER |                                                  | TEST CONDITIONS                                                   | MIN | TYP   | MAX | UNIT               |
|-----------|--------------------------------------------------|-------------------------------------------------------------------|-----|-------|-----|--------------------|
| $P_O$     | Output power                                     | THD = 1%, $f = 1\text{ kHz}$                                      |     | 850   |     | mW                 |
| THD + N   | Total harmonic distortion plus noise             | $P_O = 55\text{ mW}$ , $f = 20\text{ Hz to }20\text{ kHz}$        |     | <0.2% |     |                    |
| $k_{SVR}$ | Supply ripple rejection ratio                    | $f = 1\text{ kHz}$ , $C_{BYP} = 1\ \mu\text{F}$                   |     | -61   |     | dB                 |
| SNR       | Signal-to-noise ratio                            |                                                                   |     | 93    |     | dB                 |
| $V_n$     | Output noise voltage (no-noise weighting filter) | $C_{BYP} = 1\ \mu\text{F}$ , $f = <10\text{ Hz to }22\text{ kHz}$ |     | 40    |     | $\mu\text{V(rms)}$ |
| $Z_i$     | Input impedance                                  |                                                                   |     | >15   |     | $\text{k}\Omega$   |

**Table 1. GAIN SETTINGS**

| GAIN1 | GAIN0 | AMPLIFIER GAIN (dB) | INPUT IMPEDANCE ( $\text{k}\Omega$ ) |
|-------|-------|---------------------|--------------------------------------|
|       |       | TYP                 | TYP                                  |
| 0     | 0     | 6                   | 104                                  |
| 0     | 1     | 12                  | 74                                   |
| 1     | 0     | 18                  | 44                                   |
| 1     | 1     | 23.5                | 24                                   |

## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

|             |                                      |                 | FIGURE  |
|-------------|--------------------------------------|-----------------|---------|
| $\eta$      | Efficiency                           | vs Output power | 1       |
|             | FFT at 1.5-W output power            | vs Frequency    | 2       |
| THD+N       | Total harmonic distortion plus noise | vs Output power | 3, 4, 5 |
|             |                                      | vs Frequency    | 6, 7    |
| $k_{(SRR)}$ | Supply ripple rejection ratio        | vs Frequency    | 8       |

### TEST SETUP FOR GRAPHS

The THD+N measurements shown do not use an LC output filter, but do use a 100- $\Omega$ , 0.047- $\mu$ F RC low-pass filter with a cutoff frequency of  $\sim$ 30 kHz before the audio analyzer so the switching frequency does not dominate the measurement. This is done to ensure that the THD+N measured is just the audible THD+N. The THD+N measurements are shown at the highest gain for worst case. The efficiency was measured with no filters, and a 3- $\Omega$ , 4- $\Omega$ , or 8- $\Omega$  resistor in series with a 33- $\mu$ H inductor as the load.

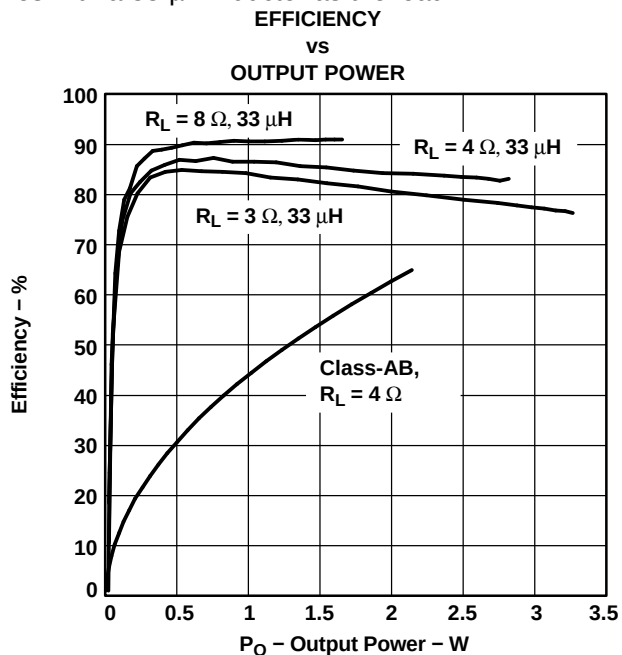


Figure 1.

## TYPICAL CHARACTERISTICS (continued)

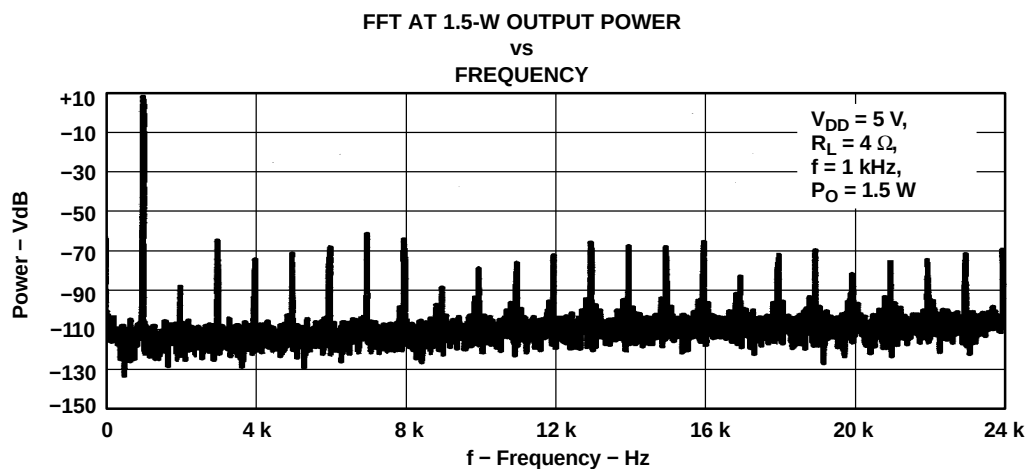


Figure 2.

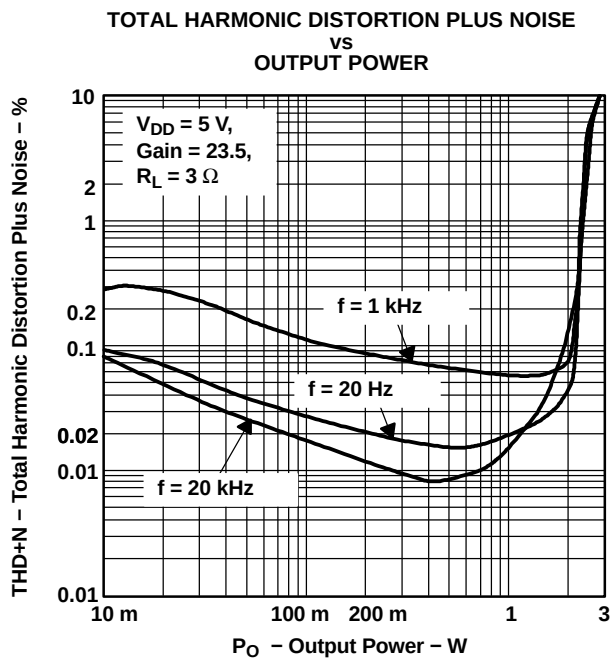


Figure 3.

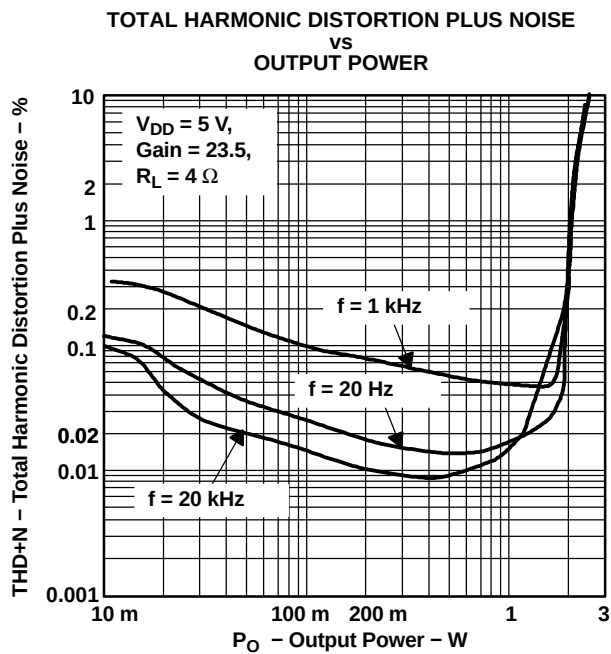


Figure 4.

## TYPICAL CHARACTERISTICS (continued)

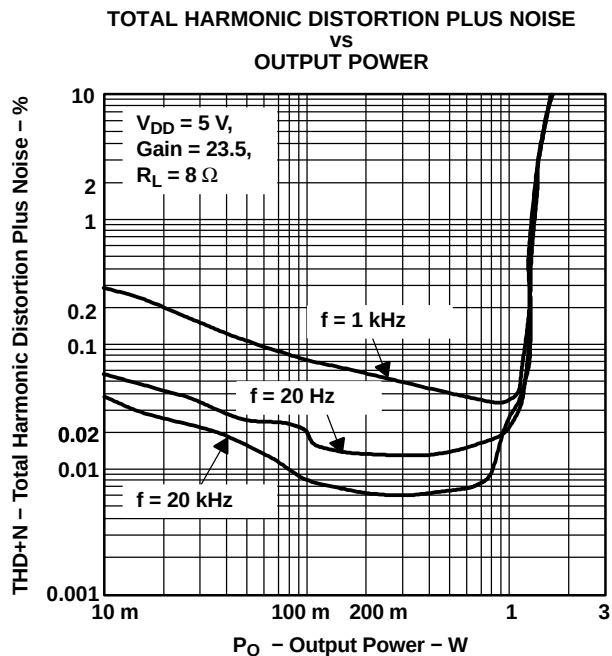


Figure 5.

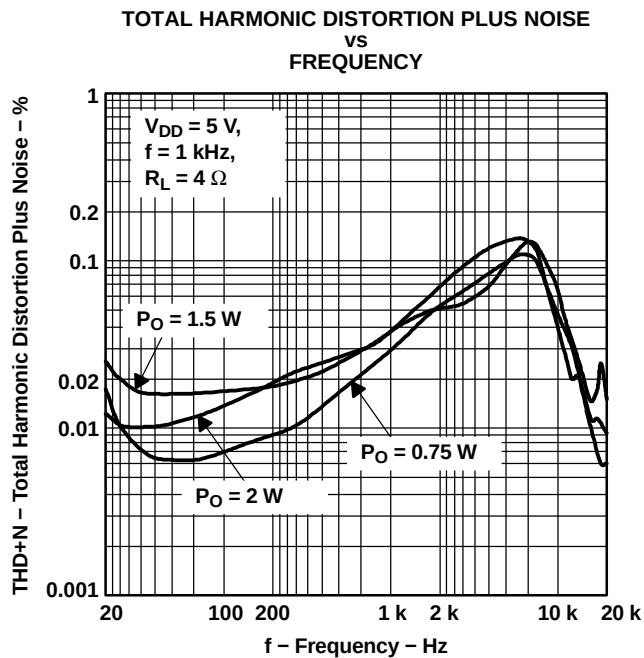


Figure 6.

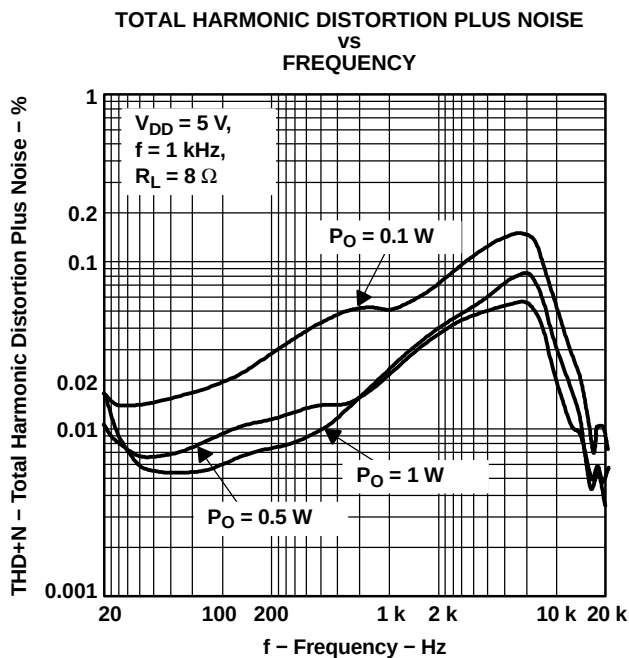


Figure 7.

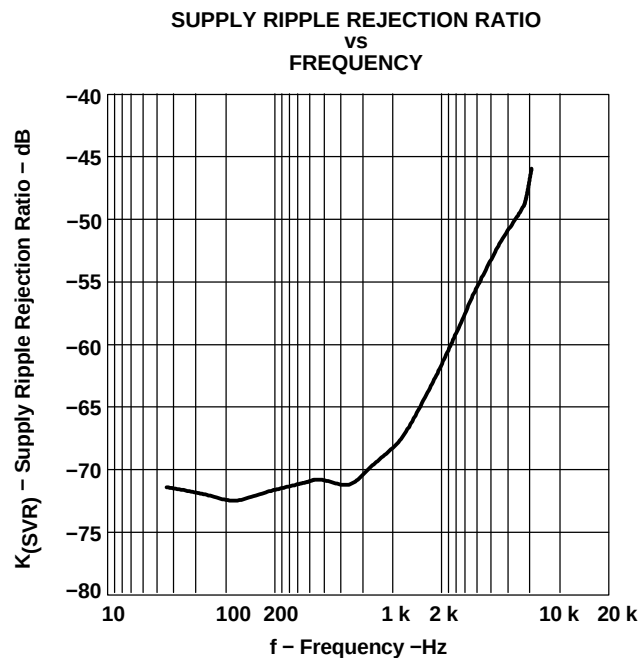


Figure 8.



## APPLICATION INFORMATION

### ELIMINATING THE OUTPUT FILTER WITH THE TPA2000D1

This section explains why the user can eliminate the output filter with the TPA2000D1.

#### EFFECT ON AUDIO

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

#### TRADITIONAL CLASS-D MODULATION SCHEME

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage,  $V_{DD}$ . Therefore, the differential prefiltered output varies between positive and negative  $V_{DD}$ , where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 9. Even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, and a high supply current.

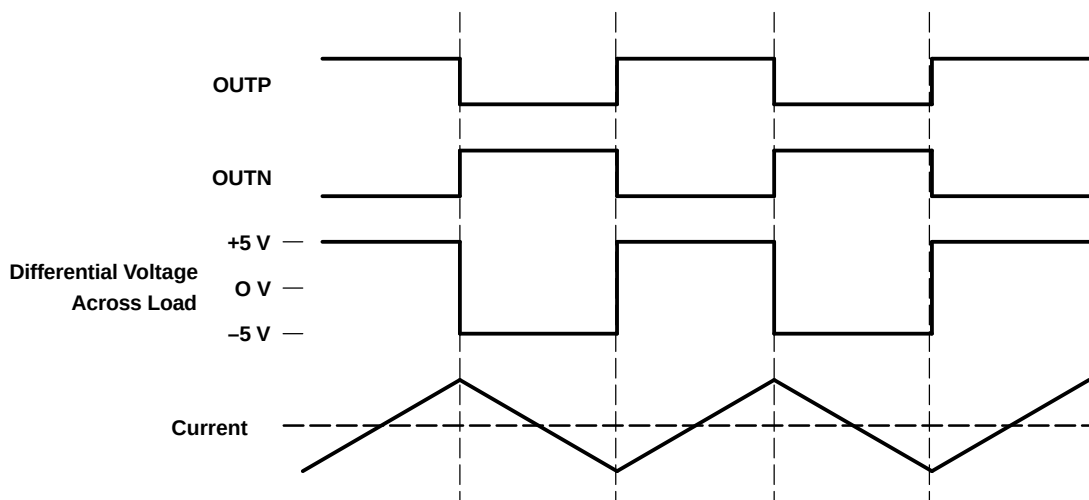
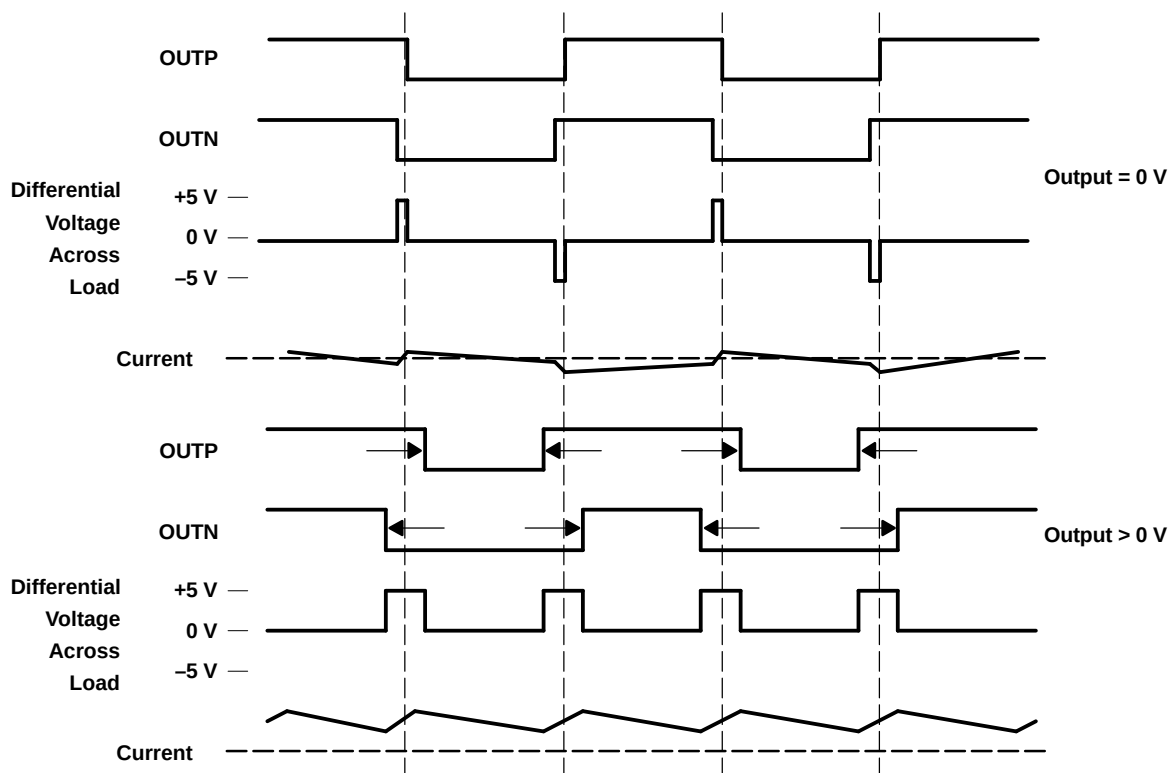


Figure 9. Traditional Class-D Modulation Scheme Output Voltage and Current Waveforms Into an Inductive Load With No Input

#### TPA2000D1 MODULATION SCHEME

The TPA2000D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative voltages. The voltage across the load sits at 0 V throughout most of the switching period greatly reducing the switching current, which reduces any  $I^2R$  losses in the load.

**APPLICATION INFORMATION (continued)**

**Figure 10. The TPA2000D1 Output Voltage and Current Waveforms Into an Inductive Load**

### EFFICIENCY: WHY YOU MUST USE A FILTER WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is  $2 \times V_{DD}$  and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2000D1 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is  $V_{DD}$  instead of  $2 \times V_{DD}$ . As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

## APPLICATION INFORMATION (continued)

### EFFECTS OF APPLYING A SQUARE WAVE INTO A SPEAKER

Audio specialists advise not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to  $1/f^2$  for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power ( $P_{SUP\ THEORETICAL}$ ) from the actual supply power ( $P_{SUP}$ ) at maximum output power ( $P_{OUT}$ ). The switching power dissipated in the speaker is the inverse of the measured efficiency ( $\eta_{MEASURED}$ ) minus the theoretical efficiency ( $\eta_{THEORETICAL}$ ) all multiplied by  $P_{OUT}$ .

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (1)$$

$$P_{SPKR} = P_{OUT}(P_{SUP} / P_{OUT} - P_{SUP\ THEORETICAL} / P_{OUT}) \text{ (at max output power)} \quad (2)$$

$$P_{SPKR} = P_{OUT}(1/\eta_{MEASURED} - 1/\eta_{THEORETICAL}) \text{ (at max output power)} \quad (3)$$

The maximum efficiency of the TPA2000D1 with an 8- $\Omega$  load is 85%. Using Equation 3 with the efficiency at maximum power (78%), we see that there is an additional 106 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

### WHEN TO USE AN OUTPUT FILTER

Design the TPA2000D1 without the filter if the traces from amplifier to speaker are short. The TPA2000D1 passed FCC and CE radiated emissions with no shielding with speaker wires eight inches long or less. Notebook PCs and powered speakers where the speaker is in the same enclosure as the amplifier are good applications for class-D without a filter.

A ferrite bead filter (shown in Figure 11) can often be used if the design is failing radiated emissions without a filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

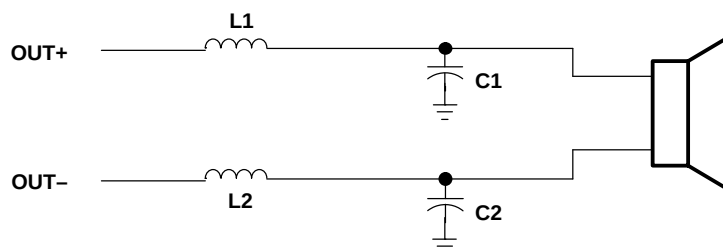
Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

The LC output filter is shown in Figure 11.

- $L1 = L2 = 22\ \mu\text{H}$  (DCR = 110 m $\Omega$ , part number = SCD0703T-220 M-S, manufacturer = GCI)
- $C1 = C2 = 1\ \mu\text{F}$

The ferrite filter is shown in Figure 11, where L is a ferrite bead.

- $L1 = L2 = \text{ferrite bead}$  (part number = MPZ1608S221, manufacturer = TDK)
- $C1 = C2 = 1\ \text{nF}$



**Figure 11. Class-D Output Filter**

**APPLICATION INFORMATION (continued)****GAIN SETTING VIA GAIN0 AND GAIN1 INPUTS**

The gain of the TPA2000D1 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance ( $Z_i$ ) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance can shift by up to 30% due to shifts in the actual resistance of the input resistors.

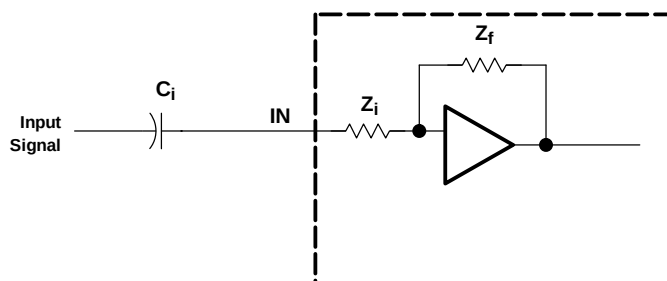
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 20 k $\Omega$ , which is the absolute minimum input impedance of the TPA2000D1. At the higher gain settings, the input impedance can increase as high as 115 k $\Omega$ .

**Table 2. GAIN SETTINGS**

| GAIN1 | GAIN0 | AMPLIFIER GAIN<br>(dB) | INPUT IMPEDANCE<br>(k $\Omega$ ) |
|-------|-------|------------------------|----------------------------------|
|       |       | TYP                    | TYP                              |
| 0     | 0     | 6                      | 104                              |
| 0     | 1     | 12                     | 74                               |
| 1     | 0     | 18                     | 44                               |
| 1     | 1     | 23.5                   | 24                               |

**INPUT RESISTANCE**

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency also changes by over six times.

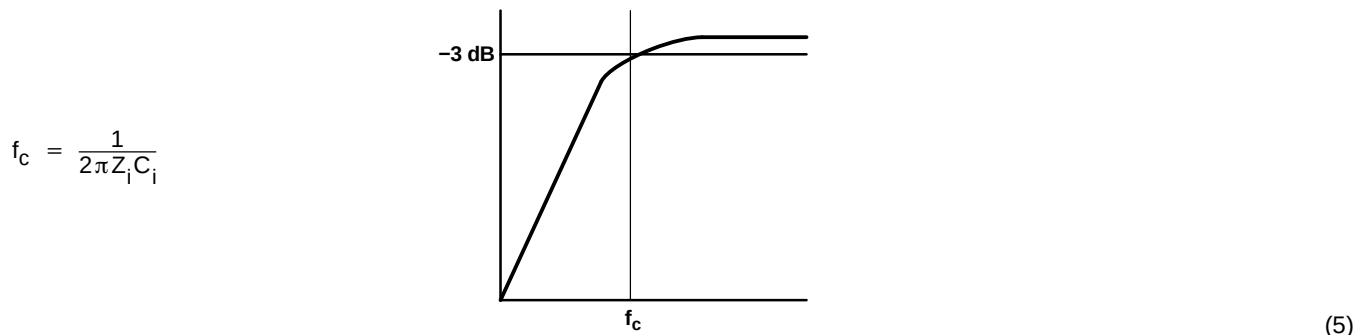


The -3-dB frequency can be calculated using Equation 4.

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_i(Z_i)} \quad (4)$$

## INPUT CAPACITOR, $C_i$

In the typical application an input capacitor ( $C_i$ ) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_i$  and the input impedance of the amplifier ( $Z_i$ ) form a high-pass filter with the corner frequency determined in Equation 5.



The value of  $C_i$  is important because it directly affects the bass (low frequency) performance of the circuit. Consider the example where  $Z_i$  is 20 k $\Omega$  and the specification calls for a flat bass response down to 80 Hz. Equation 5 is reconfigured as Equation 6.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (6)$$

In this example,  $C_i$  is 0.1  $\mu$ F, so one would likely choose a value in the range of 0.1  $\mu$ F to 1  $\mu$ F. If the gain is known and constant, use  $Z_i$  from Table 1 to calculate  $C_i$ . A further consideration for this capacitor is the leakage path from the input source through the input network ( $C_i$ ) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at  $V_{DD}/2$ , which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

$C_i$  must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing  $C_i$  for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$C_i \leq \frac{C_{BYP}}{10} \quad (7)$$

## POWER SUPPLY DECOUPLING, $C_s$

The TPA2000D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu$ F placed as close as possible to the device  $V_{DD}$  lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10  $\mu$ F or greater placed near the audio power amplifier is recommended.

## MIDRAIL BYPASS CAPACITOR, $C_{BYP}$

The midrail bypass capacitor ( $C_{BYP}$ ) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode,  $C_{BYP}$  determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ( $C_{BYP}$ ) values of 0.47- $\mu$ F to 1- $\mu$ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop,  $C_{BYP}$  should be 10 times larger than  $C_i$ .

$$C_{BYP} \geq 10 \times C_i \quad (8)$$

## DIFFERENTIAL INPUT

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA2000D1 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA2000D1 with a single-ended source, ac ground the INN input through a capacitor and apply the audio signal to the input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

## SHUTDOWN MODES

The TPA2000D1 employs a shutdown mode of operation designed to reduce supply current ( $I_{DD}$ ) to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state,  $I_{DD(SD)} = 1 \mu A$ . SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

## USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

## SWITCHING FREQUENCY

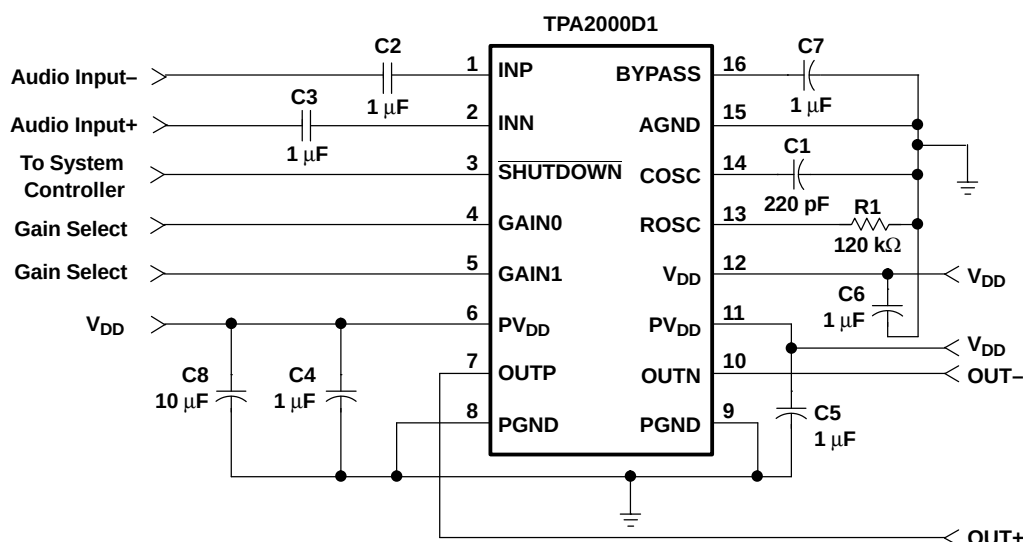
The switching frequency is determined using the values of the components connected to RO SC (pin 13) and CO SC (pin 14) and are calculated using Equation 9.

$$f_s = \frac{6.6}{R_{OSC} \times C_{OSC}} \quad (9)$$

The switching frequency was chosen to be centered on 250 kHz. This frequency represents the optimization of audio fidelity due to oversampling and the maximization of efficiency by minimizing the switching losses of the amplifier.

The recommended values are a resistance of 120 kΩ and a capacitance of 220 pF. Using these component values, the amplifier operates properly by using 5% tolerance resistors and 10% tolerance capacitors. The tolerance of the components can be changed as long as the switching frequency remains between 200 kHz and 300 kHz. Within this range, the internal circuitry of the device provides stable operation.

## APPLICATION CIRCUIT

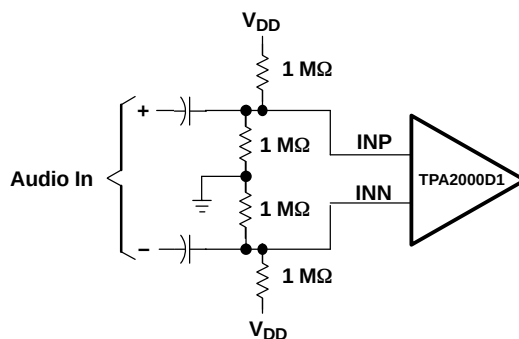


**Table 3. TPA2000D1 APPLICATION CIRCUIT BILL OF MATERIALS**

| REFERENCE | DESCRIPTION                                                        | SIZE         | QUANTITY | MANUFACTURER | PART NUMBER      |
|-----------|--------------------------------------------------------------------|--------------|----------|--------------|------------------|
| C1        | Capacitor, ceramic, 220 pF, ±10%, XICON, 50 V                      | 0805         | 1        | Mouser       | 140-CC501B221K   |
| C2 - C7   | Capacitor, ceramic, 1 μF, +80%/-20%, Y5V, 16 V                     | 0805         | 6        | Murata       | GRM40-Y5V105Z16  |
| C8        | Capacitor, ceramic, 10 μF, +80%/-20%, Y5V, 16 V                    | 1210         | 1        | Murata       | GRM235-Y5V106Z16 |
| R1        | Resistor, chip, 120 kΩ, 1/10 W, 5%, XICON                          | 0805         | 1        | Mouser       | 260-120K         |
| U1        | IC, TPA2000D1, audio power amplifier, 2-W, single channel, class-D | 24-pin TSSOP | 1        | TI           | TPA2000D1PW      |

## LOW SUPPLY VOLTAGE POP

The TPA2000D1 pops when coming out of shutdown at low supply voltages (3.3 V and less) when using the application schematic shown above. The pops occur because the common-mode input range is worse at the lower supply voltages. At low supply voltages, the inputs are not within the common-mode input range when coming out of shutdown. The outputs develop an offset voltage until the inputs settle within the common-mode input range. This causes a pop. Figure 12 shows 1-M $\Omega$  resistors added to form voltage dividers. The voltage dividers bias the inputs to  $V_{DD}/2$  that keeps the pop low at turn on and when coming out of shutdown. The resistors should be 1% tolerance to ensure the offset voltage is not increased.



**Figure 12. Voltage Dividers**



## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPA2000D1PW</a>  | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2000D1              |
| TPA2000D1PW.A                | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2000D1              |
| <a href="#">TPA2000D1PWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2000D1              |
| TPA2000D1PWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 2000D1              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

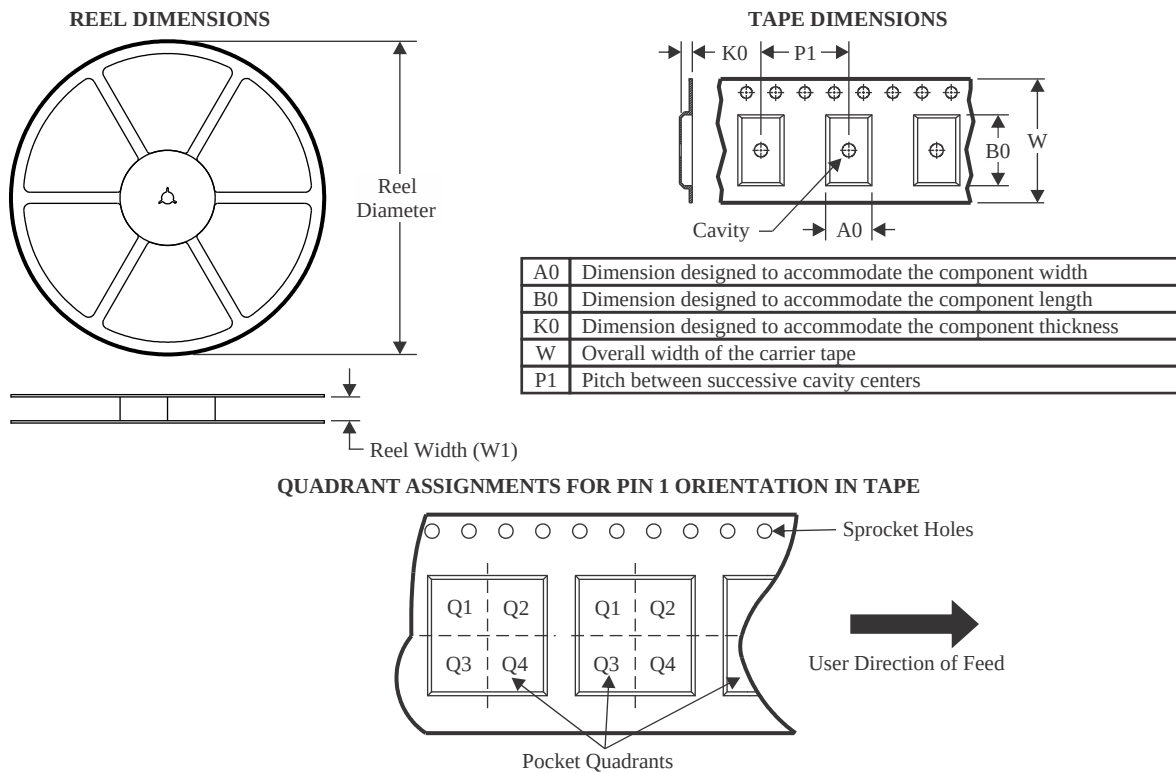
**OTHER QUALIFIED VERSIONS OF TPA2000D1 :**

- Automotive : [TPA2000D1-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

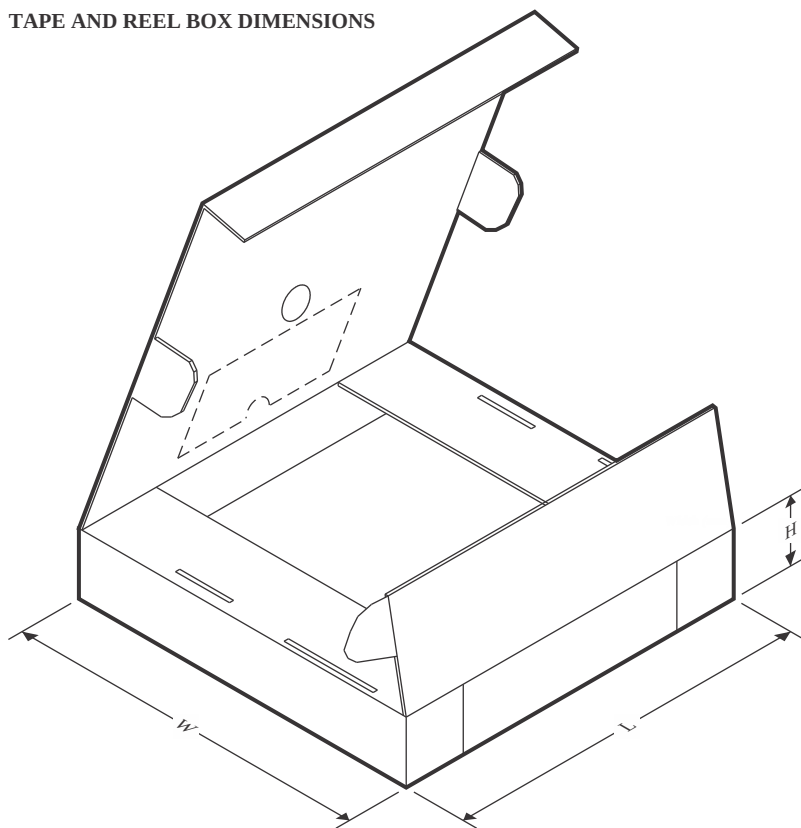
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPA2000D1PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

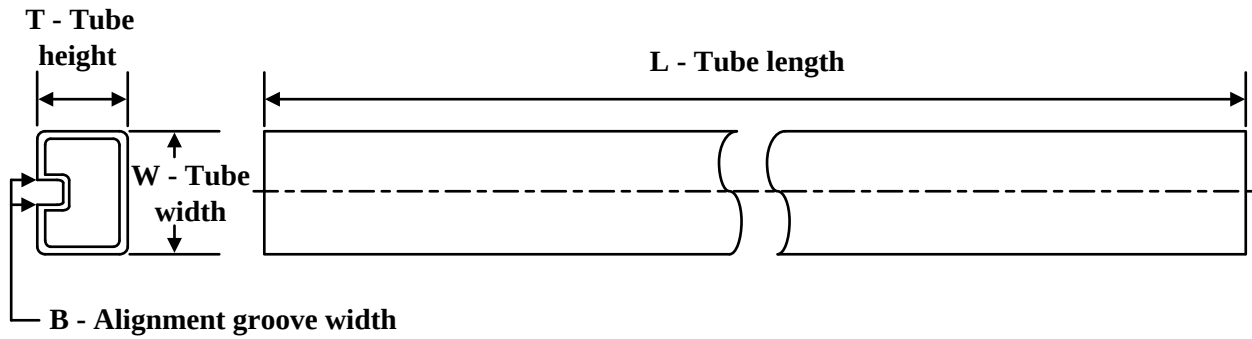
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

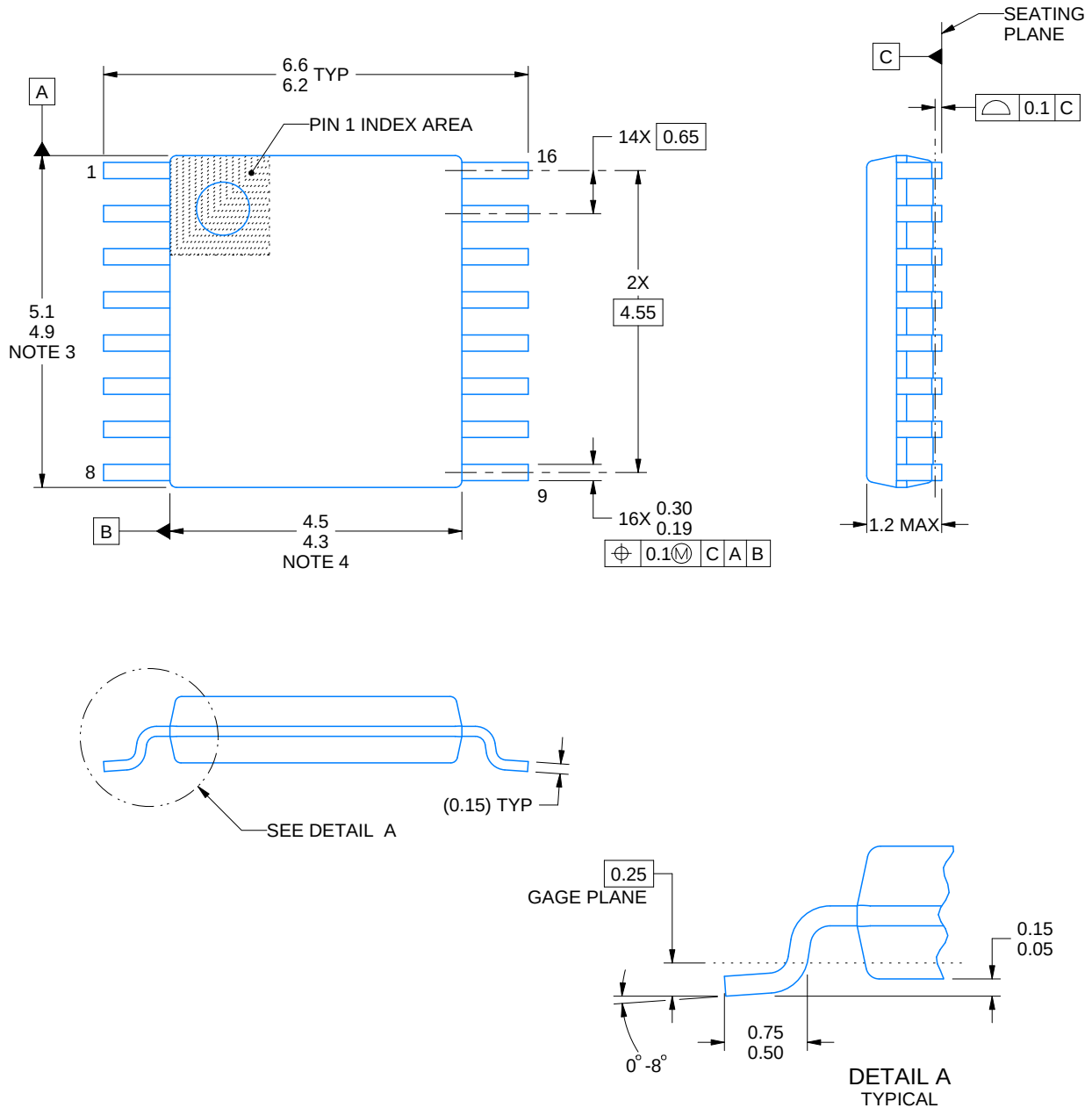
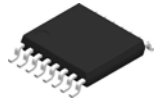
| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPA2000D1PWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPA2000D1PW   | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |
| TPA2000D1PW.A | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |



4220204/A 02/2017

## NOTES:

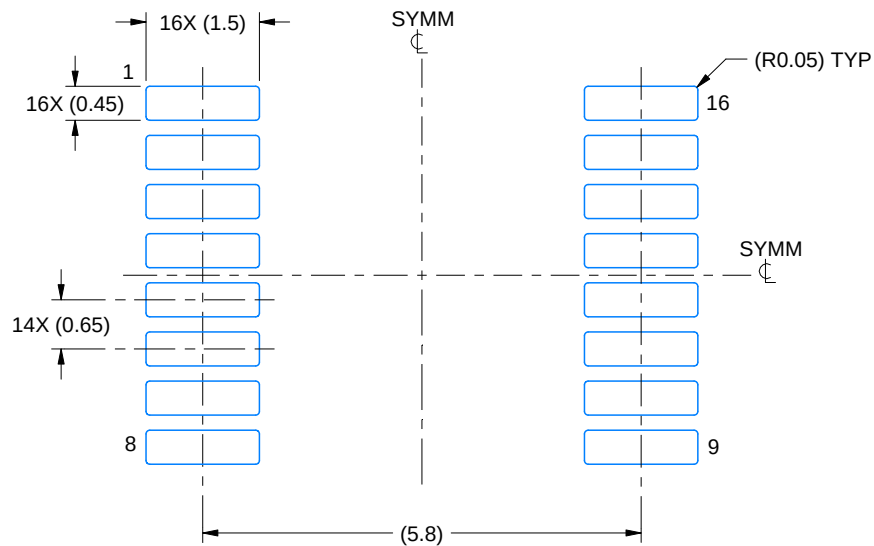
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

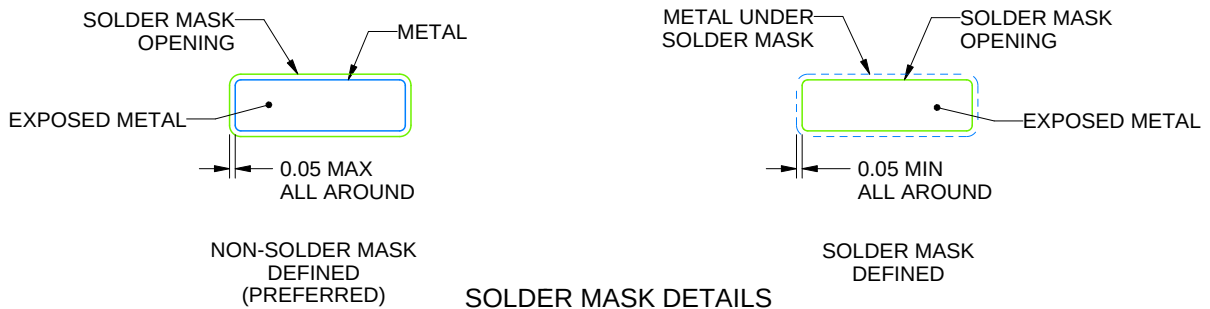
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

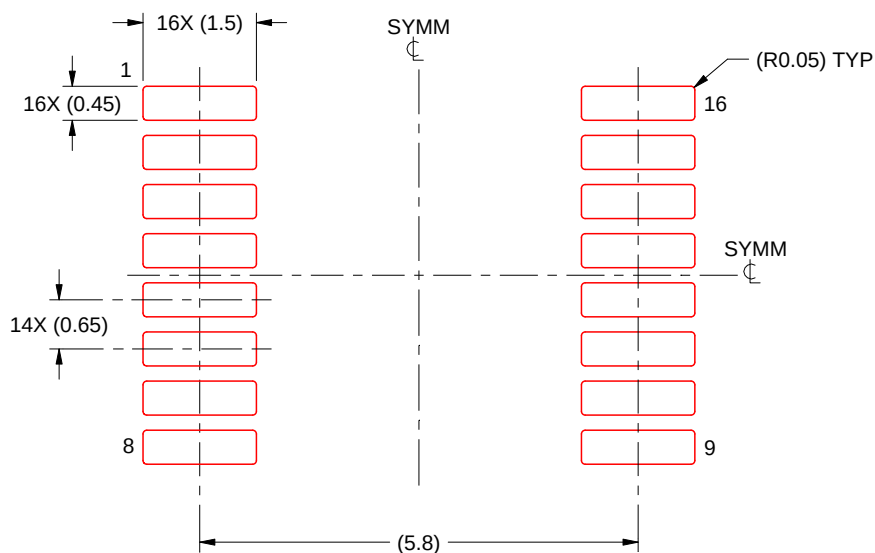
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated