UJA1078A

High-speed CAN/dual LIN core system basis chip

Rev. 3.0 — 10 December 2024 Product data sheet

1 General description

The UJA1078A core System Basis Chip (SBC) replaces the basic discrete components commonly found in Electronic Control Units (ECU) with a high-speed Controller Area Network (CAN) and two Local Interconnect Network (LIN) interfaces.

The UJA1078A supports the networking applications used to control power and sensor peripherals by using a high-speed CAN as the main network interface and the LIN interfaces as local sub-busses.

The core SBC contains the following integrated devices:

- High-speed CAN transceiver, inter-operable and downward compatible with CAN transceiver TJA1042, and compatible with the ISO 11898-2:2003 and ISO 11898-5:2006 standards
- LIN transceivers compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602, and compatible with LIN 1.3
- Advanced independent watchdog (variants with suffix W)
- 250 mA voltage regulator for supplying a microcontroller; extendable with external PNP transistor for increased current capability and dissipation distribution
- Separate voltage regulator for supplying the on-board CAN transceiver
- Serial Peripheral Interface (SPI) (full duplex)
- 2 local wake-up input ports
- Limp home output port

In addition to the advantages gained from integrating these common ECU functions in a single package, the core SBC offers an intelligent combination of system-specific functions such as:

- Advanced low-power concept
- Safe and controlled system start-up behavior
- Detailed status reporting on system and sub-system levels

The UJA1078A is designed to be used in combination with a microcontroller that incorporates a CAN controller. The SBC ensures that the microcontroller always starts up in a controlled manner.

2 Features and benefits

2.1 General

- Contains a full set of CAN and LIN ECU functions:
  - CAN transceiver and two LIN transceivers
  - Scalable 3.3 V or 5 V voltage regulator delivering up to 250 mA for a microcontroller and peripheral circuitry; an external PNP transistor can be connected for better heat distribution over the PCB
  - Separate voltage regulator for the CAN transceiver (5 V)
  - Watchdog with Window and Timeout modes and on-chip oscillator
  - Serial Peripheral Interface (SPI) for communicating with the microcontroller
  - ECU power management system
- Designed for automotive applications:
  - Enhanced ElectroMagnetic Compatibility (EMC) performance
  - ±8 kV ElectroStatic Discharge (ESD) protection Human Body Model (HBM) on the CAN/LIN bus pins and the wake-up pins
  - ±6 kV ElectroStatic Discharge protection IEC 61000-4-2 on the CAN/LIN bus pins and the wake-up pins
  - ±58 V short-circuit proof CAN/LIN bus pins
  - CAN/LIN bus pins are protected against transients in accordance with ISO 7637-3
- Supports remote flash programming via the CAN bus
- Small 6.1 mm × 11 mm HTSSOP32 package with low thermal resistance
- Pb-free; Restriction of Hazardous Substances Directive (RoHS) and dark green compliant

2.2 CAN transceiver

- ISO 11898-2:2003 and ISO 11898-5:2006 compliant high-speed CAN transceiver
- Dedicated low dropout voltage regulator for the CAN bus:
  - Independent of the microcontroller supply
  - Significantly improves EMC performance
- Bus connections are truly floating when power is off
- SPLIT output pin for stabilizing the recessive bus level

2.3 LIN transceivers

- 2 × LIN 2.2A compliant LIN transceivers
- Compliant with SAE J2602
- Downward compatible with LIN 2.2, LIN 2.1, LIN 2.0, LIN 1.3, LIN 1.2, LIN 1.1, LIN 1.0
- Low slope mode for optimized EMC performance
- Integrated LIN termination diode at pin DLIN

2.4 Power management

- Wake-up via CAN, LIN or local wake-up pins with wake-up source detection
- 2 wake-up pins:
  - WAKE1 and WAKE2 inputs can be switched off to reduce current flow
  - Output signal (WBIAS) to bias the wake-up pins, selectable sampling time of 16 ms or 64 ms
- Standby mode with very low standby current and full wake-up capability; V1 active to maintain supply to the microcontroller
- Sleep mode with very low sleep current and full wake-up capability

2.5 Control and diagnostic features

- Safe and predictable behavior under all conditions
- Programmable watchdog with independent clock source:
  - Window, Timeout (with optional cyclic wake-up) and Off modes supported (with automatic re-enable in the event of an interrupt)
- 16-bit Serial Peripheral Interface (SPI) for configuration, control and diagnosis
- Global enable output for controlling safety-critical hardware
- Limp home output (LIMP) for activating application-specific ‘limp home’ hardware in the event of a serious system malfunction
- Overtemperature shutdown
- Interrupt output pin; interrupts can be individually configured to signal V1/V2 undervoltage, CAN/LIN/local wake-up and cyclic and power-on interrupt events
- Bidirectional reset pin with variable power-on reset length to support a variety of microcontrollers
- Software-initiated system reset

2.6 Voltage regulators

- Main voltage regulator V1:
  - Scalable voltage regulator for the microcontroller, its peripherals and additional external transceivers
  - ±2 % accuracy
  - 3.3 V and 5 V versions available
  - Delivers up to 250 mA and can be combined with an external PNP transistor for better heat distribution over the PCB
  - Selectable current threshold at which the external PNP transistor starts to deliver current
  - Undervoltage warning at 90 % of nominal output voltage and undervoltage reset at 90 % or 70 % of nominal output voltage
  - Can operate at V_{BAT} voltages down to 4.5 V (e.g. during cranking), in accordance with ISO 7637 and ISO 16750-2
  - Stable output under all conditions
- Voltage regulator V2 for CAN transceiver:
  - Dedicated voltage regulator for on-chip high-speed CAN transceiver
  - Undervoltage warning at 90 % of nominal output voltage
  - Can be switched off; CAN transceiver can be supplied by V1 or by an external voltage regulator
  - Can operate at V_{BAT} voltages down to 5.5 V (e.g. during cranking) in accordance with ISO 7637
  - Stable output under all conditions

3 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
UJA1078ATW/3	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1
UJA1078ATW/3W			
UJA1078ATW/5			
UJA1078ATW/5W			

[1] UJA1078ATW/5x versions contain a 5 V regulator (V1); UJA1078ATW/3x versions contain a 3.3 V regulator (V1); versions with suffix W contain a watchdog.

4 Block diagram

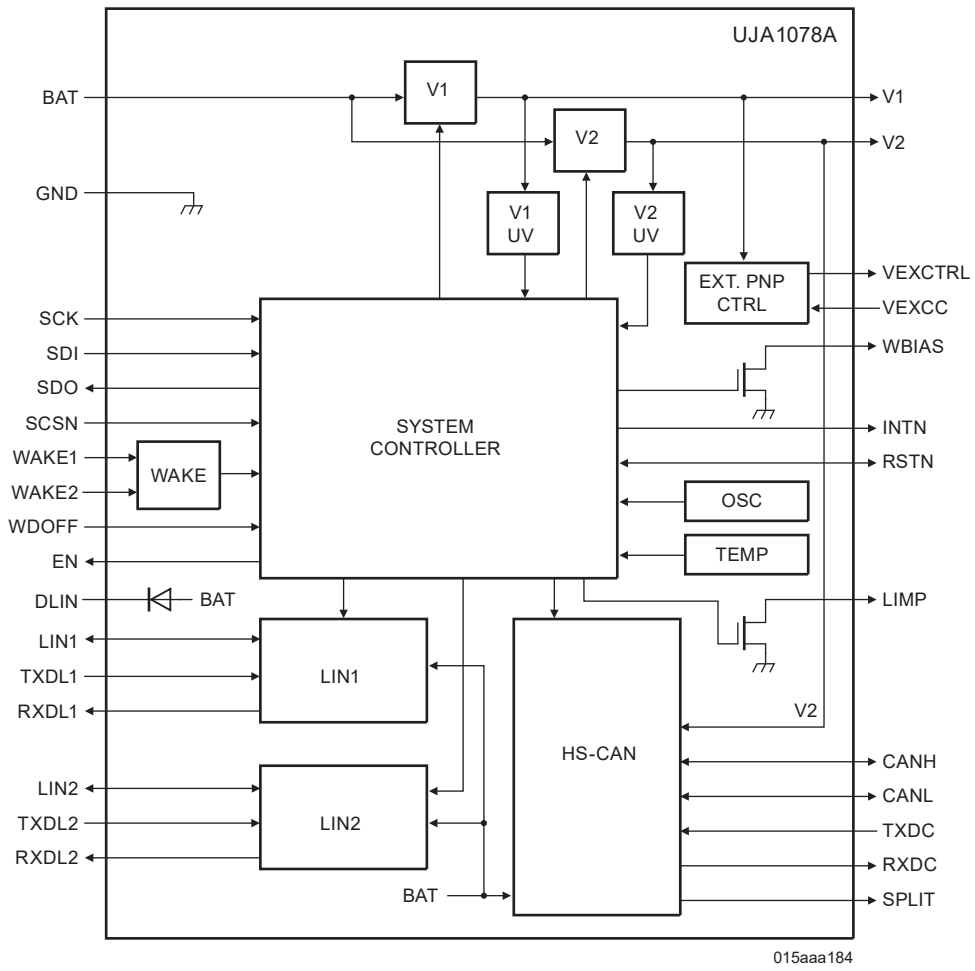


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

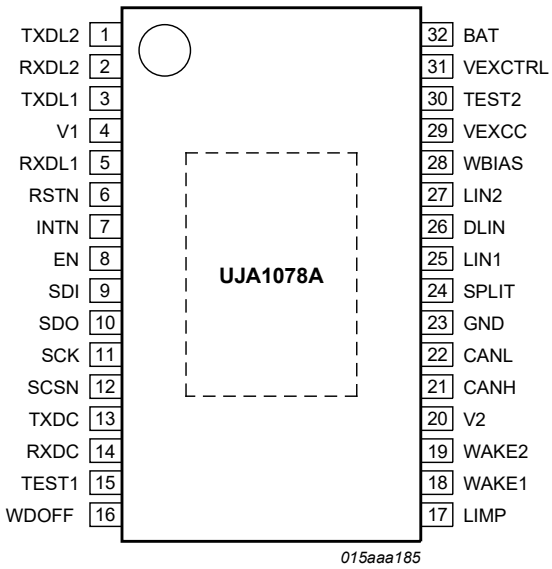


Figure 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
TXDL2	1	I	LIN2 transmit data input
RXDL2	2	O	LIN2 receive data output
TXDL1	3	I	LIN1 transmit data input
V1	4	AO	voltage regulator output for the microcontroller (5 V or 3.3 V depending on SBC version)
RXDL1	5	O	LIN1 receive data output
RSTN	6	IO	reset input/output to and from the microcontroller
INTN	7	O	interrupt output to the microcontroller
EN	8	O	enable output
SDI	9	I	SPI data input
SDO	10	O	SPI data output
SCK	11	I	SPI clock input
SCSN	12	I	SPI chip select input
TXDC	13	I	CAN transmit data input
RXDC	14	O	CAN receive data output
TEST1	15	G	test pin; pin should be connected to ground
WDOFF	16	I	WDOFF pin for deactivating the watchdog
LIMP	17	O	limp home output

Table 2. Pin description...*continued*

Symbol	Pin	Type[1]	Description
WAKE1	18	AI	local wake-up input 1
WAKE2	19	AI	local wake-up input 2
V2	20	AO	5 V voltage regulator output for CAN
CANH	21	AIO	CANH bus line
CANL	22	AIO	CANL bus line
GND[2]	23	G	ground
SPLIT	24	O	CAN bus common mode stabilization output
LIN1	25	AIO	LIN1 bus line
DLIN	26	AO	LIN termination resistor connection
LIN2	27	AIO	LIN2 bus line
WBIAS	28	AO	control pin for external wake biasing transistor
VEXCC	29	AI	current measurement for external PNP transistor; this pin is connected to the collector of the external PNP transistor
TEST2	30	G	test pin; pin should be connected to ground
VEXCTRL	31	AO	control pin of the external PNP transistor; this pin is connected to the base of the external PNP transistor
BAT	32	P	battery supply for the SBC

[1] I: digital input; O: digital output; IO: digital input/output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

6 Functional description

The UJA1078A combines the functionality of a high-speed CAN transceiver, two LIN transceivers, two voltage regulators and a watchdog (variants with suffix W) in a single, dedicated chip. It handles the power up and power down functionality of the ECU and ensures advanced system reliability. The SBC offers wake-up by bus activity, by cyclic wake-up and by the activation of external switches. Additionally, it provides a periodic control signal for pulsed testing of wake-up switches, allowing low-current operation even when the wake-up switches are closed in Standby mode.

All transceivers are optimized to be highly flexible with regard to bus topologies. In particular, the high-speed CAN transceiver is optimized to reduce ringing (bus reflections)[1].

V1, the main voltage regulator, is designed to power the ECU's microcontroller, its peripherals and additional external transceivers. An external PNP transistor can be added to improve heat distribution. V2 supplies the integrated high-speed CAN transceiver. The watchdog is clocked directly by the on-chip oscillator and can be operated in Window, Timeout and Off modes.

1 UJA1078A is not a CAN SIC transceiver.

6.1 System Controller

6.1.1 Introduction

The system controller manages register configuration and controls the internal functions of the SBC. Detailed device status information is collected and presented to the microcontroller. The system controller also provides the reset and interrupt signals.

The system controller is a state machine. The SBC operating modes, and how transitions between modes are triggered, are illustrated in Figure 3. These modes are discussed in more detail in the following sections.

6.1.2 Off mode

The SBC switches to Off mode from all other modes if the battery supply drops below the power-off detection threshold ($V_{th(det)poff}$). In Off mode, the voltage regulators are disabled and the bus systems are in a high-resistive state. The CAN bus pins are floating in this mode.

As soon as the battery supply rises above the power-on detection threshold ($V_{th(det)pon}$), the SBC goes to Standby mode, and a system reset is executed (reset pulse width of $t_{w(rst)}$, long or short; see Section 6.5.1 and Table 11).

6.1.3 Standby mode

The SBC will enter Standby mode:

- From Off mode if V_{BAT} rises above the power-on detection threshold ($V_{th(det)pon}$)
- From Sleep mode on the occurrence of a CAN, LIN or local wake-up event
- From Overtemp mode if the chip temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$
- From Normal mode if bit MC is set to 00 or a system reset is performed (see Section 6.5)

In Standby mode, V1 is switched on. The CAN and LIN transceivers will either be in a low-power state (Lowpower mode; STBCC/STBCL1/STBCL2 = 1; see Table 6) with bus wake-up detection enabled or completely switched off (Off mode; STBCx = 0) - see Section 6.7.1 and Section 6.8.1. The watchdog can be running in Timeout mode or Off mode, depending on the state of the WDOFF pin and the setting of the watchdog mode control bit (WMC) in the WD_and_Status register (Table 4).

The SBC will exit Standby mode if:

- Normal mode is selected by setting bits MC to 10 (V2 disabled) or 11 (V2 enabled)
- Sleep mode is selected by setting bits MC to 01
- The chip temperature rises above the OverTemperature Protection (OTP) activation threshold, $T_{th(act)otp}$, causing the SBC to enter Overtemp mode

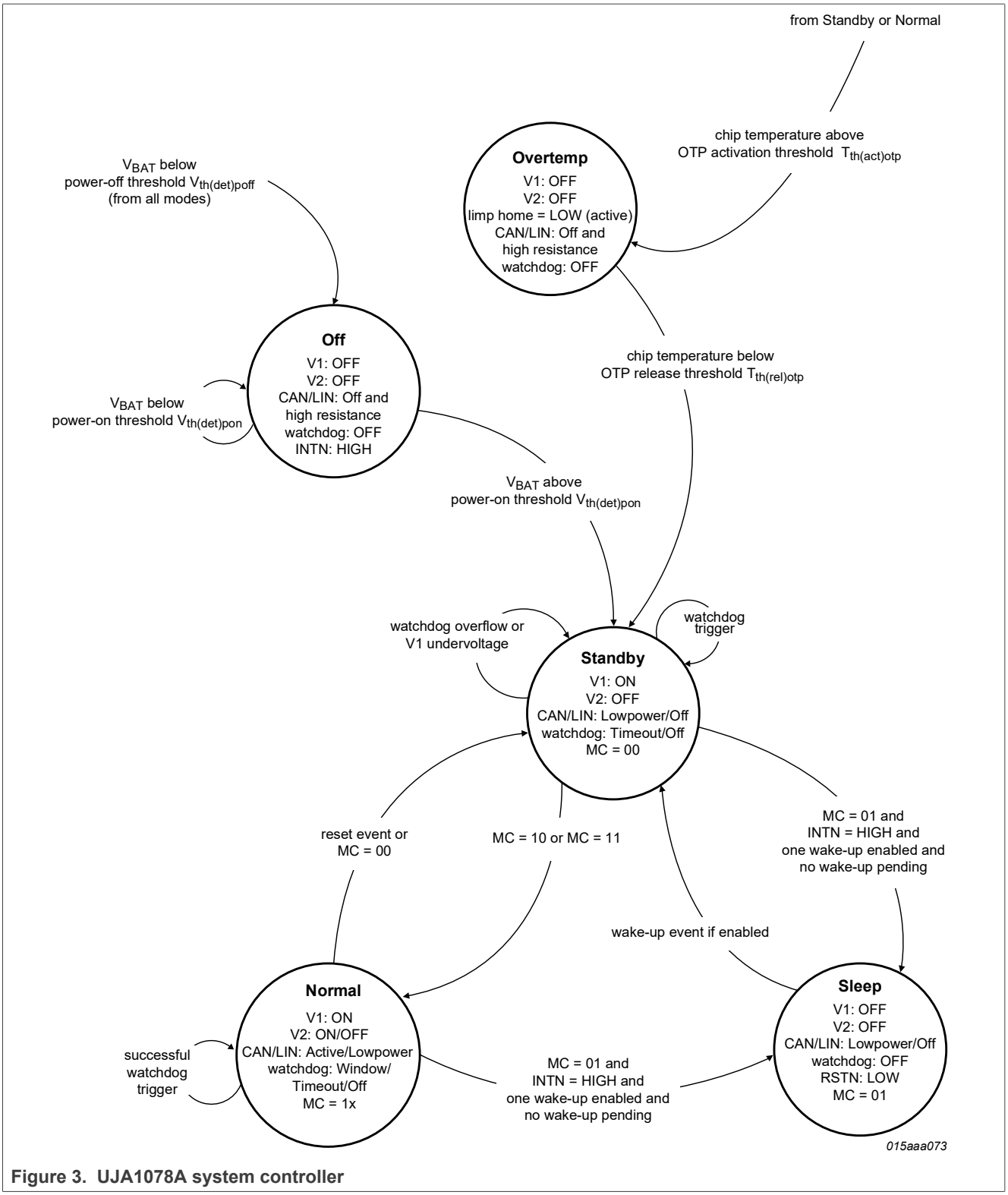


Figure 3. UJA1078A system controller

6.1.4 Normal mode

Normal mode is selected from Standby mode by setting bits MC in the Mode_Control register (Table 5) to 10 (V2 disabled) or 11 (V2 enabled).

In Normal mode, the CAN physical layer will be enabled (Active mode; STBCC = 0; see Table 6) or in a low-power state (Lowpower mode; STBCC = 1) with bus wake-up detection active.

In Normal mode, the LIN physical layers (LIN1 and LIN2) will be enabled (Active mode; STBCL1/STBCL2 = 0; see Table 6) or in a low-power state (Lowpower mode; STBCL1/STBCL2 = 1) with bus wake-up detection active.

The SBC will exit Normal mode if:

- Standby mode is selected by setting bits MC to 00
- Sleep mode is selected by setting bits MC to 01
- A system reset is generated (see Section 6.1.3; the SBC will enter Standby mode)
- The chip temperature rises above the OTP activation threshold, $T_{th(act)otp}$, causing the SBC to switch to Overtemp mode

6.1.5 Sleep mode

Sleep mode is selected from Standby mode or Normal mode by setting bits MC in the Mode_Control register (Table 5) to 01. The SBC will enter Sleep mode provided that there are no pending interrupts (pin INTN = HIGH) or wake-up events and at least one wake-up source is enabled (CAN, LIN or WAKE). Any attempt to enter Sleep mode while one of these conditions has not been satisfied will result in a short reset (3.6 ms minimum pulse width; see Section 6.5.1 and Table 11).

In Sleep mode, V1 and V2 are off and the bus transceivers will be switched off (Off mode; STBCx = 0; see Table 6) or in a low-power state (Lowpower mode; STBCx = 1) with bus wake-up detection active - see Section 6.7.1 and Section 6.8.1). The watchdog is off and the reset pin is LOW.

A CAN, LIN or local wake-up event will cause the SBC to switch from Sleep mode to Standby mode, generating a (short or long; see Section 6.5.1) system reset. The value of the mode control bits (MC) will be changed to 00 and V1 will be enabled.

6.1.6 Overtemp mode

The SBC will enter Overtemp mode from Normal mode or Standby mode when the chip temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$.

In Overtemp mode, the voltage regulators are switched off and the bus systems are in a high-resistive state. When the SBC enters Overtemp mode, the RSTN pin is driven LOW and the limp home control bit, LHC, is set so that the LIMP pin is driven LOW.

The chip temperature must drop a hysteresis level below the overtemperature shutdown threshold before the SBC can exit Overtemp mode. After leaving Overtemp mode the SBC enters Standby mode and a system reset is generated (reset pulse width of $t_{w(rst)}$, long or short; see Section 6.5.1 and Table 11).

6.2 SPI

6.2.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock; default level is LOW due to low-power concept
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge (see Figure 4).

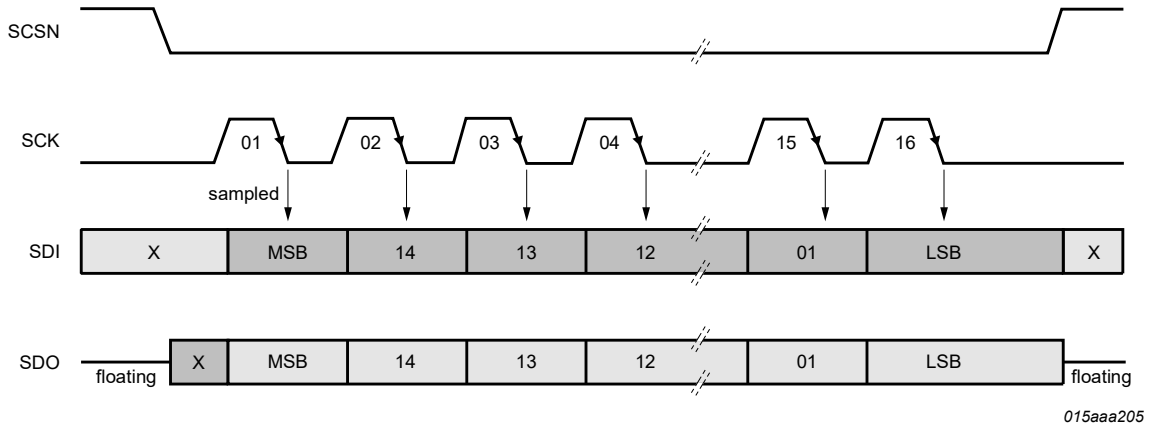


Figure 4. SPI timing protocol

6.2.2 Register map

The first three bits (A2, A1 and A0) of the message header define the register address. The fourth bit (RO) defines the selected register as read/write or read only.

Table 3. Register map

Address bits 15, 14 and 13	Write access bit 12 = 0	Read/Write access bits 11... 0
000	0 = read/write, 1 = read only	WD_and_Status register
001	0 = read/write, 1 = read only	Mode_Control register
010	0 = read/write, 1 = read only	Int_Control register
011	0 = read/write, 1 = read only	Int_Status register

6.2.3 WD_and_Status register

Table 4. WD_and_Status register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	000	register address

Table 4. WD_and_Status register...*continued*

Bit	Symbol	Access	Power-on default	Description
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	WMC	R/W	0	watchdog mode control
				0: Normal mode: watchdog in Window mode; Standby mode: watchdog in Timeout mode
				1: Normal mode: watchdog in Timeout mode; Standby mode: watchdog in Off mode
10:8	NWP[1]	R/W	100	nominal watchdog period
				000: 8 ms
				001: 16 ms
				010: 32 ms
				011: 64 ms
				100: 128 ms
				101: 256 ms
				110: 1024 ms
				111: 4096 ms
7	WOS/SWR	R/W	-	watchdog off status/software reset
				0: WDOFF pin LOW; watchdog mode determined by bit WMC
				1: watchdog disabled due to HIGH level on pin WDOFF; results in software reset
6	V1S	R	-	V1 status
				0: V1 output voltage above 90 % undervoltage recovery threshold (V_{uvr}; see Table 10)
				1: V1 output voltage below 90 % undervoltage detection threshold (V_{uvd}; see Table 10)
5	V2S	R	-	V2 status
				0: V2 output voltage above undervoltage release threshold (V_{uvr}; see Table 10)
				1: V2 output voltage below undervoltage detection threshold (V_{uvd}; see Table 10)
4	WLS1	R	-	wake-up 1 status
				0: WAKE1 input voltage below switching threshold ($V_{th(sw)}$)
				1: WAKE1 input voltage above switching threshold ($V_{th(sw)}$)
3	WLS2	R	-	wake-up 2 status
				0: WAKE2 input voltage below switching threshold ($V_{th(sw)}$)
				1: WAKE2 input voltage above switching threshold ($V_{th(sw)}$)
2:0	reserved	R	000	

[1] Bit NWP is set to its default value (100) after a reset.

6.2.4 Mode_Control register

Table 5. Mode_Control register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	001	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11:10	MC	R/W	00	mode control
				00: Standby mode
				01: Sleep mode
				10: Normal mode; V2 off
				11: Normal mode; V2 on
9	LHWC[1]	R/W	1	limp home warning control
				0: no limp home warning
				1: limp home warning is set; next reset will activate LIMP output
8	LHC[2]	R/W	0	limp home control
				0: LIMP pin set floating
				1: LIMP pin driven LOW
7	ENC	R/W	0	enable control
				0: EN pin driven LOW
				1: EN pin driven HIGH in Normal mode
6	LSC	R/W	0	LIN slope control
				0: normal slope, 20 kbit/s
				1: low slope, 10.4 kbit/s
5	WBC	R/W	0	wake bias control
				0: pin WBIAS floating if WSEn = 0; 16 ms sampling if WSEn = 1
				1: pin WBIAS LOW if WSEn = 0; 64 ms sampling if WSEn = 1
4	PDC	R/W	0	power distribution control
				0: V1 threshold current for activating the external PNP transistor, load current rising; $I_{th(act)PNP}$ = 85 mA (typ. at T_{vj} = 150 °C); V1 threshold current for deactivating the external PNP transistor, load current falling; $I_{th(deact)PNP}$ = 50 mA (typ. at T_{vj} = 150 °C); see Figure 7
				1: V1 threshold current for activating the external PNP transistor; load current rising; $I_{th(act)PNP}$ = 50 mA (typ. at T_{vj} = 150 °C); V1 threshold current for deactivating the external PNP transistor; load current falling; $I_{th(deact)PNP}$ = 15 mA (typ. at T_{vj} = 150 °C); see Figure 7
3:0	reserved	R	0000	

[1] Bit LHWC is set to 1 after a reset.

[2] Bit LHC is set to 1 after a reset, if LHWC was set to 1 prior to the reset.

6.2.5 Int_Control register

Table 6. Int_Control register

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	010	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	V1UIE	R/W	0	V1 undervoltage interrupt enable
				0: V1 undervoltage warning interrupts cannot be requested
				1: V1 undervoltage warning interrupts can be requested
10	V2UIE	R/W	0	V2 undervoltage interrupt enable
				0: V2 undervoltage warning interrupts cannot be requested
				1: V2 undervoltage warning interrupts can be requested
9	STBCL1	R/W	0	LIN1 standby control
				0: When the SBC is in Normal mode (MC = 1x): LIN1 is in Active mode. The wake-up flag (visible on RXDL1) is cleared regardless of the value of V_{BAT}. When the SBC is in Standby/Sleep mode (MC = 0x): LIN1 is in Off mode. Bus wake-up detection is disabled. LIN1 wake-up interrupts cannot be requested.
				1: LIN1 is in Lowpower mode with bus wake-up detection enabled, regardless of the SBC mode (MC = xx). LIN1 wake-up interrupts can be requested.
8	STBCL2	R/W	0	LIN2 standby control
				0: When the SBC is in Normal mode (MC = 1x): LIN2 is in Active mode. The wake-up flag (visible on RXDL2) is cleared regardless of the value of V_{BAT}. When the SBC is in Standby/Sleep mode (MC = 0x): LIN2 is in Off mode. Bus wake-up detection is disabled. LIN2 wake-up interrupts cannot be requested.
				1: LIN2 is in Lowpower mode with bus wake-up detection enabled, regardless of the SBC mode (MC = xx). LIN2 wake-up interrupts can be requested.
7:6	WIC1	R/W	00	wake-up interrupt 1 control
				00: wake-up interrupt 1 disabled
				01: wake-up interrupt 1 on rising edge
				10: wake-up interrupt 1 on falling edge
				11: wake-up interrupt 1 on both edges
5:4	WIC2	R/W	00	wake-up interrupt 2 control
				00: wake-up interrupt 2 disabled

Table 6. Int_Control register...*continued*

Bit	Symbol	Access	Power-on default	Description
				01: wake-up interrupt 2 on rising edge
				10: wake-up interrupt 2 on falling edge
				11: wake-up interrupt 2 on both edges
3	STBCC	R/W	0	CAN standby control
				0: When the SBC is in Normal mode (MC = 1x): CAN is in Active mode. The wake-up flag (visible on RXDC) is cleared regardless of V2 output voltage. When the SBC is in Standby/Sleep mode (MC = 0x): CAN is in Off mode. Bus wake-up detection is disabled. CAN wake-up interrupts cannot be requested.
				1: CAN is in Lowpower mode with bus wake-up detection enabled, regardless of the SBC mode (MC = xx). CAN wake-up interrupts can be requested.
2	RTHC	R/W	0	reset threshold control
				0: The reset threshold is set to the 90 % V1 undervoltage detection voltage (V_{uvd}; see Table 10)
				1: The reset threshold is set to the 70 % V1 undervoltage detection voltage (V_{uvd}; see Table 10)
1	WSE1	R/W	0	WAKE1 sample enable
				0: sampling continuously
				1: sampling of WAKE1 is synchronized with WBIAS (sample rate controlled by WBC)
0	WSE2	R/W	0	WAKE2 sample enable
				0: sampling continuously
				1: sampling of WAKE1 is synchronized with WBIAS (sample rate controlled by WBC)

6.2.6 Int_Status register

Table 7. Int_Status register[1]

Bit	Symbol	Access	Power-on default	Description
15:13	A2, A1, A0	R	011	register address
12	RO	R/W	0	access status
				0: register set to read/write
				1: register set to read only
11	V1UI	R/W	0	V1 undervoltage interrupts
				0: no V1 undervoltage warning interrupt pending
				1: V1 undervoltage warning interrupt pending
10	V2UI	R/W	0	V2 undervoltage interrupts
				0: no V2 undervoltage warning interrupt pending

Table 7. Int_Status register[1]*...continued*

Bit	Symbol	Access	Power-on default	Description
				1: V2 undervoltage warning interrupt pending
9	LWI1	R/W	0	LIN wake-up interrupt 1
				0: no LIN1 wake-up interrupt pending
				1: LIN1 wake-up interrupt pending
8	LWI2	R/W	0	LIN wake-up interrupt 2
				0: no LIN2 wake-up interrupt pending
				1: LIN2 wake-up interrupt pending
7	CI	R/W	0	cyclic interrupt
				0: no cyclic interrupt pending
				1: cyclic interrupt pending
6	WI1	R/W	0	wake-up interrupt 1
				0: no wake-up interrupt 1 pending
				1: wake-up interrupt 1 pending
5	POSI	R/W	1	power-on status interrupt
				0: no power-on interrupt pending
				1: power-on interrupt pending
4	WI2	R/W	0	wake-up interrupt 2
				0: no wake-up interrupt 2 pending
				1: wake-up interrupt 2 pending
3	CWI	R/W	0	CAN wake-up interrupt
				0: no CAN wake-up interrupt pending
				1: CAN wake-up interrupt pending
2:0	reserved	R	000	

[1] An interrupt can be cleared by writing 1 to the relevant bit in the Int_Status register.

6.3 On-chip oscillator

The on-chip oscillator provides the timing reference for the on-chip watchdog and the internal timers. The on-chip oscillator is supplied by an internal supply that is connected to V_{BAT} and is independent of V1/V2.

6.4 Watchdog (variants with suffix W)

Three watchdog modes are supported: Window, Timeout and Off. The watchdog period is programmed via the NWP control bits in the WD_and_Status register (see Table 4). The default watchdog period is 128 ms.

A watchdog trigger event is any write access to the WD_and_Status register. When the watchdog is triggered, the watchdog timer is reset.

In watchdog Window mode, a watchdog trigger event within a closed watchdog window (i.e. the first half of the window before $t_{trig(wd)1}$) will generate an SBC reset. If the watchdog is triggered before the watchdog timer

overflows in Timeout or Window mode, or within the open watchdog window (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the timer restarts immediately.

The following watchdog events result in an immediate system reset:

- the watchdog overflows in Window mode
- the watchdog is triggered in the first half of the watchdog period in Window mode
- the watchdog overflows in Timeout mode while a cyclic interrupt (CI) is pending
- the state of the WDOFF pin changes in Normal mode or Standby mode
- the watchdog mode control bit (WMC) changes state in Normal mode

After a watchdog reset (short reset; see Section 6.5.1 and Table 11), the default watchdog period is selected (NWP = 100). The watchdog can be switched off completely by forcing pin WDOFF HIGH. The watchdog can also be switched off by setting bit WMC to 1 in Standby mode. If the watchdog was turned off by setting WMC, any pending interrupt will re-enable it.

Note that the state of bit WMC cannot be changed in Standby mode if an interrupt is pending. Any attempt to change WMC when an interrupt is pending will be ignored.

6.4.1 Watchdog Window behavior

The watchdog runs continuously in Window mode.

If the watchdog overflows, or is triggered in the first half of the watchdog period (less than $t_{trig(wd)1}$ after the start of the watchdog period), a system reset will be performed. Watchdog overflow occurs if the watchdog is not triggered within $t_{trig(wd)2}$ after the start of the watchdog period.

If the watchdog is triggered in the second half of the watchdog period (at least $t_{trig(wd)1}$, but not more than $t_{trig(wd)2}$, after the start of the watchdog period), the watchdog will be reset.

The watchdog is in Window mode when pin WDOFF is LOW, the SBC is in Normal mode and the watchdog mode control bit (WMC) is set to 0.

6.4.2 Watchdog Timeout behavior

The watchdog runs continuously in Timeout mode. It can be reset at any time by a watchdog trigger. If the watchdog overflows, the CI bit is set. If a CI is already pending, a system reset is performed.

The watchdog is in Timeout mode when pin WDOFF is LOW and:

- the SBC is in Standby mode and bit WMC = 0 or
- the SBC is in Normal mode and bit WMC = 1

6.4.3 Watchdog Off behavior

The watchdog is disabled in this state.

The watchdog is in Off mode when:

- the SBC is in Off, Overtemp or Sleep modes
- the SBC is in Standby mode and bit WMC = 1
- the SBC is in any mode and the WDOFF pin is HIGH

6.5 System reset

The following events will cause the SBC to perform a system reset:

- V1 undervoltage (reset pulse length selected via external pull-up resistor on RSTN pin)

- An external reset (pin RSTN forced LOW)
- Watchdog overflow (Window mode)
- Watchdog overflow in Timeout mode with CI pending
- Watchdog triggered too early in Window mode
- WMC value changed in Normal mode
- WDOFF pin state changed
- SBC goes to Sleep mode (MC set to 01; see Table 5) while pin INTN is driven LOW
- SBC goes to Sleep mode (MC set to 01; see Table 5) while STBCC = STBCL1 = STBCL2 = WIC1 = WIC2 = 0
- SBC goes to Sleep mode (MC set to 01; see Table 5) while wake-up pending
- Software reset (SWR = 1)
- SBC leaves Overtemp mode (reset pulse length selected via external pull-up resistor on RSTN pin)

A watchdog overflow in Timeout mode requests a CI, if a CI is not already pending.

The UJA1078A provides three signals for dealing with reset events:

- RSTN pin input/output for performing a global ECU system reset or forcing an external reset
- EN pin, a fail-safe global enable output
- LIMP pin, a fail-safe limp home output

6.5.1 RSTN pin

A system reset is triggered if the bidirectional RSTN pin is forced LOW for at least t_{fltr} by the microcontroller (external reset). A reset pulse is output on pin RSTN by the SBC when a system reset is triggered internally.

The reset pulse width ($t_{w(rst)}$) is selectable (short or long) if the system reset was generated by a V1 undervoltage event (see Section 6.6.2) or by the SBC leaving Off ($V_{BAT} > V_{th(det)pon}$) or Overtemp (temperature < $T_{th(rel)otp}$) modes. A short reset pulse is selected by connecting a 1000 Ω ±10 % resistor between pins RSTN and V1. If a resistor is not connected, the reset pulse will be long (see Table 11).

In all other cases (e.g. watchdog-related reset events) the reset pulse length will be short.

6.5.2 EN output

The EN pin can be used to control external hardware, such as power components, or as a general-purpose output when the system is running properly.

In Normal and Standby modes, the microcontroller can set the EN control bit (bit ENC in the Mode_Control register; see Table 5) via the SPI interface. Pin EN will be HIGH when ENC = 1 and MC = 10 or 11. A reset event will cause pin EN to go LOW. EN pin behavior is illustrated in Figure 5.

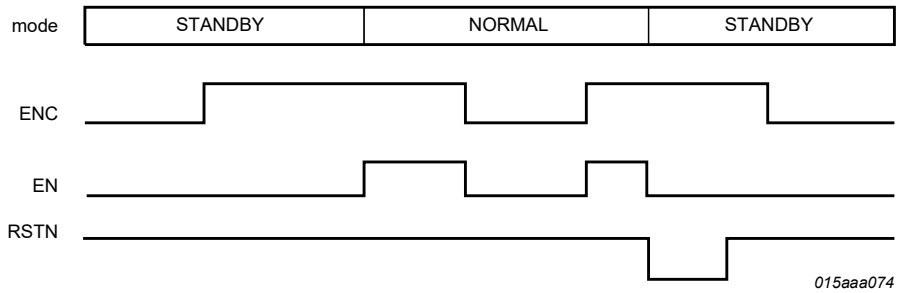


Figure 5. Behavior of EN pin

6.5.3 LIMP output

The LIMP pin can be used to enable the so called ‘limp home’ hardware in the event of an ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, pins RSTN or V1 clamped LOW and user-initiated or external reset events.

The LIMP pin is a battery-related, active-LOW, open-drain output.

A system reset will cause the limp home warning control bit (bit LHWC in the Mode_Control register; see Table 5) to be set. If LHWC is already set when the system reset is generated, bit LHC will be set which will force the LIMP pin LOW. The application should clear LHWC after each reset event to ensure the LIMP output is not activated during normal operation.

In Overtemp mode, bit LHC is always set and, consequently, the LIMP output is always active. If the application manages to recover from the event that activated the LIMP output, LHC can be cleared to deactivate the LIMP output.

6.6 Power supplies

6.6.1 Battery pin (BAT)

The SBC contains a single supply pin, BAT. An external diode is needed in series to protect the device against negative voltages. The operating range is from 4.5 V to 28 V. The SBC can handle maximum voltages up to 40 V.

If the voltage on pin BAT falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC immediately enters Off mode, which means that the voltage regulators and the internal logic are shut down. The SBC leaves Off mode for Standby mode as soon as the voltage rises above the power-on detection threshold, $V_{th(det)pon}$. The POSI bit in the Int_Status register is set to 1 when the SBC leaves Off mode.

6.6.2 Voltage regulator V1

Voltage regulator V1 is intended to supply the microcontroller, its periphery and additional transceivers. V1 is supplied by pin BAT and delivers up to 250 mA at 3.3 V or 5 V (depending on the UJA1078A variant).

To prevent the device overheating at high ambient temperatures or high average currents, an external PNP transistor can be connected as illustrated in Figure 6. In this configuration, the power dissipation is distributed between the SBC and the PNP transistor.

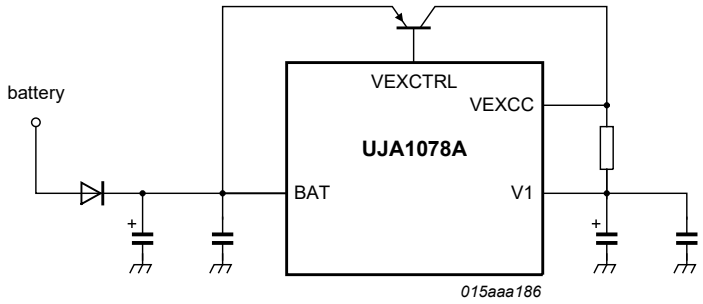


Figure 6. External PNP transistor control circuit

Pin VEXCTRL activates the PNP transistor with an initial current and slowly increases that current while the V1 output current is above the PNP activation threshold, $I_{th(act)PNP}$. Bit PDC in the Mode_Control register (Table 5) is used to regulate how power dissipation is distributed. The PNP activation threshold is 85 mA when PDC = 0 and 50 mA when PDC = 1 (typ. at T_{vj} = 150 °C). V1 will continue to deliver $I_{th(act)PNP}$ while the transistor delivers the additional load current (see Figure 7 and Figure 8).

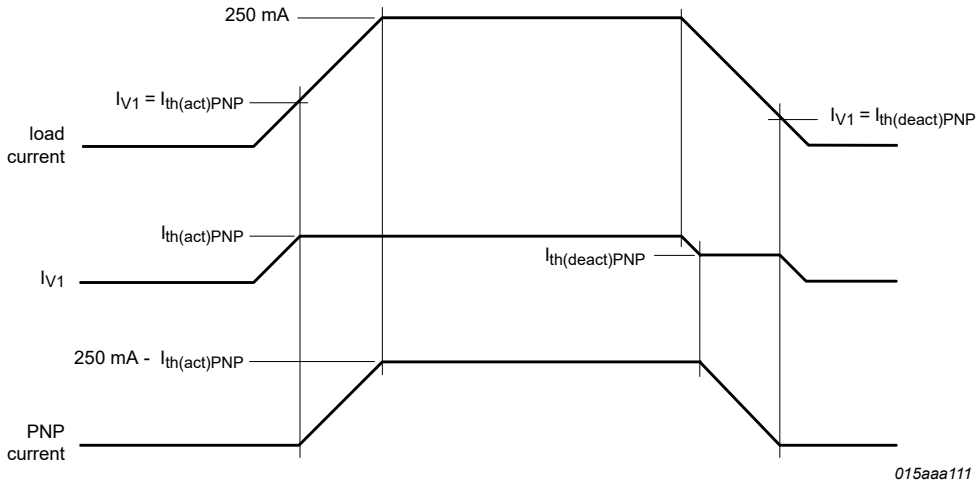


Figure 7. V1 and PNP currents at a slow ramping load current of 250 mA

Figure 7 illustrates how V1 and the PNP transistor combine to supply a slow-ramping load current of 250 mA. V1 supplies the load current up to $I_{th(act)PNP}$. Any additional load current requirement is provided by the PNP transistor, up to its current limit. If the load current continues to rise after the PNP current limit has been reached, I_{V1} will increase above the selected PDC threshold (to a maximum of 250 mA).

For a fast ramping load current, V1 will deliver the required load current (to a maximum of 250 mA) until the PNP transistor has switched on. Once the transistor has been activated, V1 will deliver at least $I_{th(act)PNP}$, with the transistor contributing the balance of the load current (see Figure 8).

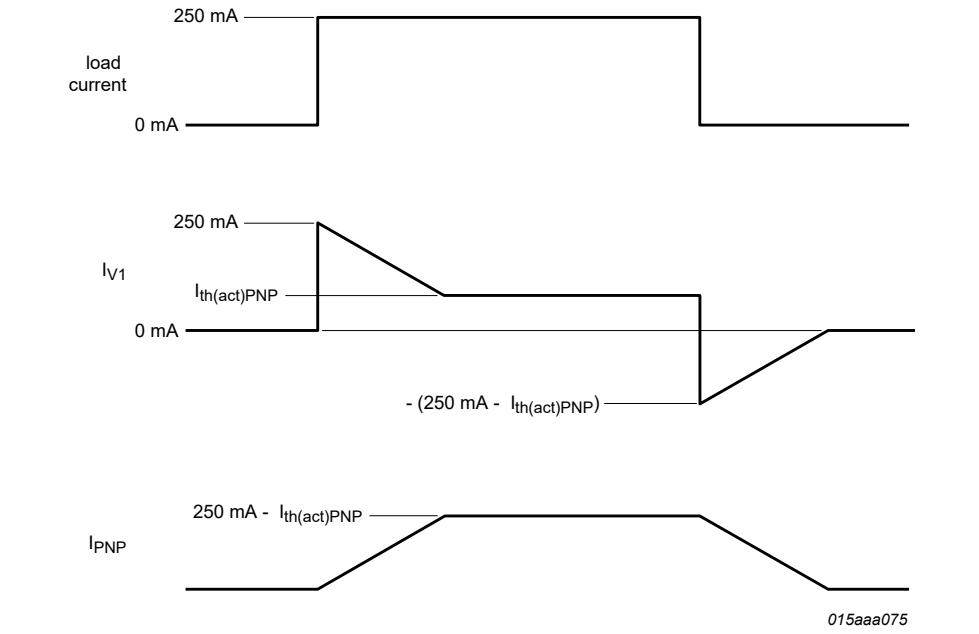


Figure 8. V1 and PNP currents at a fast ramping load current of 250 mA

For short-circuit protection, a resistor needs to be connected between pins V1 and VEXCC to allow the current to be monitored. This resistor limits the current delivered by the external transistor. If the voltage difference between pins VEXCC and V1 reaches $V_{th(act)Ilim}$, the PNP current-limiting activation threshold voltage, the transistor base current (on pin VEXCTRL) will not increase further.

The thermal performance of the transistor needs to be considered when calculating the value of this resistor. A 3.3 Ω resistor was used with the BCP52-16 employed during testing. Note that the selection of the transistor is not critical. In general, any PNP transistor with a current amplification factor (β) of between 60 and 500 can be used.

If an external PNP transistor is not used, pin VEXCC must be connected to V1 while pin VEXCTRL can be left open.

One advantage of this scalable voltage regulator concept is that there are no PCB layout restrictions when using the external PNP. The distance between the UJA1078A and the external PNP doesn't affect the stability of the regulator loop because the loop is realized within the UJA1078A. Therefore, it is recommended that the distance between the UJA1078A and PNP transistor be maximized for optimal thermal distribution.

The output voltage on V1 is monitored continuously and a system reset signal is generated if an undervoltage event occurs. A system reset is generated if the voltage on V1 falls below the undervoltage detection voltage (V_{uvd}; see Table 10). The reset threshold (90 % or 70 % of the nominal value) is set via the Reset Threshold Control bit (RTHC) in the Int_Control register (Table 6). In addition, an undervoltage warning (a V1UI interrupt) will be generated at 90 % of the nominal output voltage. The status of V1 can be read via bit V1S in the WD_and_Status register (Table 4).

6.6.3 Voltage regulator V2

Voltage regulator V2 is reserved for the high-speed CAN transceiver, providing a 5 V supply.

V2 can be activated and deactivated via the MC bits in the Mode_Control register (Table 5). An undervoltage warning (a V2UI interrupt) is generated when the output voltage drops below 90 % of its nominal value. The status of V2 can be read via bit V2S in the WD_and_Status register (Table 4) in Normal mode (V2S = 1 in all other modes).

V2 can be deactivated (MC = 10) to allow the internal CAN transceiver to be supplied from an external source or from V1. The alternative voltage source must be connected to pin V2. All internal functions (e.g. undervoltage protection) will work normally.

6.7 CAN transceiver

The analog section of the UJA1078A CAN transceiver corresponds to that integrated into the TJA1042/ TJA1043. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to a CAN protocol controller.

6.7.1 CAN operating modes

6.7.1.1 Active mode

The CAN transceiver is in Active mode when:

- the SBC is in Normal mode (MC = 10 or 11)
- the transceiver is enabled (bit STBCC = 0; see Table 6)

and

- V2 is enabled and its output voltage is above its undervoltage threshold, V_{uvd}
  or
- V2 is disabled but an external voltage source, or V1, connected to pin V2 is above its undervoltage threshold (see Section 6.6.3)

In CAN Active mode, the transceiver can transmit and receive data via the CANH and CANL pins. The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXDC. The

transmitter converts digital data generated by a CAN controller, and input on pin TXDC, to signals suitable for transmission over the bus lines.

6.7.1.2 Lowpower/Off modes

The CAN transceiver will be in Lowpower mode with bus wake-up detection enabled if bit STBCC = 1 (see Table 6). The CAN transceiver can be woken up remotely via pins CANH and CANL in Lowpower mode.

When the SBC is in Standby mode or Sleep mode (MC = 00 or 01), the CAN transceiver will be in Off mode if bit STBCC = 0. The CAN transceiver is powered down completely in Off mode to minimize quiescent current consumption.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or electromagnetic interference (EMI).

A recessive-dominant-recessive-dominant sequence must occur on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 9; note that additional pulses may occur between the recessive/dominant phases). The minimum recessive/dominant bus times for CAN transceiver wake-up ($t_{wake(busrec)min}$ and $t_{wake(busdom)min}$) must be satisfied (see Table 11).

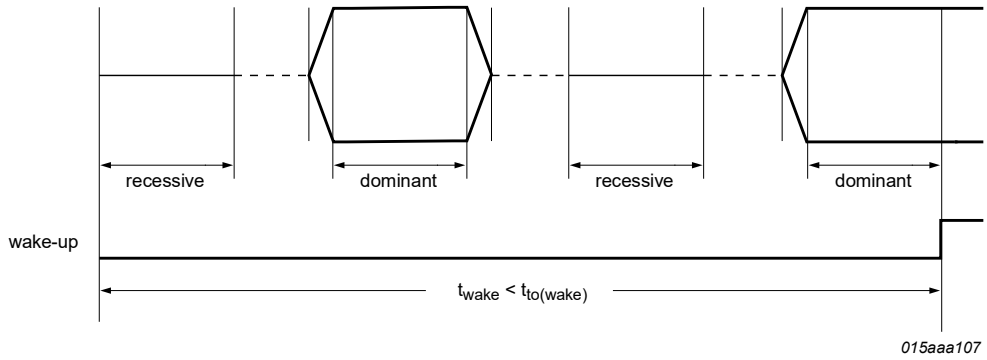


Figure 9. CAN wake-up timing diagram

6.7.2 Split circuit

Pin SPLIT provides a DC stabilized voltage of $0.5V_{V2}$. It is activated in CAN Active mode only. Pin SPLIT is floating in CAN Lowpower and Off modes. The V_{SPLIT} circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the center tap of the split termination (see Figure 10).

A transceiver in the network that is not supplied and that generates a significant leakage current from the bus lines to ground, can result in a recessive bus voltage of < $0.5V_{V2}$. In this event, the split circuit will stabilize the recessive voltage at $0.5V_{V2}$. So a start of transmission will not generate a step in the common-mode signal which would lead to poor ElectroMagnetic Emission (EME) performance.

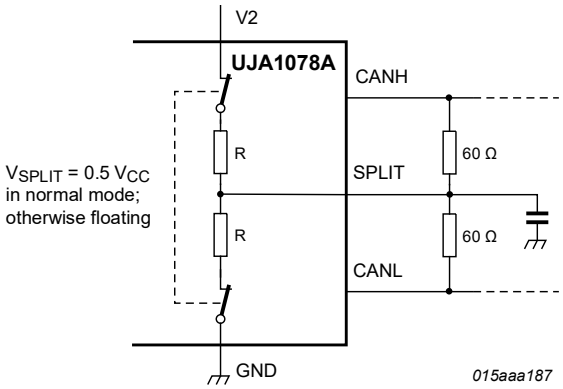


Figure 10. Stabilization circuitry and application using the SPLIT pin

6.7.3 Fail-safe features

6.7.3.1 TXDC dominant time-out function

A TXDC dominant time-out timer is started when pin TXDC is forced LOW. If the LOW state on pin TXDC persists for longer than the TXDC dominant time-out time ($t_{to(dom)TXDC}$), the transmitter will be disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXDC dominant time-out timer is reset when pin TXDC goes HIGH. The TXDC dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

6.7.3.2 Pull-up on TXDC pin

Pin TXDC has an internal pull-up towards V_{V1} to ensure a safe defined state in case the pin is left floating.

6.8 LIN1/LIN2 transceivers

The analog sections of the UJA1078A LIN transceivers are derived from those integrated into the TJA1021. Unlike the TJA1021 however, the UJA1078A does not include an internal responder termination resistor. Therefore, external termination resistors need to be connected in both commander and responder applications (see Figure 11 and Figure 12).

The transceiver is the interface between the LIN commander/responder protocol controller and the physical bus in a LIN. It is primarily intended for in-vehicle sub-networks using baud rates from 1 kBd up to 20 kBd and is LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/SAE J2602 compliant.

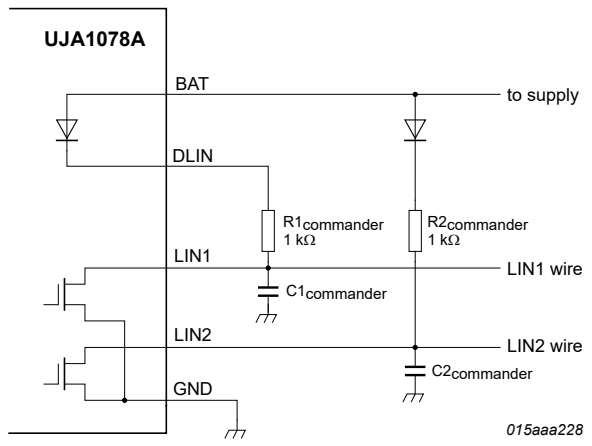


Figure 11. Typical commander application

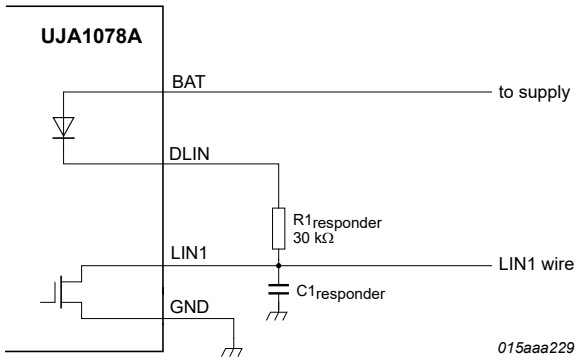


Figure 12. Typical responder application

6.8.1 LIN operating modes

6.8.1.1 Active mode

The LIN transceivers will be in Active mode when:

- the SBC is in Normal mode (MC = 10 or 11) and
- the transceivers are enabled (STBCL1 = 0 and/or STBCL2 = 0; see Table 6) and
- the battery voltage (V_{BAT}) is above the LIN undervoltage recovery threshold, $V_{uvr(LIN)}$.

In LIN Active mode, the transceivers can transmit and receive data via the LIN bus pins.

The receiver detects data streams on the LIN bus pins (LIN1 and LIN2) and transfers them to the microcontroller via pins RXDL1 and RXDL2 (see Figure 1) - LIN recessive is represented by a HIGH level on RXDL1/RXDL2, LIN dominant by a LOW level.

The transmit data streams of the protocol controller at the TXDL inputs (TXDL1 and TXDL2) are converted by the transmitter into bus signals with optimized slew rate and wave shaping to minimize EME.

6.8.1.2 Lowpower/Off modes

The LIN transceivers will be in Lowpower mode with bus wake-up detection enabled if bit STBCLx = 1 (see Table 6). The LIN transceivers can be woken up remotely via pins LIN1 and LIN2 in Lowpower mode.

When the SBC is in Standby mode or Sleep mode (MC = 00 or 01), the LIN transceivers will be in Off mode if bit STBCLx = 0. The LIN transceivers are powered down completely in Off mode to minimize quiescent current consumption.

Filters at the receiver inputs prevent unwanted wake-up events due to automotive transients or EMI. The wake-up event must remain valid for at least the minimum dominant bus time for wake-up of the LIN transceivers, $t_{wake(busdom)min}$ (see Table 11).

6.8.2 Fail-safe features

6.8.2.1 General fail-safe features

The following fail-safe features have been implemented:

- Pins TXDL1 and TXDL2 have internal pull-ups towards V_{V1} to guarantee safe, defined states if these pins are left floating
- The current of the transmitter output stage is limited in order to protect the transmitter against short circuits to pin BAT
- A loss of power (pins BAT and GND) has no impact on the bus lines or on the microcontroller. There will be no reverse currents from the bus.

6.8.2.2 TXDL dominant time-out function

A TXDL dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communications) if TXDL1 or TXDL2 is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on the TXDL pin. If the pin remains LOW for longer than the TXDL dominant time-out time ($t_{to(dom)TXDL}$), the transmitter is disabled, driving the bus lines to a recessive state. The timer is reset by a positive edge on the TXDL pin.

6.9 Local wake-up input

The SBC provides 2 local wake-up pins (WAKE1 and WAKE2). The edge sensitivity (falling, rising or both) of the wake-up pins can be configured independently via the WIC1 and WIC2 bits in the Int_Control register Table 6). These bits can also be used to disable wake-up via the wake-up pins. When wake-up is enabled, a valid wake-up event on either of these pins will cause a wake-up interrupt to be generated in Standby mode or Normal mode. If the SBC is in Sleep mode when the wake-up event occurs, it will wake up and enter Standby mode. The status of the wake-up pins can be read via the wake-up level status bits (WLS1 and WLS2) in the WD_and_Status register (Table 4).

Note that bits WLS1 and WLS2 are only active when at least one of the wake up interrupts is enabled (WIC1 ≠ 00 or WIC2 ≠ 00).

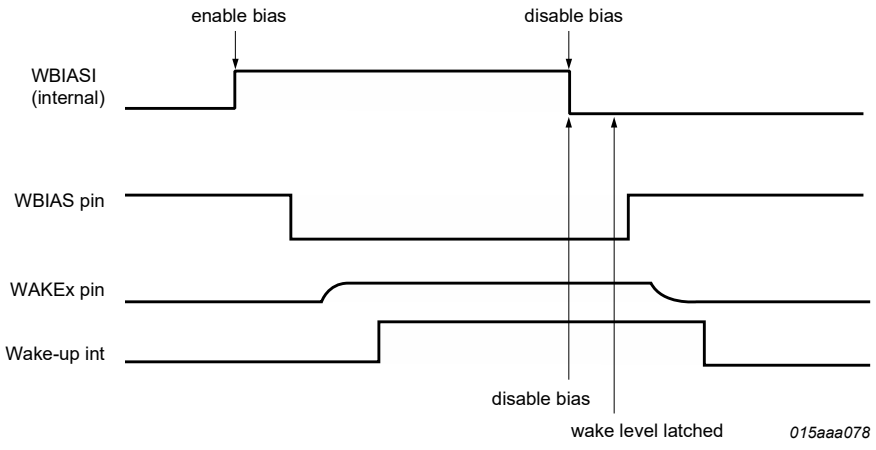


Figure 13. Wake-up pin sampling synchronized with WBIAS signal

The sampling of the wake-up pins can be synchronized with the WBIAS signal by setting bits WSE1 and WSE2 in the Int_Control register to 1 (if WSEx = 0, wake-up pins are sampled continuously). The sampling will be performed on the rising edge of WBIAS (see Figure 13). The sampling time, 16 ms or 64 ms, is selected via the Wake Bias Control bit (WBC) in the Mode_Control register.

Figure 14 shows a typical circuit for implementing cyclic sampling of the wake-up inputs.

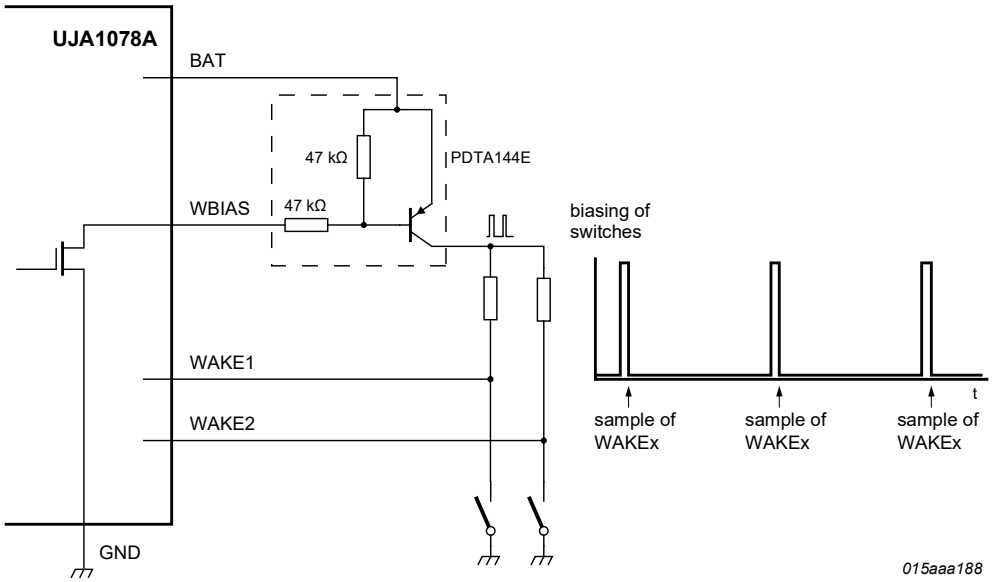


Figure 14. Typical application for cyclic sampling of wake-up signals

6.10 Interrupt output

Pin INTN is an active-LOW, open-drain interrupt output. It is driven LOW when at least one interrupt is pending. An interrupt can be cleared by writing 1 to the corresponding bit in the Int_Status register (Table 7). Clearing bits LWI1, LWI2 and CWI in Standby mode only clears the interrupt status bits and not the pending wake-up. The pending wake-up is cleared on entering Normal mode and when the corresponding standby control bit (STBCC, STBCL1 or STBCL2) is 0.

On devices that contain a watchdog, the CI is enabled when the watchdog switches to Timeout mode while the SBC is in Standby mode or Normal mode (provided pin WDOFF = LOW). A CI is generated if the watchdog overflows in Timeout mode.

The CI is provided to alert the microcontroller when the watchdog overflows in Timeout mode. The CI will wake up the microcontroller from a µC standby mode. After polling the Int_Status register, the microcontroller will be aware that the application is in cyclic wake up mode. It can then perform some checks on CAN and LIN before returning to the µC standby mode.

6.11 Temperature protection

The temperature of the SBC chip is monitored in Normal and Standby modes. If the temperature is too high, the SBC will go to Overtemp mode, where the RSTN pin is driven LOW and limp home is activated. In addition, the voltage regulators and the CAN and LIN transmitters are switched off (see also Section 6.1.6). When the temperature falls below the temperature shutdown threshold, the SBC will go to Standby mode. The temperature shutdown threshold is between 165 °C and 200 °C.

7 Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	DC value			
		pins V1, V2 and INTN	-0.3	7	V
		pins TXDC, RXDC, EN, SDI, SDO, SCK, SCSN, TXDL1, TXDL2, RXDL1, RXDL2, RSTN and WDOFF	-0.3	V_{V1} + 0.3	V
		pin VEXCC	V_{V1} - 0.3	V_{V1} + 0.35	V
		pins WAKE1, WAKE2 and WBIAS; with respect to any other pin	-58	+58	V
		pin LIMP and BAT	-0.3	+40	V
		pin VEXCTRL	-0.3	V_{BAT} + 0.3	V
		pins CANH, CANL, SPLIT, LIN1 and LIN2; with respect to any other pin	-58	+58	V
		pin DLIN; with respect to any other pin	V_{BAT} - 0.3	+58	V
$I_{R(V1-BAT)}$	reverse current from pin V1 to pin BAT	$V_{V1} \leq 5$ V [2]	-	250	mA
I_{DLIN}	current on pin DLIN		-65	0	mA
V_{trt}	transient voltage	on pins [3] BAT: via reverse polarity diode/capacitor CANL, CANH, SPLIT: coupling with two capacitors on the bus lines LIN1, LIN2: coupling via 1 nF capacitor DLIN, WAKE1, WAKE2: via 1 kΩ series resistor			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit)			
		on pins CANH, CANL, LIN1 and LIN2; pin BAT with capacitor; pins SPLIT, DLIN, WAKE1 and WAKE2 via a series resistor [4]	-6	+6	kV
		Human Body Model (HBM)			
		on any pin [5]	-2	+2	kV
		pins CANH, CANL, LIN1, LIN2, SPLIT, DLIN, WAKE1, WAKE2 [6]	-8	+8	kV
		pin BAT; referenced to ground [7]	-4	+4	kV
		pin TEST2; referenced to pin BAT [7]	-1.25	+2	kV
		pin TEST2; referenced to other reference pins [7]	-2	+2	kV

Table 8. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [8]			
		on any pin	-300	+300	V
		CDM [9]			
		corner pins	-750	+750	V
		any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[10]	-40	+150	°C
T_{stg}	storage temperature	[11]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] A reverse diode connected between V1 (anode) and BAT (cathode) limits the voltage drop voltage from V1(+) to BAT (-).
[3] Verified by an external test house to ensure pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.
[4] ESD performance according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house for pins BAT, CANH, CANL, LIN1, LIN2, WAKE1 and WAKE2. The result is equal to or better than ±6 kV.
[5] According to AEC-Q100-002.
[6] V1, V2 and BAT connected to GND, emulating application circuit. HBM pulse as specified in AECQ100-002 used.
[7] HBM pulse as specified in AEC-Q100-002 used.
[8] Machine Model (MM): according to AEC-Q100-003.
[9] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).
[10] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[11] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HTSSOP32 package	33	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]		9	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		8	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).
[2] Case temperature refers to the centre of the heatsink at the bottom of the package.

9 Static characteristics

Table 10. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; $V_{BAT} > V_{V1}$; $V_{BAT} > V_{V2}$; $R_{LIN1} = R_{LIN2}$ = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
V_{BAT}	battery supply voltage		4.5	-	28	V
I_{BAT}	battery supply current	MC = 00 (Standby; V1 on, V2 off)				

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		STBCC = STBCL1 = STBCL2 = 1 (CAN/LIN wake-up enabled) WIC1 = WIC2 = 11 (WAKE interrupts enabled) 7.5 V < V_{BAT} < 28 V; I_{V1} = 0 mA V_{RSTN} = V_{SCSN} = V_{V1} V_{TXDL1} = V_{TXDL2} = V_{TXDC} = V_{V1} V_{SDI} = V_{SCK} = 0 V				
		T_{vj} = -40 °C	-	84	99	µA
		T_{vj} = 25 °C	-	77	89	µA
		T_{vj} = 150 °C	-	69	81	µA
		MC = 01 (Sleep; V1 off, V2 off) STBCC = STBCL1 = STBCL2 = 1 (CAN/LIN wake-up enabled) WIC1 = WIC2 = 11 (WAKE interrupts enabled) 7.5 V < V_{BAT} < 28 V; V_{V1} = 0 V				
		T_{vj} = -40 °C	-	62	72	µA
		T_{vj} = 25 °C	-	57	66	µA
		T_{vj} = 150 °C	-	53	59	µA
		contributed by LIN wake-up receiver STBCL1/STBCL2 = 1 V_{LIN1} = V_{LIN2} = V_{BAT} 5.5 V < V_{BAT} < 28 V	-	1.1	2	µA
		contributed by CAN wake-up receiver STBCC = 1; V_{CANH} = V_{CANL} = 2.5 V 5.5 V < V_{BAT} < 28 V	1	6	13	µA
		contributed by WAKEx pin edge detectors; WIC1 = WIC2 = 11; V_{WAKE1} = V_{WAKE2} = V_{BAT}	0	5	10	µA
$I_{BAT(add)}$	additional battery supply current	5.1 V < V_{BAT} < 7.5 V	-	-	50	µA
		4.5 V < V_{BAT} < 5.1 V V1 on (5 V version)	-	-	3	mA
		V2 on; MC = 11 V2UIE = 1; I_{V2} = 0 mA	100	-	950	µA
		CAN Active mode (recessive) STBCC = 0; MC = 1x; V_{TXDC} = V_{V1} I_{CANH} = I_{CANL} = 0 mA 5.5 V < V_{BAT} < 28 V	-	-	10	mA
		CAN active (dominant)	-	-	70	mA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		STBCC = 0; MC = 1x; V_{TXDC} = 0 V $R_{(CANH-CANL)}$ = 45 Ω 5.5 V < V_{BAT} < 28 V				
		LINx Active mode (recessive) STBCLx = 0; MC = 1x V_{TXDL1} = V_{TXDL2} = V_{V1} I_{DLIN} = I_{LIN1} = I_{LIN2} = 0 mA 5.5 V < V_{BAT} < 28 V	-	-	1300	µA
		LINx Active mode (dominant); STBCLx = 0; MC = 1x V_{TXDL1} = V_{TXDL2} = 0 V I_{DLIN} = I_{LIN1} = I_{LIN2} = 0 mA; V_{BAT} = 14 V	-	-	5	mA
		LINx Active mode (dominant); STBCLx = 0; MC = 1x V_{TXDL1}= V_{TXDL2} = 0 V I_{DLIN} = I_{LIN1} = I_{LIN2} = 0 mA; V_{BAT} = 28 V	-	-	10	mA
$V_{th(det)pon}$	power-on detection threshold voltage		4.5	-	5.5	V
$V_{th(det)poff}$	power-off detection threshold voltage		4.25	-	4.5	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		200	-	-	mV
$V_{uvd(LIN)}$	LIN undervoltage detection voltage		5	-	5.3	V
$V_{uvr(LIN)}$	LIN undervoltage recovery voltage		5	-	5.5	V
$V_{hys(uvd)LIN}$	LIN undervoltage detection hysteresis voltage		25	-	300	mV
$V_{uvd(ctrl)lext}$	external current control undervoltage detection voltage		5.9	-	7.5	V
Voltage source; pin V1						
V_O	output voltage	$V_{O(V1)nom}$ = 5 V; V_{BAT} = 5.5 V to 28 V I_{V1} = -200 mA to -5 mA	4.9	5	5.1	V
		$V_{O(V1)nom}$ = 5 V; V_{BAT} = 5.5 V to 28 V I_{V1} = -250 mA to -200 mA	4.75	5	5.1	V
		$V_{O(V1)nom}$ = 5 V; V_{BAT} = 5.5 V to 5.75 V I_{V1} = -250 mA to -5 mA 150 °C < T_{vj} < 200 °C	4.5	5	5.1	V
		$V_{O(V1)nom}$ = 5 V; V_{BAT} = 5.75 V to 28 V I_{V1} = -250 mA to -5 mA 150 °C < T_{vj} < 200 °C	4.85	5	5.1	V

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{O(V1)nom}$ = 3.3 V; V_{BAT} = 4.5 V to 28 V I_{V1} = -250 mA to -5 mA	3.234	3.3	3.366	V
		$V_{O(V1)nom}$ = 3.3 V; V_{BAT} = 4.5 V to 28 V I_{V1} = -250 mA to -5 mA 150 °C < T_{vj} < 200 °C	2.97	3.3	3.366	V
$R_{(BAT-V1)}$	resistance between pin BAT and pin V1	$V_{O(V1)nom}$ = 5 V; V_{BAT} = 4.5 V to 5.5 V I_{V1} = -250 mA to -5 mA regulator in saturation	-	-	3	Ω
V_{uvd}	undervoltage detection voltage	90 %; $V_{O(V1)nom}$ = 5 V; RTHC = 0	4.5	-	4.75	V
		90 %; $V_{O(V1)nom}$ = 3.3 V; RTHC = 0	2.97	-	3.135	V
		70 %; $V_{O(V1)nom}$ = 5 V; RTHC = 1	3.5	-	3.75	V
V_{uvr}	undervoltage recovery voltage	90 %; $V_{O(V1)nom}$ = 5 V	4.56	-	4.9	V
		90 %; $V_{O(V1)nom}$ = 3.3 V	3.025	-	3.234	V
$I_{O(sc)}$	short-circuit output current	I_{VEXCC} = 0 mA	-600	-	-250	mA
Load regulation						
ΔV_{V1}	voltage variation on pin V1	as a function of load current variation V_{BAT} = 5.75 V to 28 V I_{V1} = -250 mA to -5 mA	-	-	25	mV
Line regulation						
ΔV_{V1}	voltage variation on pin V1	as a function of supply voltage variation V_{BAT} = 5.5 V to 28 V I_{V1} = -30 mA	-	-	25	mV
PNP base; pin VEXCTRL						
$I_{O(sc)}$	short-circuit output current	$V_{VEXCTRL}$ ≥ 4.5 V; V_{BAT} = 6 V to 28 V	3.5	5.8	8	mA
$I_{th(act)PNP}$	PNP activation threshold current	load current increasing; external PNP transistor connected - see Section 6.6.2				
		PDC 0	74	130	191	mA
		PDC 0; T_{vj} = 150 °C	74	85	99	mA
		PDC 1	44	76	114	mA
		PDC 1; T_{vj} = 150 °C	44	50	59	mA
$I_{th(deact)PNP}$	PNP deactivation threshold current	load current falling; external PNP transistor connected - see Section 6.6.2				
		PDC 0	40	76	120	mA
		PDC 0; T_{vj} = 150 °C	44	50	59	mA
		PDC 1	11	22	36	mA
		PDC 1; T_{vj} = 150 °C	12	15	18	mA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PNP collector; pin VEXCC						
$V_{th(act)Ilim}$	current limiting activation threshold voltage	measured across resistor connected between pins VEXCC and V1 (see Section 6.6.2) 2.97 V ≤ V_{V1} ≤ 5.5 V 6 V < V_{BAT} < 28 V	240	-	330	mV
Voltage source; pin V2						
V_O	output voltage	V_{BAT} = 5.5 V to 28 V I_{V2} = -100 mA to 0 mA	4.75	5	5.25	V
		V_{BAT} = 6 V to 28 V I_{V2} = -120 mA to 0 mA	4.75	5	5.25	V
ΔV_{V2}	voltage variation on pin V2	as a function of supply voltage variation V_{BAT} = 5.5 V to 28 V I_{V2} = -10 mA	-	-	60	mV
		as a function of load current variation; 6 V < V_{BAT} < 28 V I_{V2} = -100 mA to -5 mA	-	-	80	mV
V_{uvd}	undervoltage detection voltage		4.5	-	4.70	V
V_{uvr}	undervoltage recovery voltage		4.55	-	4.75	V
V_{uvhys}	undervoltage hysteresis voltage		20	-	80	mV
$I_{O(sc)}$	short-circuit output current	V_{V2} = 0 V to 5.5 V	-250	-	-100	mA
Serial peripheral interface inputs; pins SDI, SCK and SCSN						
$V_{th(sw)}$	switching threshold voltage	V_{V1} = 2.97 V to 5.5 V	$0.3V_{V1}$	-	$0.7V_{V1}$	V
$V_{hys(i)}$	input hysteresis voltage	V_{V1} = 2.97 V to 5.5 V	100	-	900	mV
$R_{pd(SCK)}$	pull-down resistance on pin SCK		50	130	400	kΩ
$R_{pu(SCSN)}$	pull-up resistance on pin SCSN		50	130	400	kΩ
$I_{LI(SDI)}$	input leakage current on pin SDI		-5	-	+5	µA
Serial peripheral interface data output; pin SDO						
I_{OH}	HIGH-level output current	V_{SCSN} = 0 V; V_O = V_{V1} - 0.4 V V_{V1} = 2.97 V to 5.5 V	-30	-	-1.6	mA
I_{OL}	LOW-level output current	V_{SCSN} = 0 V; V_O = 0.4 V V_{V1} = 2.97 V to 5.5 V	1.6	-	30	mA
I_{LO}	output leakage current	V_{SCSN} = V_{V1}; V_O = 0 V to V_{V1} V_{V1} = 2.97 V to 5.5 V	-5	-	5	µA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset output with clamping detection; pin RSTN						
I_{OH}	HIGH-level output current	V_{RSTN} = 0.8V_{V1} V_{V1} = 2.97 V to 5.5 V	-1500	-	-100	µA
I_{OL}	LOW-level output current	strong; V_{RSTN} = 0.2V_{V1} V_{V1} = 2.97 V to 5.5 V -40 °C < T_{vj} < 200 °C	4.9	-	40	mA
		weak; V_{RSTN} = 0.8V_{V1} V_{V1} = 2.97 V to 5.5 V -40 °C < T_{vj} < 200 °C	200	-	540	µA
V_{OL}	LOW-level output voltage	V_{V1} = 1 V to 5.5 V pull-up resistor to V_{V1} ≥ 900 Ω -40 °C < T_{vj} < 200 °C; V_{BAT} < 28 V	0	-	0.2V_{V1}	V
		V_{V1} = 2.975 V to 5.5 V pull-up resistor to V1 ≥ 900 Ω; -40 °C < T_{vj} < 200 °C	0	-	0.5	V
V_{OH}	HIGH-level output voltage	-40 °C < T_{vj} < 200 °C	0.8V_{V1}	-	V_{V1} + 0.3	V
$V_{th(sw)}$	switching threshold voltage	V_{V1} = 2.97 V to 5.5 V	0.3V_{V1}	-	0.7V_{V1}	V
$V_{hys(i)}$	input hysteresis voltage	V_{V1} = 2.97 V to 5.5 V	100	-	900	mV
Interrupt output; pin INTN						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	-	15	mA
Enable output; pin EN						
I_{OH}	HIGH-level output current	V_{OH} = V_{V1} - 0. 4 V V_{V1} = 2.97 V to 5.5 V	-20	-	-1.6	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{V1} = 2.97 V to 5.5 V	1.6	-	20	mA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA; V_{V1} = 1.5 V	-	-	0.4	V
Watchdog off input; pin WDOFF						
$V_{th(sw)}$	switching threshold voltage	V_{V1} = 2.97 V to 5.5 V	0.3V_{V1}	-	0.7V_{V1}	V
$V_{hys(i)}$	input hysteresis voltage	V_{V1} = 2.97 V to 5.5 V	100	-	900	mV
R_{pupd}	pull-up/pull-down resistance	V_{V1} = 2.97 V to 5.5 V	5	10	20	kΩ
Wake input; pin WAKE1, WAKE2						
$V_{th(sw)}$	switching threshold voltage		2	-	3.75	V
$V_{hys(i)}$	input hysteresis voltage		100	-	1000	mV
I_{pu}	pull-up current	V_{WAKE} = 0 V for t < t_{wake}	-2	-	0	µA
I_{pd}	pull-down current	V_{WAKE} = V_{BAT} for t < t_{wake}	0	-	2	µA
Limp home output; pin LIMP						
I_O	output current	V_{LIMP} = 0.4 V; LHC = 1	0.8	-	8	mA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		T_{vj} = -40 °C to 200 °C				
Wake bias output; pin WBIAS						
I_O	output current	V_{WBIAS} = 1.4 V	1	-	7	mA
CAN transmit data input; pin TXDC						
$V_{th(sw)}$	switching threshold voltage	V_{V1} = 2.97 V to 5.5 V	$0.3V_{V1}$	-	$0.7V_{V1}$	V
$V_{hys(i)}$	input hysteresis voltage	V_{V1} = 2.97 V to 5.5 V	100	-	900	mV
R_{pu}	pull-up resistance		4	12	25	kΩ
CAN receive data output; pin RXDC						
I_{OH}	HIGH-level output current	CAN Active mode V_{RXDC} = V_{V1} - 0.4 V	-20	-	-1.5	mA
I_{OL}	LOW-level output current	V_{RXDC} = 0.4 V	1.6	-	20	mA
R_{pu}	pull-up resistance	MC = 00; Standby mode	4	12	25	kΩ
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode V_{V2} = 4.5 V to 5.5 V; V_{TXDC} = 0 V $R_{(CANH-CANL)}$ = 60 Ω				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{V2} - V_{CANH} - V_{CANL} $R_{(CANH-CANL)}$ = 60 Ω	-400	-	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	CAN Active mode (dominant) V_{V2} = 4.75 V to 5.25 V; V_{TXDC} = 0 V $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω	1.5	-	3.0	V
		CAN Active mode (recessive) V_{V2} = 4.5 V to 5.5 V; V_{TXDC} = V_{V1} $R_{(CANH-CANL)}$ = no load	-50	0	+50	mV
$V_{O(rec)}$	recessive output voltage	CAN Active mode; V_{V2} = 4.5 V to 5.5 V V_{TXDC} = V_{V1} $R_{(CANH-CANL)}$ = no load	2	$0.5V_{V2}$	3	V
		CAN Lowpower/Off mode $R_{(CANH-CANL)}$ = no load	-0.1	-	+0.1	V
$I_{O(dom)}$	dominant output current	CAN Active mode V_{TXDC} = 0 V; V_{V2} = 5 V				
		pin CANH; V_{CANH} = 0 V	-100	-70	-40	mA
		pin CANL; V_{CANL} = 40 V	40	70	100	mA
$I_{O(rec)}$	recessive output current	V_{CANL} = V_{CANH} = -27 V to +32 V V_{TXDC} = V_{V1}; V_{V2} = 4.5 V to 5.5 V	-3	-	+3	mA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(RX)dif}$	differential receiver threshold voltage	CAN Active mode V_{V2} = 4.5 V to 5.5 V -30 V < V_{CANH} < +30 V -30 V < V_{CANL} < +30 V	0.5	0.7	0.9	V
		CAN Lowpower mode -12 V < V_{CANH} < +12 V -12 V < V_{CANL} < +12 V	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active mode V_{V2} = 4.5 V to 5.5 V -30 V < V_{CANH} < +30 V -30 V < V_{CANL} < +30 V	40	120	400	mV
$R_{i(cm)}$	common-mode input resistance	CAN Active mode; V_{V2} = 5 V V_{CANH} = V_{CANL} = 5 V	9	15	28	kΩ
ΔR_i	input resistance deviation	CAN Active mode; V_{V2} = 5 V V_{CANH} = V_{CANL} = 5 V	-1	-	+1	%
$R_{i(dif)}$	differential input resistance	CAN Active mode; V_{V2} = 5.5 V V_{CANH} = V_{CANL} = -35 V to +35 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	CAN Active mode; not tested	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	CAN Active mode; not tested	-	-	10	pF
I_{LI}	input leakage current	V_{BAT} = 0 V; V_{V2} = 0 V V_{CANH} = V_{CANL} = 5 V	-5	-	+5	µA
CAN bus common mode stabilization output; pin SPLIT						
V_O	output voltage	CAN Active mode V_{V2} = 4.5 V to 5.5 V I_{SPLIT} = -500 µA to 500 µA	$0.3V_{V2}$	$0.5V_{V2}$	$0.7V_{V2}$	V
		CAN Active mode V_{V2} = 4.5 V to 5.5 V; R_L ≥ 1 MΩ	0.45 × V_{V2}	0.5 × V_{V2}	0.55 × V_{V2}	V
I_L	leakage current	CAN Lowpower/Off mode or Active mode with V_{V2} < 4.5 V V_{SPLIT} = -30 V to + 30 V	-5	-	+5	µA
LIN transmit data input; pin TXDL1, TXDL2						
$V_{th(sw)}$	switching threshold voltage	V_{V1} = 2.97 V to 5.5 V	$0.3V_{V1}$	-	$0.7V_{V1}$	V
$V_{hys(i)}$	input hysteresis voltage	V_{V1} = 2.97 V to 5.5 V	100	-	900	mV
R_{pu}	pull-up resistance		4	12	25	kΩ
LIN receive data output; pin RXDL1, RXDL2						
I_{OH}	HIGH-level output current	LIN Active mode V_{RXDL1} = V_{RXDL2} = V_{V1} - 0.4 V	-20	-	-1.5	mA
I_{OL}	LOW-level output current	V_{RXDL1} = V_{RXDL2} = 0.4 V	1.6	-	20	mA

Table 10. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; positive currents flow in the IC; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	pull-up resistance	MC = 00; Standby mode	4	12	25	kΩ
LIN bus line; pin LIN1, LIN2						
I_{BUS_LIM}	current limitation for driver dominant state	LIN Active mode V_{BAT} = V_{LIN1} = V_{LIN2} = 18 V V_{TXDL1} = V_{TXDL2} = 0 V	40	-	100	mA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	V_{LIN1} = V_{LIN2} = 28 V [2] V_{BAT} = 5.5 V; V_{TXDL1} = V_{TXDL2} = V_{V1}	-	-	2	µA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	V_{TXDL1} = V_{TXDL2} = V_{V1} V_{LIN1} = V_{LIN2} = 0 V; V_{BAT} = 14 V	-10	-	+10	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = V_{GND} = 28 V; V_{LIN1} = V_{LIN2} = 0 V	-100	-	10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; V_{LIN1} = V_{LIN2} = 28 V [2]	-	-	2	µA
V_{BUSrec}	receiver recessive state	V_{BAT} = 5.5 V to 18 V	0.6 × V_{BAT}	-	-	V
V_{BUSdom}	receiver dominant state	V_{BAT} = 5.5 V to 18 V	-	-	0.4V_{BAT}	V
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec}) / 2 V_{BAT} = 5.5 V to 18 V; LIN Active mode	0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = V_{BUSrec} - V_{BUSdom} V_{BAT} = 5.5 V to 18 V; LIN Active mode	0.05 × V_{BAT}	0.15 × V_{BAT}	0.175 × V_{BAT}	V
C_{LIN1}	capacitance on pin LIN1	with respect to GND	-	-	30	pF
C_{LIN2}	capacitance on pin LIN2	with respect to GND	-	-	30	pF
$V_{O(dom)}$	dominant output voltage	V_{TXDL1} = V_{TXDL2} = 0 V; V_{BAT} = 7 V LIN Active mode	-	-	1.4	V
		V_{TXDL1} = V_{TXDL2} = 0 V; V_{BAT} = 18 V LIN Active mode	-	-	2.0	V
LIN bus termination; pin DLIN						
$\Delta V_{(DLIN-BAT)}$	voltage difference between pin DLIN and pin BAT	5 mA < I_{DLIN} < 20 mA	0.4	0.65	1	V
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		165	180	200	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		126	138	150	°C

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Not tested in production; guartanteed by design.

10 Dynamic characteristics

Table 11. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage source; pin V1						
$t_{d(uvd)}$	undervoltage detection delay time	V_{V1} falling; dV_{V1}/dt = 0.1 V/µs	7	-	23	µs
$t_{det(CL)L}$	LOW-level clamping detection time	V_{V1} < 0.9$V_{O(V1)nom}$; V1 active V_{WDOFF} = 0 V (watchdog variants only)	95	-	140	ms
Voltage source; pin V2						
$t_{d(uvd)}$	undervoltage detection delay time	V_{V2} falling, dV_{V2}/dt = 0.1 V/µs	7	-	23	µs
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 17						
$t_{cy(clk)}$	clock cycle time	V_{V1} = 2.97 V to 5.5 V	320	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	V_{V1} = 2.97 V to 5.5 V; clock is LOW when SPI select falls	110	-	-	ns
t_{SPILAG}	SPI enable lag time	V_{V1} = 2.97 V to 5.5 V; clock is LOW when SPI select rises	140	-	-	ns
$t_{clk(H)}$	clock HIGH time	V_{V1} = 2.97 V to 5.5 V	160	-	-	ns
$t_{clk(L)}$	clock LOW time	V_{V1} = 2.97 V to 5.5 V	160	-	-	ns
$t_{su(D)}$	data input set-up time	V_{V1} = 2.97 V to 5.5 V	0	-	-	ns
$t_{h(D)}$	data input hold time	V_{V1} = 2.97 V to 5.5 V	80	-	-	ns
$t_{v(Q)}$	data output valid time	pin SDO; V_{V1} = 2.97 V to 5.5 V C_L = 100 pF	-	-	110	ns
$t_{WH(S)}$	chip select pulse width HIGH	V_{V1} = 2.97 V to 5.5 V	20	-	-	ns
Reset output; pin RSTN						
$t_{w(rst)}$	reset pulse width	long; $R_{pu(RSTN)}$ > 25 kΩ	20	-	25	ms
		short; $R_{pu(RSTN)}$ = 900 Ω to 1100 Ω	3.6	-	5	ms
$t_{det(CL)L}$	LOW-level clamping detection time	RSTN driven HIGH internally but pin RSTN remains LOW; V_{WDOFF} = 0 V (watchdog variants only)	95	-	140	ms
t_{fltr}	filter time		7	-	18	µs
Watchdog off input; pin WDOFF						
t_{fltr}	filter time		0.9	-	2.3	ms
Wake input; pin WAKE1, WAKE2						
t_{wake}	wake-up time		10	-	40	µs
$t_{d(po)}$	power-on delay time		113	-	278	µs

Table 11. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN transceiver timing; pins CANH, CANL, TXDC and RXDC; see Figure 15 and Figure 18						
$t_{d(TXDCH-RXDCH)}$	delay time from TXDC HIGH to RXDC HIGH	50 % V_{TXDC} to 50 % V_{RXDC} V_{V2} = 4.5 V to 5.5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF; C_{RXDC} = 15 pF f_{TXDC} = 250 kHz	60	-	235	ns
$t_{d(TXDCL-RXDCL)}$	delay time from TXDC LOW to RXDC LOW	50 % V_{TXDC} to 50 % V_{RXDC} V_{V2} = 4.5 V to 5.5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF; C_{RXDC} = 15 pF f_{TXDC} = 250 kHz	60	-	235	ns
$t_{d(TXDC-busdom)}$	delay time from TXDC to bus dominant	V_{V2} = 4.5 V to 5. 5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF	-	70	-	ns
$t_{d(TXDC-busrec)}$	delay time from TXDC to bus recessive	V_{V2} = 4.5 V to 5.5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF	-	90	-	ns
$t_{d(busdom-RXDC)}$	delay time from bus dominant to RXDC	V_{V2} = 4.5 V to 5.5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF C_{RXDC} = 15 pF	-	75	-	ns
$t_{d(busrec-RXDC)}$	delay time from bus recessive to RXDC	V_{V2} = 4.5 V to 5.5 V $R_{(CANH-CANL)}$ = 60 Ω $C_{(CANH-CANL)}$ = 100 pF C_{RXDC} = 15 pF	-	95	-	ns
Bus wake-up timing; pins CANH and CANL; see Figure 9						
$t_{wake(busdom)min}$	minimum bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL Sleep mode	0.5	-	3	µs
		second pulse for wake-up on pins CANH and CANL	0.5	-	3	µs
$t_{wake(busrec)min}$	minimum bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; Sleep mode	0.5	-	3	µs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	3	µs
$t_{to(wake)}$	wake-up time-out time	between wake-up and confirm messages; Sleep mode	0.4	-	1.2	ms
$t_{to(dom)TXDC}$	TXDC dominant time-out time	CAN online; V_{V2} = 4.5 V to 5.5 V V_{TXDC} = 0 V	1.8	-	4.5	ms

Table 11. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN transceivers; pins LIN1, LIN2, TXDL1, TXDL2, RXDL1, RXDL2; see Figure 16 and Figure 19						
δ1	duty cycle 1	$V_{th(rec)RX(max)}$ = 0.744V_{BAT} [2] $V_{th(dom)RX(max)}$ = 0.581V_{BAT}; t_{bit} = 50 µs [3] V_{BAT} = 7 V to 18 V; LSC = 0	0.396	-	-	
		$V_{th(rec)RX(max)}$ = 0.76V_{BAT} [2] $V_{th(dom)RX(max)}$ = 0.593V_{BAT}; t_{bit} = 50 µs [3] V_{BAT} = 5.5 V to 7 V; LSC = 0	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)RX(min)}$ = 0.422V_{BAT} [3] $V_{th(dom)RX(min)}$ = 0.284V_{BAT}; t_{bit} = 50 µs [4] V_{BAT} = 7.6 V to 18 V; LSC = 0	-	-	0.581	
		$V_{th(rec)RX(min)}$ = 0.41V_{BAT} [3] $V_{th(dom)RX(min)}$ = 0.275V_{BAT}; t_{bit} = 50 µs [4] V_{BAT} = 6.1 V to 7.6 V; LSC = 0	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)RX(max)}$ = 0.778V_{BAT} [2] $V_{th(dom)RX(max)}$ = 0.616V_{BAT} [3] t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V; LSC = 1	0.417	-	-	
		$V_{th(rec)RX(max)}$ = 0.797V_{BAT} [2] $V_{th(dom)RX(max)}$ = 0.630V_{BAT} [3] t_{bit} = 96 µs; V_{BAT} = 5.5 V to 7 V; LSC = 1	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)RX(min)}$ = 0.389V_{BAT} [3] $V_{th(dom)RX(min)}$ = 0.251V_{BAT}; t_{bit} = 96 µs [4] V_{BAT} = 7.6 V to 18 V; LSC = 1	-	-	0.590	
		$V_{th(rec)RX(min)}$ = 0.378V_{BAT} [3] $V_{th(dom)RX(min)}$ = 0.242V_{BAT}; t_{bit} = 96 µs [4] V_{BAT} = 6.1 V to 7.6V; LSC = 1	-	-	0.590	
$t_{PD(RX)r}$	rising receiver propagation delay	V_{BAT} = 5.5 V to 18 V R_{RXDL1} = R_{RXDL2} = 2.4 kΩ C_{RXDL1} = C_{RXDL2} = 20 pF	-	-	6	µs
$t_{PD(RX)f}$	falling receiver propagation delay	V_{BAT} = 5.5 V to 18 V R_{RXDL1} = R_{RXDL2} = 2.4 kΩ C_{RXDL1} = C_{RXDL2} = 20 pF	-	-	6	µs
$t_{PD(RX)sym}$	receiver propagation delay symmetry	V_{BAT} = 5.5 V to 18 V [5] R_{RXDL1} = R_{RXDL2} = 2.4 kΩ C_{RXDL1} = C_{RXDL2} = 20 pF	-2	-	+2	µs
$t_{wake(busdom)min}$	minimum bus dominant wake-up time		28	-	104	µs
$t_{to(dom)TXDL}$	TXDL dominant time-out time	LIN online mode; V_{TXDL} = 0 V	20	-	80	ms
Wake bias output; pin WBIAS						
t_{WBIASL}	WBIAS LOW time		227	-	278	µs
t_{cy}	cycle time	WBC = 1	58.1	-	71.2	ms

Table 11. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{BAT} > V_{V1}; V_{BAT} > V_{V2}; R_{LIN1} = R_{LIN2} = 500 Ω; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω; all voltages are defined with respect to ground; typical values are given at V_{BAT} = 14 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		WBC = 0	14.5	-	17.8	ms
Watchdog						
$t_{trig(wd)1}$	watchdog trigger time 1	Normal mode watchdog Window mode only [6]	0.45 × NWP[7]	-	0.555 × NWP[7]	ms
$t_{trig(wd)2}$	watchdog trigger time 2	Normal, Standby and Sleep modes watchdog Window mode only [8]	0.9 × NWP[7]	-	1.11 × NWP[7]	ms
Oscillator						
f_{osc}	oscillator frequency		460.8	512	563.2	kHz

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 16.

[3] Bus load conditions are: C_L = 1 nF and R_L = 1 kΩ; C_L = 6.8 nF and R_L = 660 Ω; C_L = 10 nF and R_L = 500 Ω.

[4] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 16.

[5] $t_{PD(RX)sym} = t_{PD(RX)r} - t_{PD(RX)f}$.

[6] A system reset will be performed if the watchdog is in Window mode and is triggered less than $t_{trig(wd)1}$ after the start of the watchdog period (or in the first half of the watchdog period).

[7] The nominal watchdog period is programmed via the NWP control bits in the WD_and_Status register (see Table 4); valid in watchdog Window mode only.

[8] The watchdog will be reset if it is in window mode and is triggered at least $t_{trig(wd)1}$, but not more than $t_{trig(wd)2}$, after the start of the watchdog period (or in the second half of the watchdog period). A system reset will be performed if the watchdog is triggered more than $t_{trig(wd)2}$ after the start of the watchdog period (watchdog overflows).

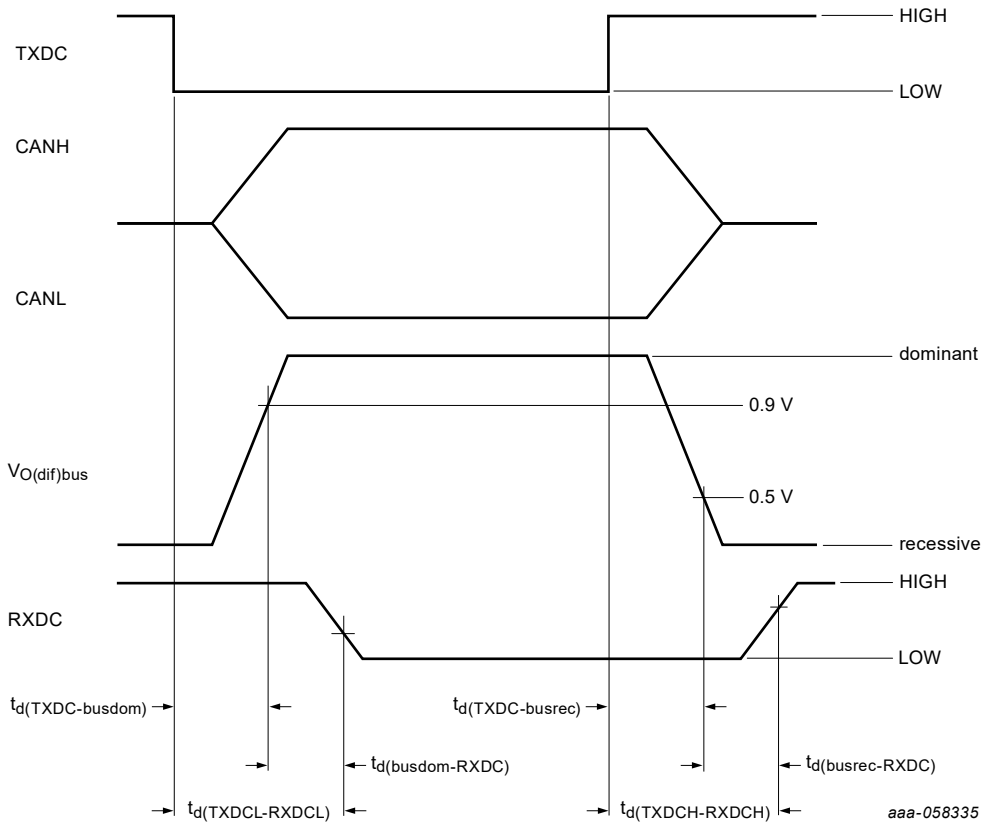


Figure 15. CAN transceiver timing diagram

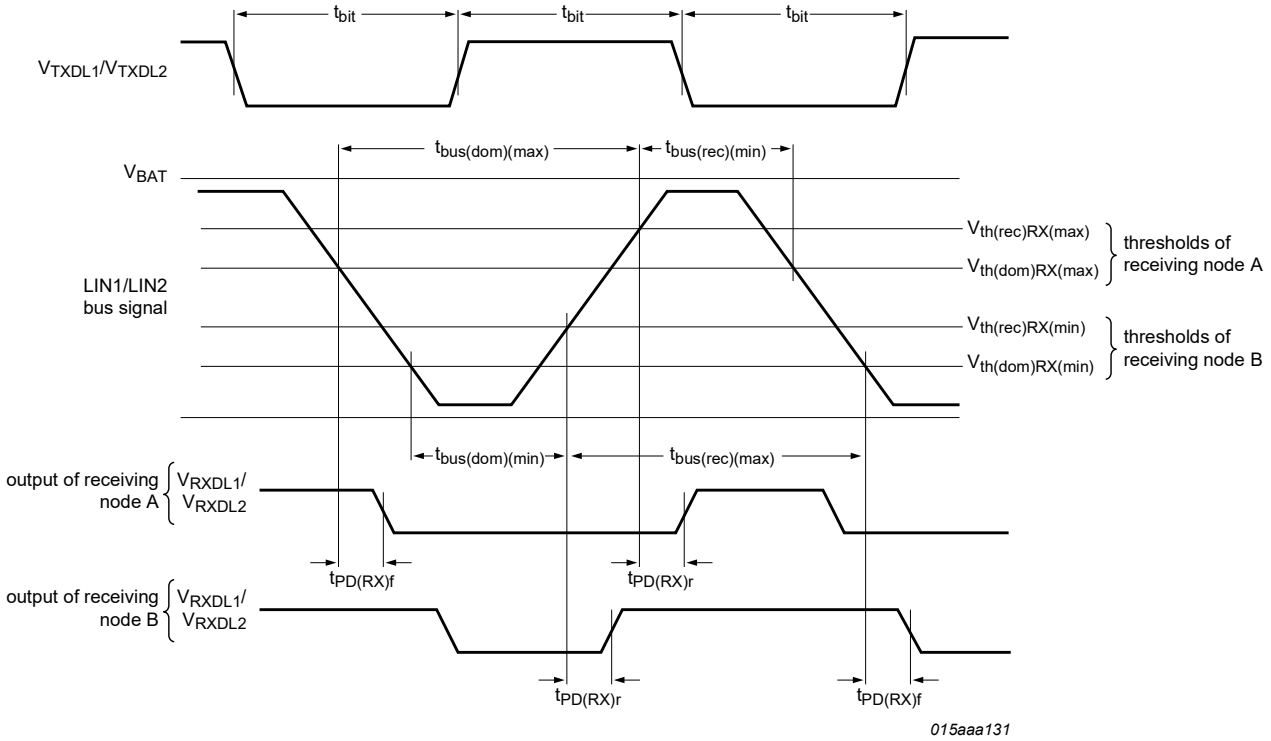


Figure 16. Timing diagram LIN transceivers

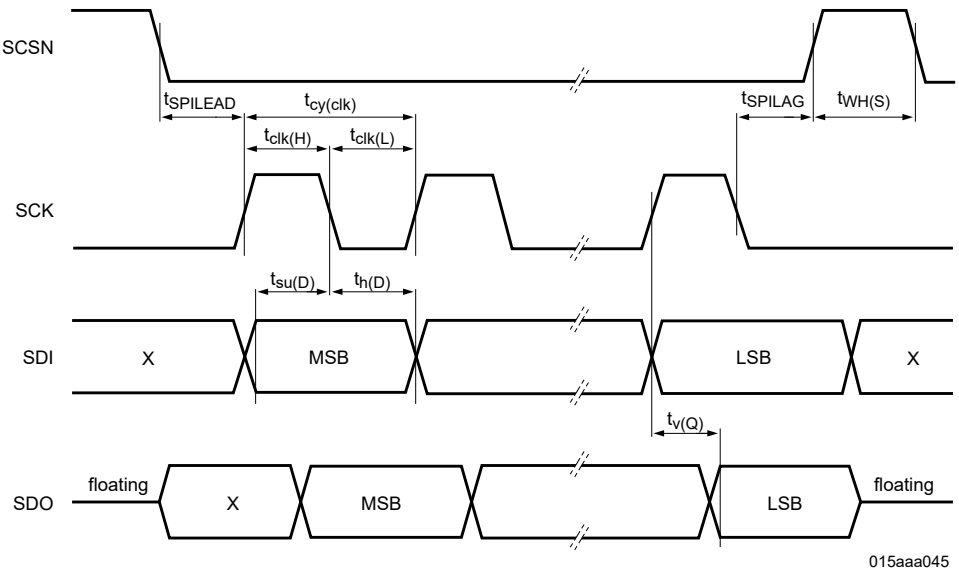


Figure 17. SPI timing diagram

11 Application information

Further information on the application of the UJA107xA can be found in the *NXP AH1002 Application Hints - Core System Basis Chip UJA107xA*.

12 Test information

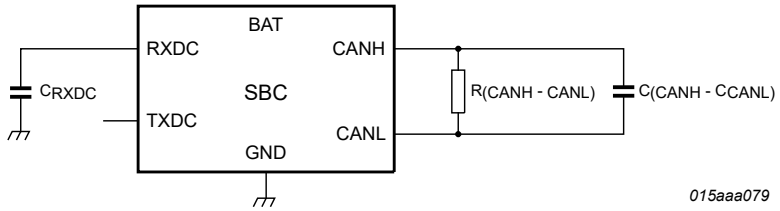


Figure 18. Timing test circuit for CAN transceiver

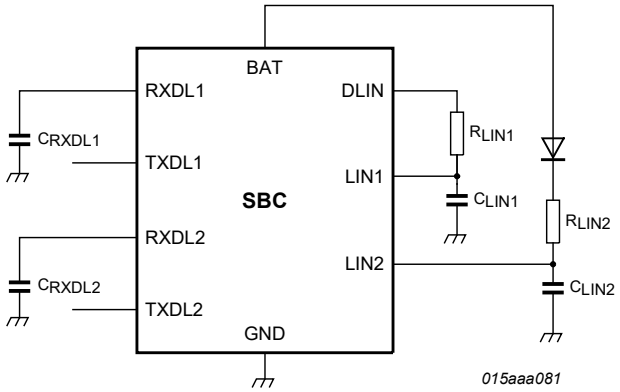


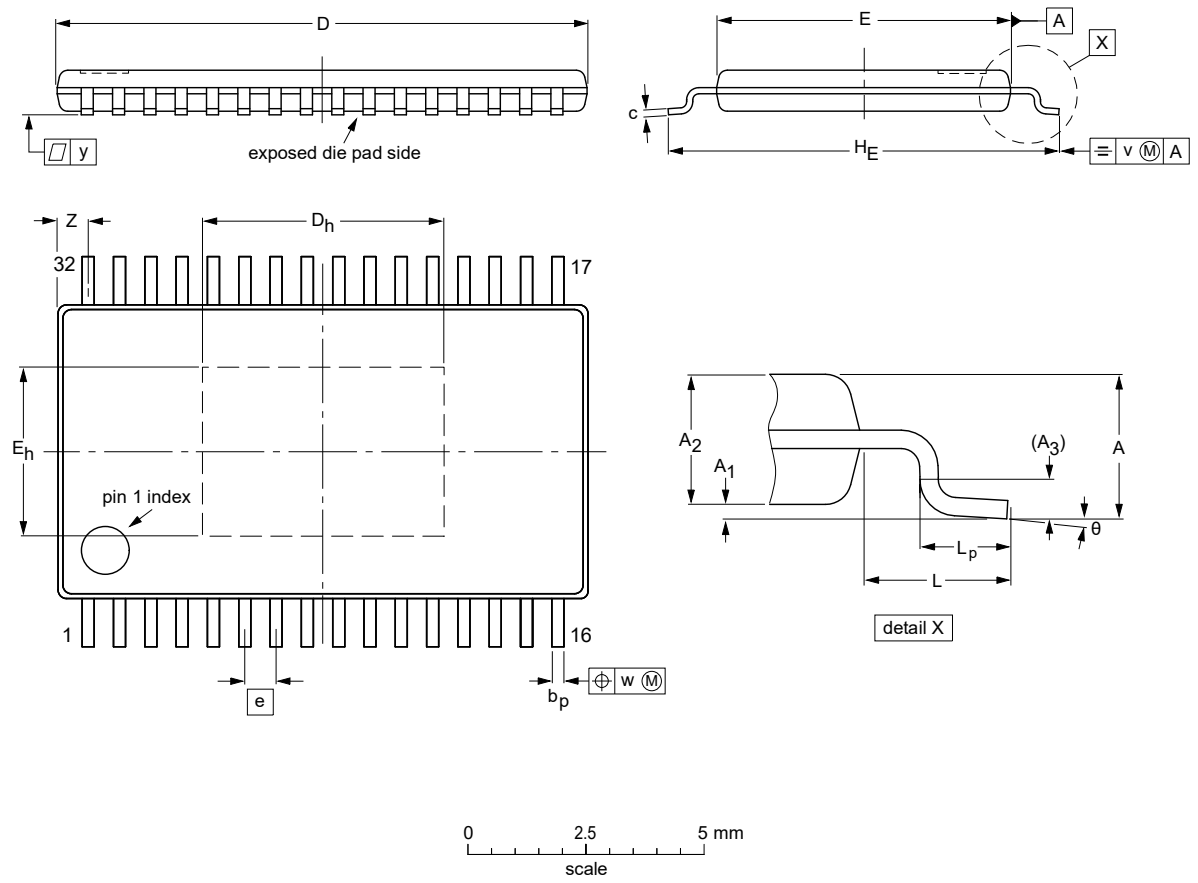
Figure 19. Timing test circuit for LIN transceivers

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13 Package outline

HTSSOP32: plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad **SOT549-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	5.1 4.9	6.2 6.0	3.6 3.4	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT549-1		MO-153				~~03-04-07~~ 05-11-02

Figure 20. Package outline SOT549-1 (HTSSOP32)

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and Table 13

Table 12. SnPb eutectic process (from J-STD-020D)

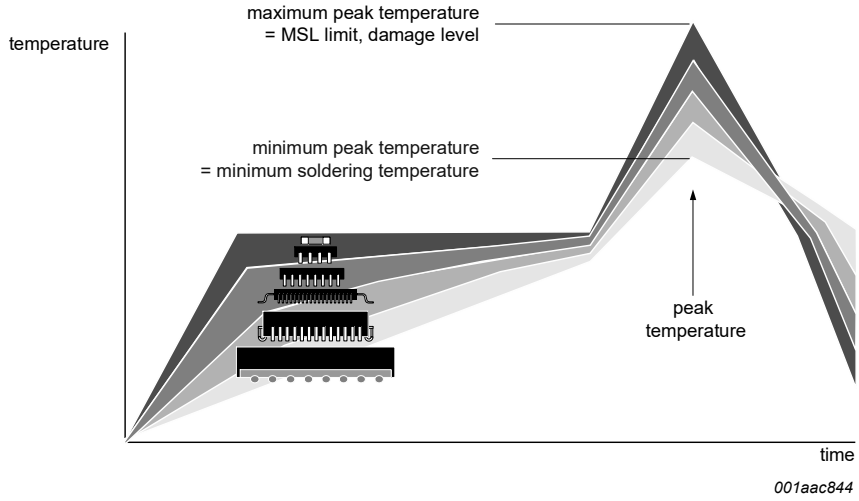
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



MSL: Moisture Sensitivity Level

Figure 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15 Revision history

Table 14. Revision history

Document ID	Release date	Description
UJA1078A v.3.0	10 December 2024	Product data sheet Modifications: • Section 1, Section 2.3, Section 6.8: now LIN 2.2/LIN 2.2A compliant • Table 1: device type numbers revised • Figure 1: pin VEXCC changed to input • Table 2: 'Type' column and table notes added (table note 2 replaces original text below table) • Section 6: added footnote 1 • Section 6.5.1: text amended 900 Ω changed to 1000 Ω (typo) • Section 6.6.2: text of 3rd and 6th paragraphs revised • Section 6.6.2, Table 5 (bit PDC): text and Figure 7, Figure 8 revised • Section 6.8: terms master/slave changed to commander/responder • Table 8: revised • Table 9: thermal characteristics revised • Table 10: table note 1 added; table note 2 amended; LIN symbol names and parameter descriptions updated to conform to LIN specification: – $I_{L(log)}$ changed to $I_{BUS\_NO\_GND}$ – $I_{L(lob)}$ changed to $I_{BUS\_NO\_BAT}$ – $V_{rec(RX)}$ changed to V_{BUSrec} – $V_{dom(RX)}$ changed to V_{BUSdom} – $V_{th(cntr)RX}$ changed to V_{BUS_CNT} – $V_{th(hys)RX}$ changed to V_{HYS} • Table 11: table note 1 added; figure references added in subheadings • Section 11 added • Section 12.1: AEC-Q100 reference clarified • Legal information: 'Suitability for use in automotive applications' updated
UJA1078A v.2.0	28 January 2011	Product data sheet
UJA1078A v.1.0	9 July 2010	Product data sheet; initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Contents