

## 3-V to 5.5-V Multichannel RS-232 Compatible Line Driver and Receiver

### 1 Features

- Operate with 3-V to 5.5-V  $V_{CC}$  supply
- Operate up to 1 Mbit/s
- Low supply current: 300  $\mu$ A typical
- External capacitors:  $4 \times 0.1 \mu$ F
- Accept 5-V logic input with 3.3-V supply
- RS-232 bus-pin ESD protection exceeds  $\pm 15$  kV using human-body model (HBM)

### 2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

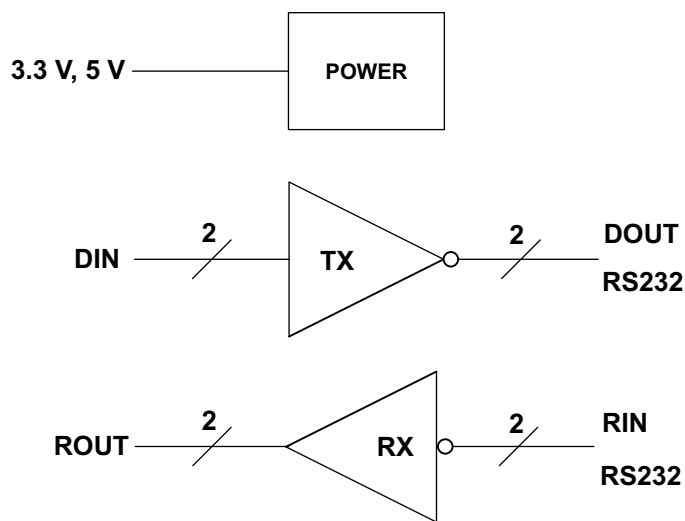
### 3 Description

The SN65C3232 and SN75C3232 consist of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin-to-pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at typical data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ $\mu$ s to 150 V/ $\mu$ s.

#### Device Information

| PART NUMBER            | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|------------------------|------------------------|-------------------|
| SN65C3232<br>SN75C3232 | D (SOIC) (16)          | 9.90 mm x 3.91 mm |
|                        | DB (SSOP) (16)         | 6.20 mm x 5.30 mm |
|                        | DW (SOIC) (16)         | 10.3 mm x 7.50 mm |
|                        | PW (TSSOP) (16)        | 5.00 mm v 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Diagram



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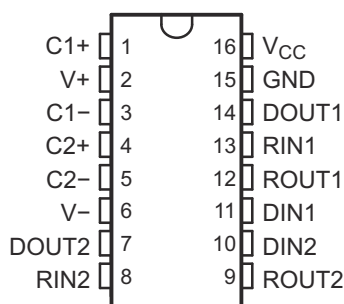
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision B (November 2004) to Revision C (June 2021)</b>                                                                                                                                                                                                                                                                                                                                                              | <b>Page</b> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1           |
| • Added <i>Applications</i> : Industrial PCs, Wired networking, and Data center and enterprise computing.....                                                                                                                                                                                                                                                                                                                         | 1           |
| • Added thermal parameter values for all packages and changed the thermal parameters for D package in the <i>Thermal Information</i> table.....                                                                                                                                                                                                                                                                                       | 5           |

## 5 Pin Configuration and Functions



**Figure 5-1. D, DW, DB and PW Package, 16-Pin SOIC, SSOP and TSSOP, Top View**

| PIN   |     | I/O | DESCRIPTION                                                   |
|-------|-----|-----|---------------------------------------------------------------|
| NAME  | NO. |     |                                                               |
| C1+   | 1   | —   | Positive lead of C1 capacitor                                 |
| V+    | 2   | O   | Positive charge pump output for storage capacitor only        |
| C1-   | 3   | —   | Negative lead of C1 capacitor                                 |
| C2+   | 4   | —   | Positive lead of C2 capacitor                                 |
| C2-   | 5   | —   | Negative lead of C2 capacitor                                 |
| V-    | 6   | O   | Negative charge pump output for storage capacitor only        |
| DOUT2 | 7   | O   | RS232 line data output (to remote RS232 system)               |
| RIN2  | 8   | I   | RS232 line data input (from remote RS232 system)              |
| ROUT2 | 9   | O   | Logic data output (to UART)                                   |
| DIN2  | 10  | I   | Logic data input (from UART)                                  |
| DIN1  | 11  | I   | Logic data input (from UART)                                  |
| ROUT1 | 12  | O   | Logic data output (to UART)                                   |
| RIN1  | 13  | I   | RS232 line data input (from remote RS232 system)              |
| DOUT1 | 14  | O   | RS232 line data output (to remote RS232 system)               |
| GND   | 15  | —   | Ground                                                        |
| VCC   | 16  | —   | Supply Voltage, Connect to external 3-V to 5.5-V power supply |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                                     |           | MIN   | MAX                   | UNIT |
|------------------|-----------------------------------------------------|-----------|-------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range <sup>(2)</sup>                 |           | −0.3  | 6                     | V    |
| V+               | Positive-output supply voltage range <sup>(2)</sup> |           | −0.3  | 7                     | V    |
| V−               | Negative-output supply voltage range <sup>(2)</sup> |           | 0.3   | −7                    | V    |
| V+ − V−          | Supply voltage difference <sup>(2)</sup>            |           |       | 13                    | V    |
| V <sub>I</sub>   | Input voltage range                                 | Drivers   | −0.3  | 6                     | V    |
|                  |                                                     | Receivers | −25   | 25                    |      |
| V <sub>O</sub>   | Output voltage range                                | Drivers   | −13.2 | 13.2                  | V    |
|                  |                                                     | Receivers | −0.3  | V <sub>CC</sub> + 0.3 |      |
| T <sub>J</sub>   | Operating virtual junction temperature              |           |       | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature range                           |           | −65   | 150                   | °C   |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

|                    |                         |                                                                                |                              | VALUE   | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|------------------------------|---------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | All pins except RIN and DOUT | ±3000   | V    |
|                    |                         |                                                                                | RIN and DOUT Pins            | ±15,000 |      |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | All pins                     | ±1500   |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See [Typical Operating Circuit and Capacitor Values](#), See <sup>(1)</sup>

|                 |                                 |                         | MIN                     | NOM | MAX | UNIT |
|-----------------|---------------------------------|-------------------------|-------------------------|-----|-----|------|
| Supply voltage  |                                 | V <sub>CC</sub> = 3.3 V | 3                       | 3.3 | 3.6 | V    |
|                 |                                 | V <sub>CC</sub> = 5 V   | 4.5                     | 5   | 5.5 |      |
| V <sub>IH</sub> | Driver high-level input voltage | DIN                     | V <sub>CC</sub> = 3.3 V | 2   |     | V    |
|                 |                                 |                         | V <sub>CC</sub> = 5 V   | 2.4 |     |      |
| V <sub>IL</sub> | Driver low-level input voltage  | DIN                     |                         |     | 0.8 | V    |
| V <sub>I</sub>  | Driver input voltage            | DIN                     | 0                       |     | 5.5 | V    |
|                 | Receiver input voltage          |                         | −25                     |     | 25  |      |
| T <sub>A</sub>  | Operating free-air temperature  | SN75C3232               | 0                       |     | 70  | °C   |
|                 |                                 | SN65C3232               | −40                     |     | 85  |      |

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN65C3232, SN75C3232 |          |           |           | UNIT |
|-------------------------------|----------------------------------------------|----------------------|----------|-----------|-----------|------|
|                               |                                              | PW (TSSOP)           | D (SOIC) | DW (SOIC) | DB (SSOP) |      |
|                               |                                              | 16 PINS              | 16 PINS  | 16 PINS   | 16 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 108.0                | 85.9     | 57.0      | 46.0      | °C/W |
| R <sub>θJCTop</sub>           | Junction-to-case (top) thermal resistance    | 20.8                 | 43.1     | 33.5      | 36.2      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 45.1                 | 44.5     | 37.1      | 43.8      | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.6                  | 10.1     | 7.5       | 4.2       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 45.1                 | 44.1     | 37.1      | 42.9      | °C/W |
| R <sub>θJBot</sub>            | Junction-to-case (bottom) thermal resistance | –                    | –        | –         | –         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#))

| PARAMETER <sup>(2)</sup> |                | TEST CONDITIONS                         | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|--------------------------|----------------|-----------------------------------------|-----|--------------------|-----|------|
| I <sub>CC</sub>          | Supply current | No load, V <sub>CC</sub> = 3.3 V or 5 V |     | 0.3                | 1   | mA   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.6 Driver Section - Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#))

| PARAMETER                                                   | TEST CONDITIONS <sup>(3)</sup>                                                     | MIN                     | TYP <sup>(1)</sup> | MAX | UNIT |
|-------------------------------------------------------------|------------------------------------------------------------------------------------|-------------------------|--------------------|-----|------|
| V <sub>OH</sub> High-level output voltage                   | DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND                                    | 5                       | 5.4                |     | V    |
| V <sub>OL</sub> Low-level output voltage                    | DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>                        | –5                      | –5.4               |     | V    |
| I <sub>IH</sub> High-level input current                    | V <sub>I</sub> = V <sub>CC</sub>                                                   |                         | ±0.01              | ±1  | μA   |
| I <sub>IL</sub> Low-level input current                     | V <sub>I</sub> at GND                                                              |                         | ±0.01              | ±1  | μA   |
| I <sub>OS</sub> Short-circuit output current <sup>(2)</sup> | V <sub>O</sub> = 0 V                                                               | V <sub>CC</sub> = 3.6 V |                    | ±35 | ±60  |
|                                                             |                                                                                    | V <sub>CC</sub> = 5.5 V |                    | ±35 | ±90  |
| r <sub>o</sub> Output resistance                            | V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V | 300                     | 10M                |     | Ω    |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.7 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#))

| PARAMETER                                                                   | TEST CONDITIONS <sup>(3)</sup>                                                                    | MIN                                                        | TYP <sup>(1)</sup> | MAX  | UNIT   |
|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|------------------------------------------------------------|--------------------|------|--------|
| Maximum data rate<br>(see <a href="#">Figure 7-1</a> )                      | R <sub>L</sub> = 3 kΩ,<br>One DOUT switching                                                      | C <sub>L</sub> = 1000 pF                                   |                    | 250  | kbit/s |
|                                                                             |                                                                                                   | C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V    |                    | 1000 |        |
|                                                                             |                                                                                                   | C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 4.5 V to 5.5 V |                    | 1000 |        |
| t <sub>sk(p)</sub> Pulse skew <sup>(2)</sup>                                | C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, See <a href="#">Figure 7-2</a> |                                                            | 300                |      | ns     |
| SR(tr) Slew rate,<br>transition region<br>(see <a href="#">Figure 7-1</a> ) | R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 150 pF to 1000 pF, V <sub>CC</sub> = 3.3 V        | 18                                                         |                    | 150  | V/μs   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.8 Receiver Section - Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#))

| PARAMETER        |                                                         | TEST CONDITIONS <sup>(2)</sup> | MIN                   | TYP <sup>(1)</sup>    | MAX | UNIT |
|------------------|---------------------------------------------------------|--------------------------------|-----------------------|-----------------------|-----|------|
| V <sub>OH</sub>  | High-level output voltage                               | I <sub>OH</sub> = –1 mA        | V <sub>CC</sub> – 0.6 | V <sub>CC</sub> – 0.1 |     | V    |
| V <sub>OL</sub>  | Low-level output voltage                                | I <sub>OL</sub> = 1.6 mA       |                       |                       | 0.4 | V    |
| V <sub>IT+</sub> | Positive-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        |                       | 1.5                   | 2.4 | V    |
|                  |                                                         | V <sub>CC</sub> = 5 V          |                       | 1.8                   | 2.4 |      |
| V <sub>IT–</sub> | Negative-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        | 0.6                   | 1.2                   |     | V    |
|                  |                                                         | V <sub>CC</sub> = 5 V          | 0.8                   | 1.5                   |     |      |
| V <sub>hys</sub> | Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                |                       | 0.3                   |     | V    |
| r <sub>i</sub>   | Input resistance                                        | V <sub>I</sub> = ±3 V to ±25 V | 3                     | 5                     | 7   | kΩ   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.9 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Typical Operating Circuit and Capacitor Values](#))

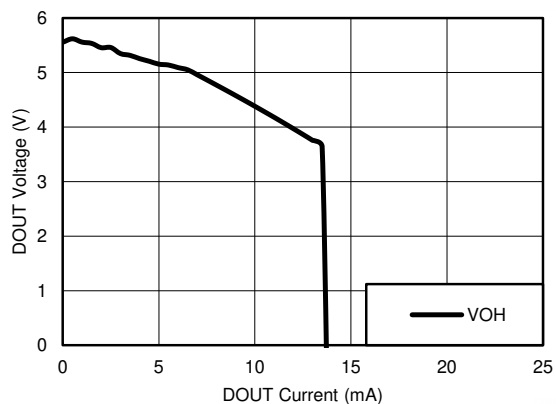
| PARAMETER          |                                                   | TEST CONDITIONS <sup>(3)</sup> | TYP <sup>(1)</sup> | UNIT |
|--------------------|---------------------------------------------------|--------------------------------|--------------------|------|
| t <sub>PLH</sub>   | Propagation delay time, low- to high-level output | C <sub>L</sub> = 150 pF        | 300                | ns   |
| t <sub>PHL</sub>   | Propagation delay time, high- to low-level output | C <sub>L</sub> = 150 pF        | 300                | ns   |
| t <sub>sk(p)</sub> | Pulse skew <sup>(2)</sup>                         |                                | 300                | ns   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

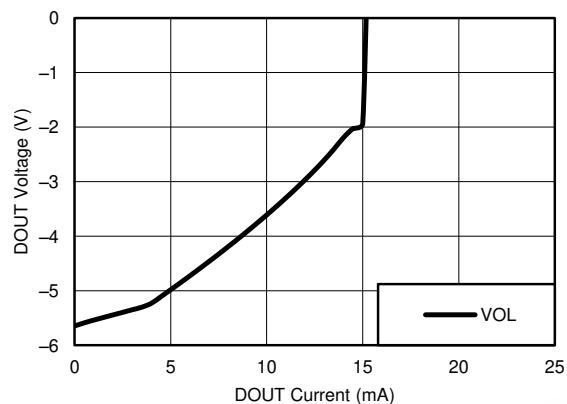
(3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.10 Typical Characteristics



$V_{CC} = 3.3\text{ V}$

**Figure 6-1. DOUT  $V_{OH}$  vs Load Current, Both Drivers Loaded**

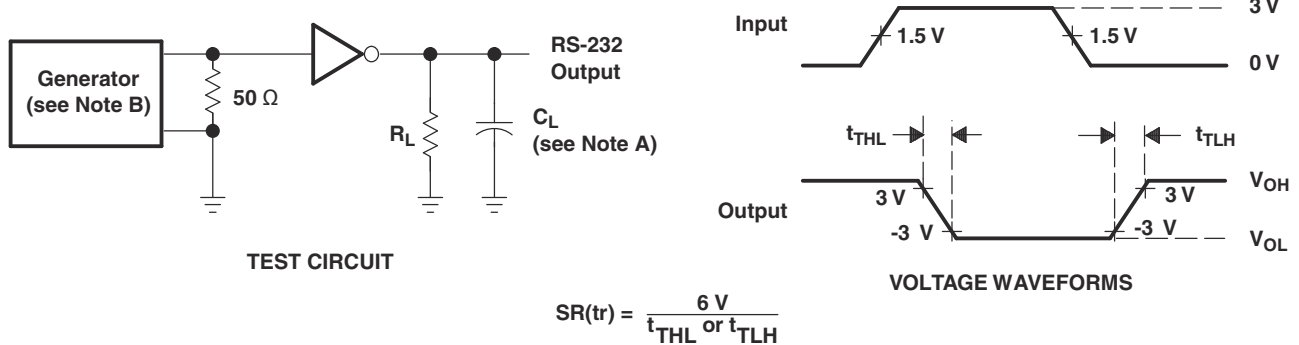


$V_{CC} = 3.3\text{ V}$

**Figure 6-2. DOUT  $V_{OL}$  vs Load Current, Both Drivers Loaded**

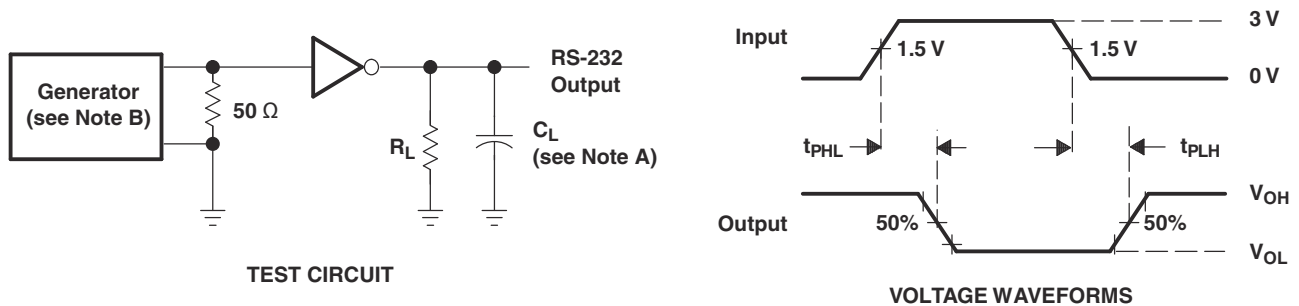


## 7 Parameter Measurement Information



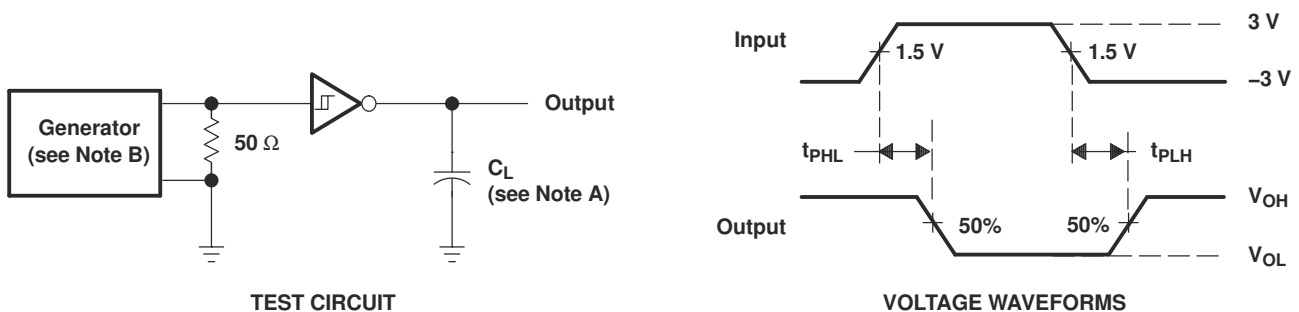
- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

**Figure 7-1. Driver Slew Rate**



- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

**Figure 7-2. Driver Pulse Skew**



- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

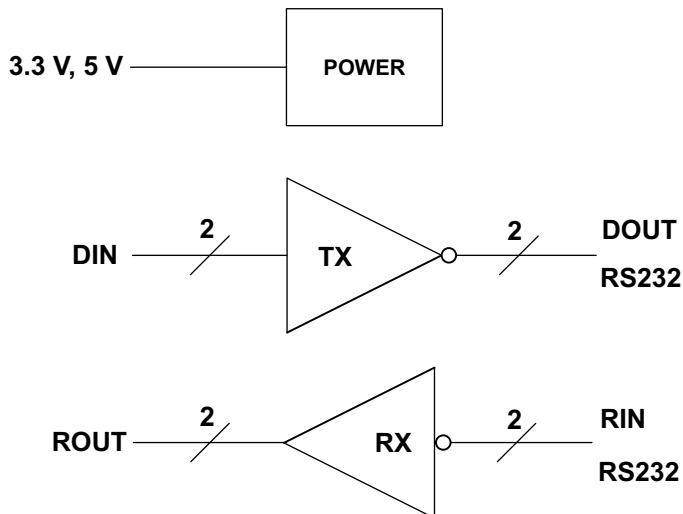
**Figure 7-3. Receiver Propagation Delay Times**

## 8 Detailed Description

### 8.1 Overview

The device consists of two line drivers, two-line receivers, and a dual charge-pump circuit with IEC61000-4-2 ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

#### 8.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

#### 8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

## 8.4 Device Functional Modes

Table 8-1 and Table 8-2 list the functional modes of the drivers and receivers of MAX3232E.

**Table 8-1. Each Driver<sup>(1)</sup>**

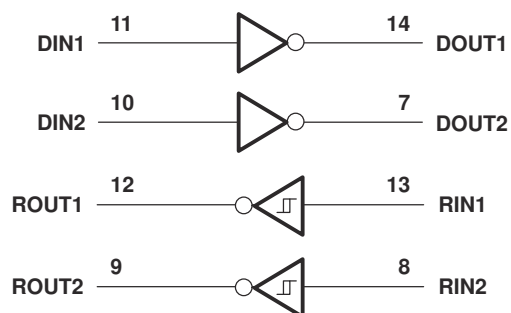
| INPUT<br>DIN | OUTPUT<br>DOUT |
|--------------|----------------|
| L            | H              |
| H            | L              |

(1) H = high level, L = low level

**Table 8-2. Each Receiver<sup>(1)</sup>**

| INPUT<br>RIN | OUTPUT<br>ROUT |
|--------------|----------------|
| L            | H              |
| H            | L              |
| Open         | H              |

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off



**Figure 8-1. Logic Diagram**

### 8.4.1 $V_{CC}$ Powered by 3 V to 5.5 V

The device is in normal operation.

### 8.4.2 $V_{CC}$ Unpowered, $V_{CC} = 0$ V

When the device is unpowered, it can be safely connected to an active remote RS232 device.

## 9 Application and Implementation

### Note

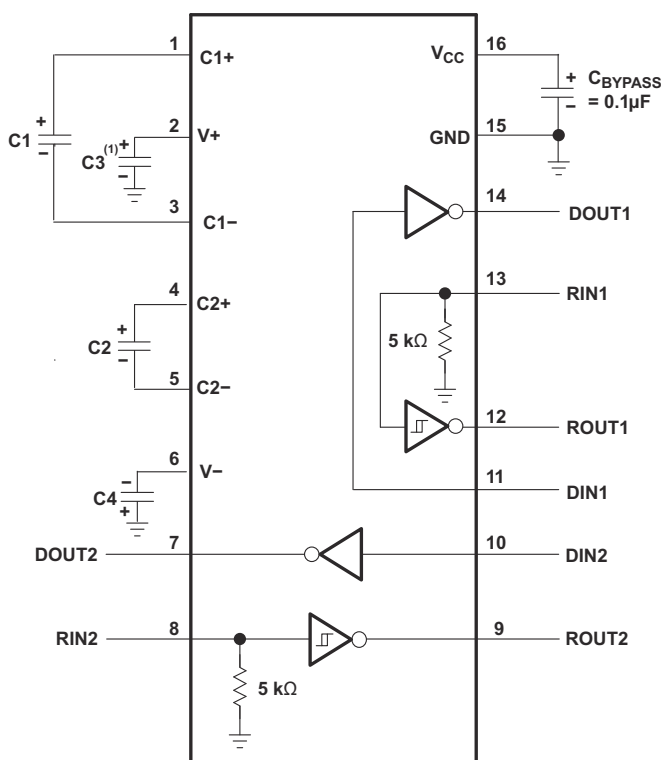
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

For proper operation, add capacitors as shown in [Table 9-1](#).

#### 9.1.1 Typical Application

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



A. C3 can be connected to  $V_{CC}$  or GND

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 9-1. Typical Operating Circuit and Capacitor Values**

**Table 9-1. VCC vs Capacitor Values**

| V <sub>CC</sub> | C1       | C2, C3, C4 |
|-----------------|----------|------------|
| 3.3 V ± 0.3 V   | 0.1 μF   | 0.1 μF     |
| 5 V ± 0.5 V     | 0.047 μF | 0.33 μF    |
| 3 V to 5.5 V    | 0.1 μF   | 0.47 μF    |

### 9.1.1.1 Design Requirements

The recommended  $V_{CC}$  is 3.3 V or 5 V. 3 V to 5.5 V is also possible

The maximum recommended bit rate is 250 kbit/s.

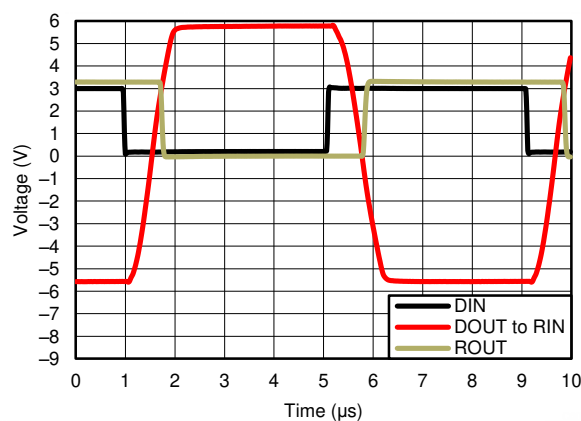
### 9.1.1.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on  $V_{CC}$  level for best performance.

### 9.1.1.3 Application Performance Plots

Figure 9-2 curves are for 3.3-V  $V_{CC}$  and 250-kbit/s alternative bit data stream.



**Figure 9-2. 250 kbit/s Driver to Receiver Loopback Timing Waveform,  $V_{CC} = 3.3$  V**

## 10 Layout

### 10.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

### 10.2 Layout Example

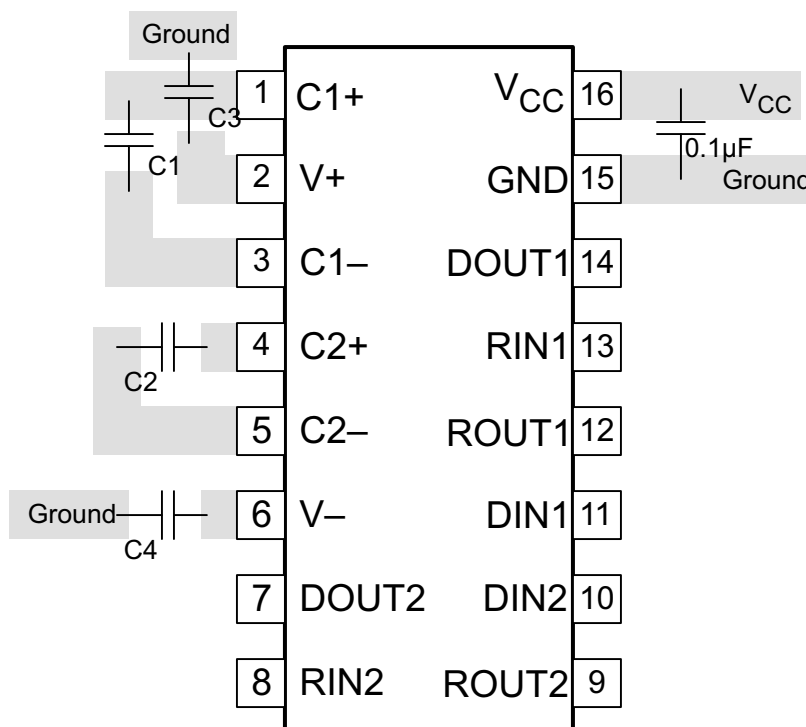


Figure 10-1. Layout Diagram

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

##### 11.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65C3232D</a>   | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | 65C3232             |
| <a href="#">SN65C3232DBR</a> | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| SN65C3232DBR.A               | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| <a href="#">SN65C3232DR</a>  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| SN65C3232DR.A                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| SN65C3232DRG4.A              | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| <a href="#">SN65C3232DW</a>  | Active        | Production           | SOIC (DW)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| SN65C3232DW.A                | Active        | Production           | SOIC (DW)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| <a href="#">SN65C3232DWR</a> | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| SN65C3232DWR.A               | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65C3232             |
| <a href="#">SN65C3232PWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CB3232              |
| SN65C3232PWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CB3232              |
| <a href="#">SN75C3232D</a>   | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75C3232             |
| <a href="#">SN75C3232DBR</a> | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | CA3232              |
| SN75C3232DBR.A               | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | CA3232              |
| <a href="#">SN75C3232DR</a>  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |
| SN75C3232DR.A                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |
| <a href="#">SN75C3232DW</a>  | Active        | Production           | SOIC (DW)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |
| SN75C3232DW.A                | Active        | Production           | SOIC (DW)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |
| <a href="#">SN75C3232DWR</a> | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |
| SN75C3232DWR.A               | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 75C3232             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.



(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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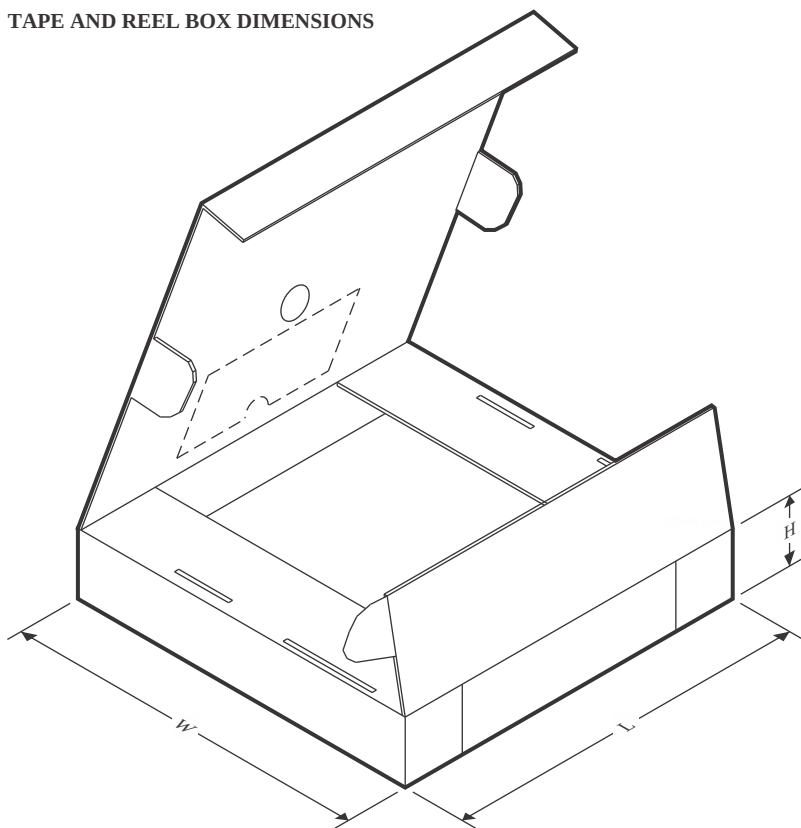
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C3232DBR | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN65C3232DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN65C3232DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| SN65C3232PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN65C3232PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN75C3232DBR | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN75C3232DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN75C3232DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C3232DBR | SSOP         | DB              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN65C3232DR  | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| SN65C3232DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| SN65C3232PWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN65C3232PWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN75C3232DBR | SSOP         | DB              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN75C3232DR  | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| SN75C3232DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |

## TUBE

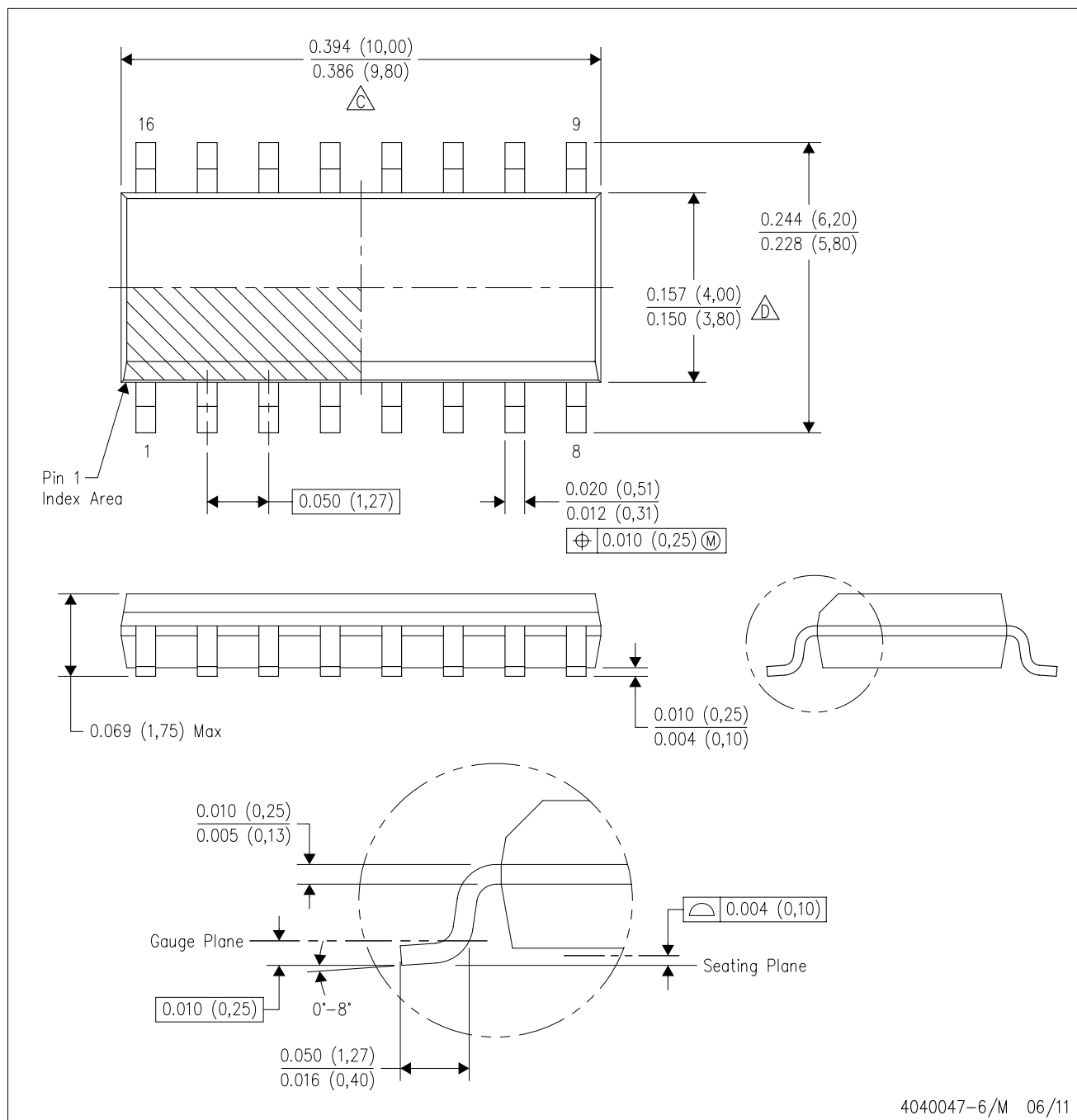


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65C3232DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| SN65C3232DW.A | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| SN75C3232DW   | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| SN75C3232DW.A | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |

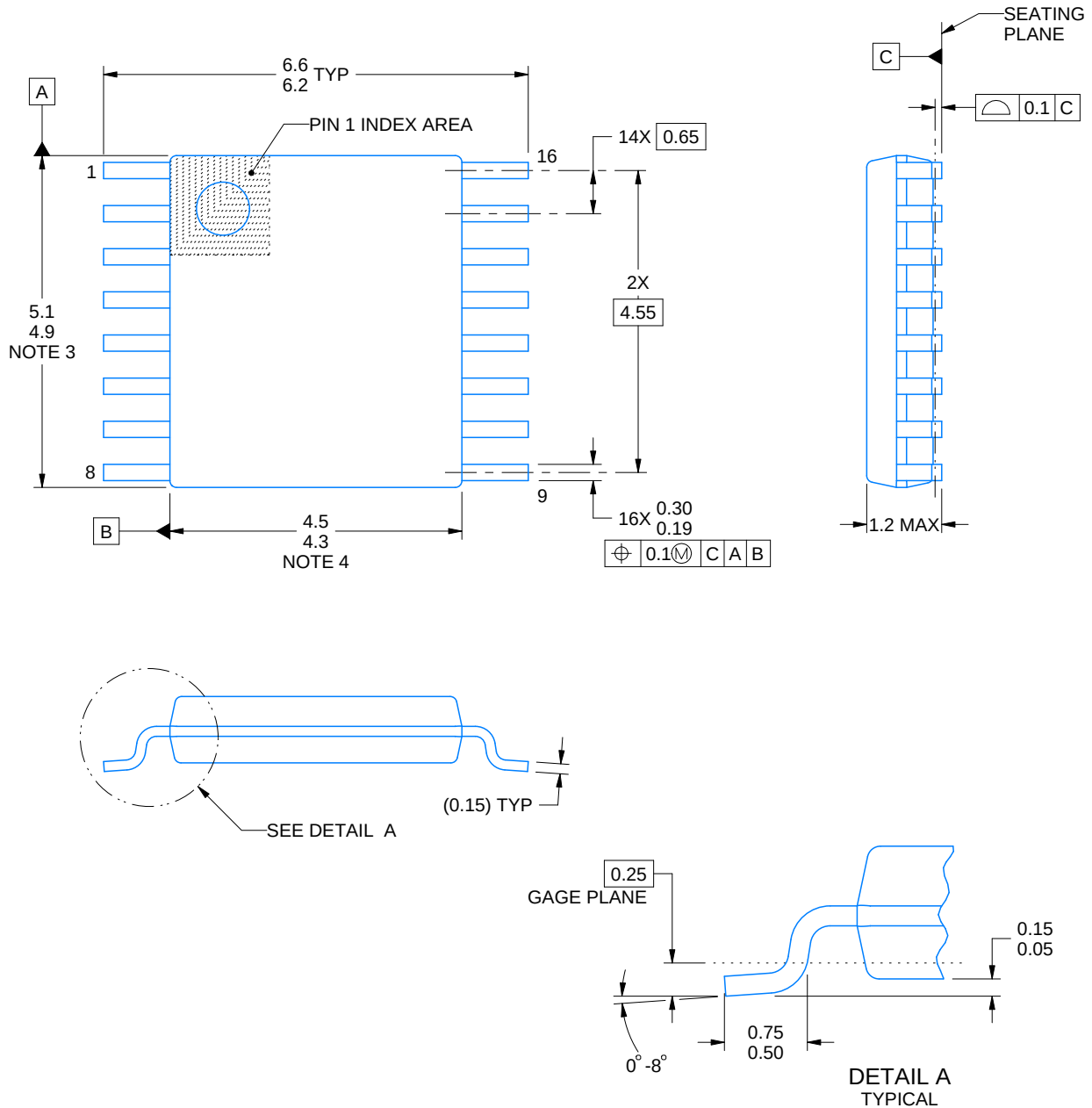
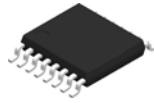
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

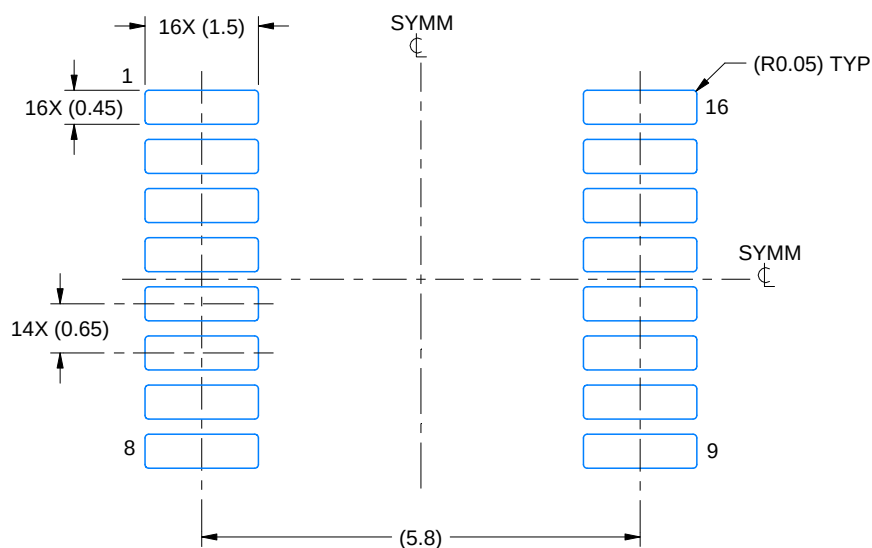
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

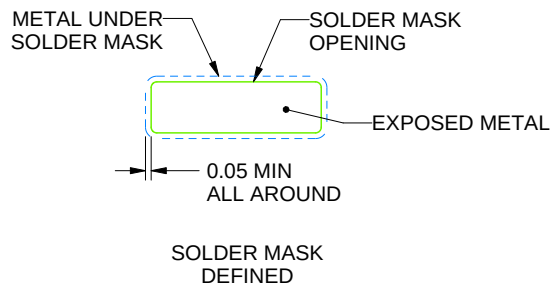
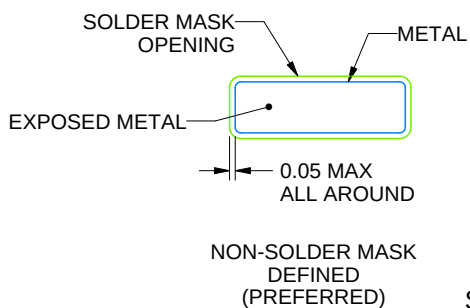
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

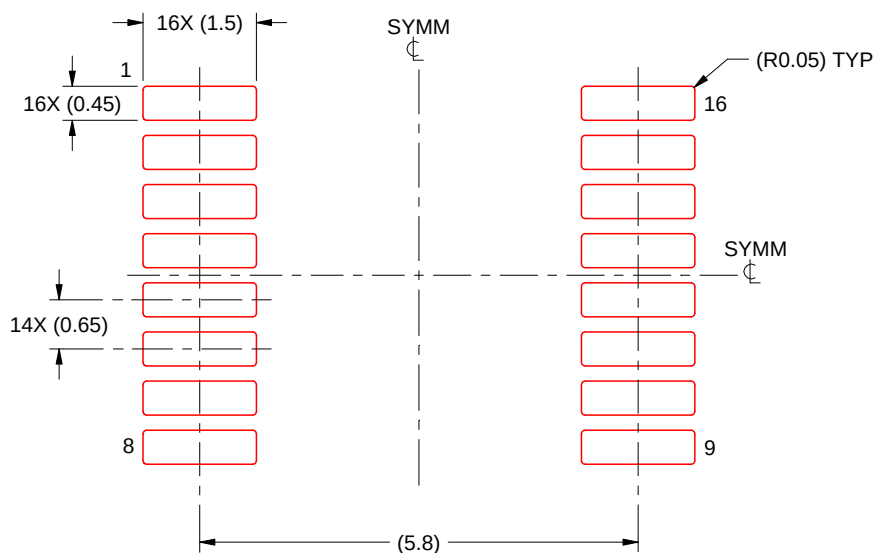
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



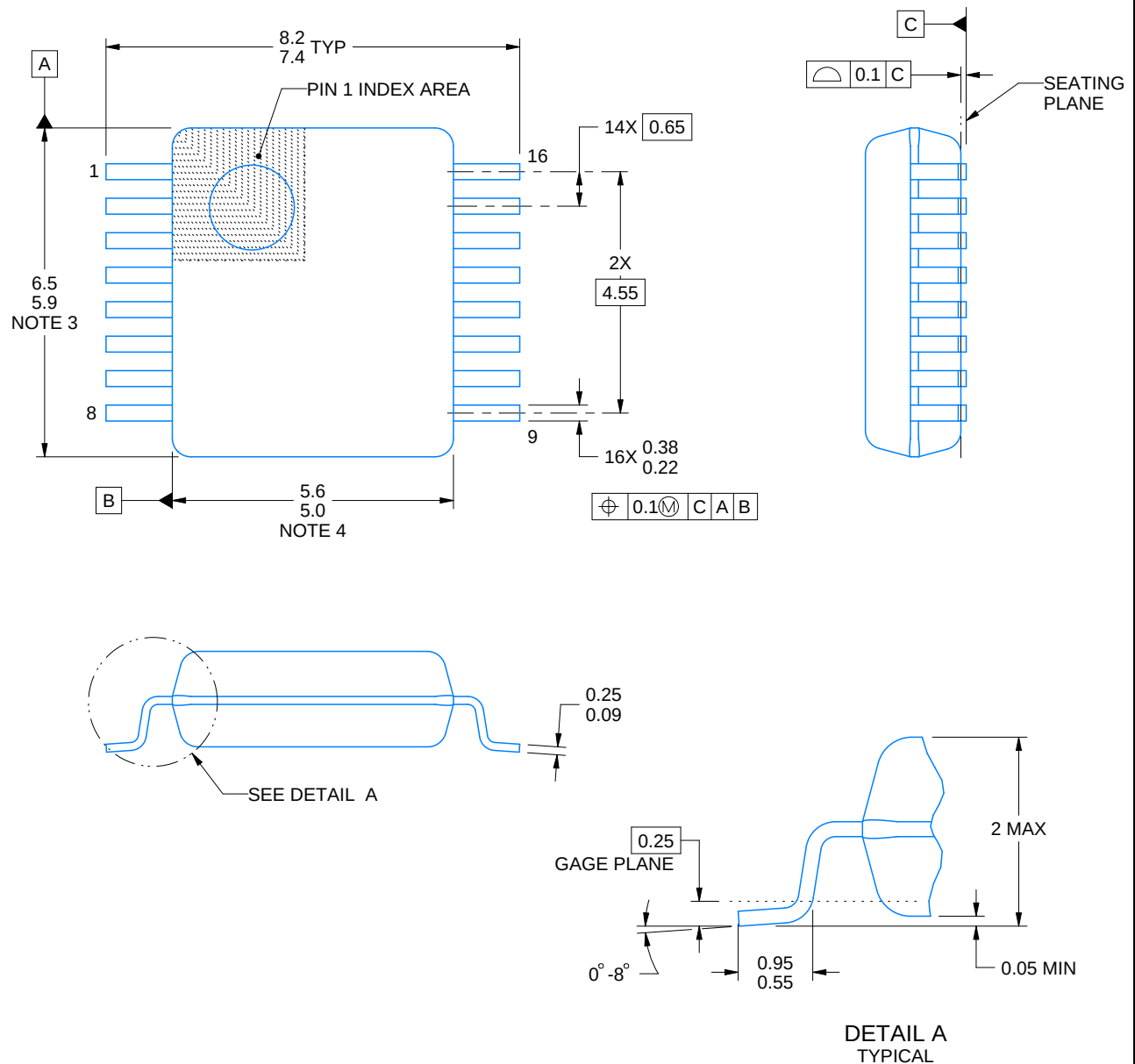
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





4220763/A 05/2022

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

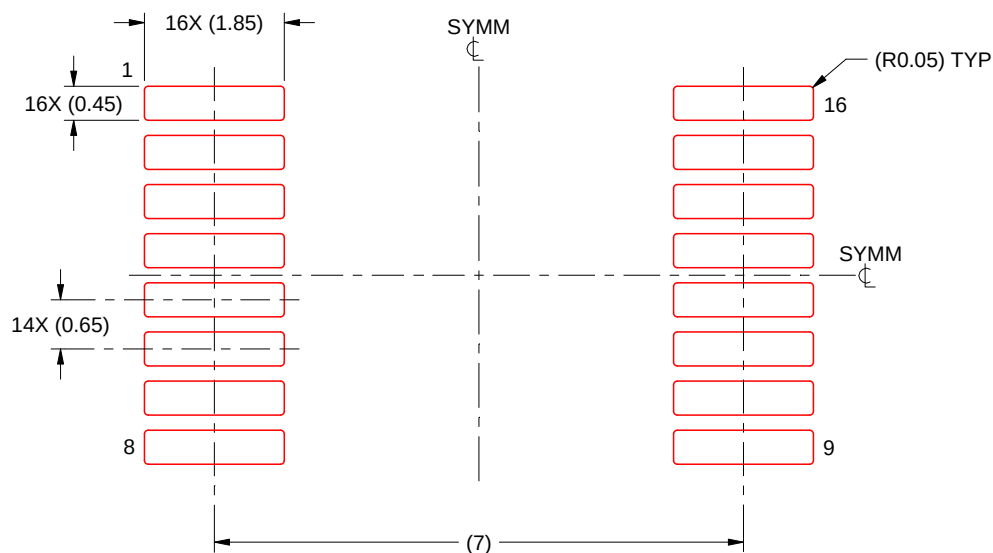


## EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

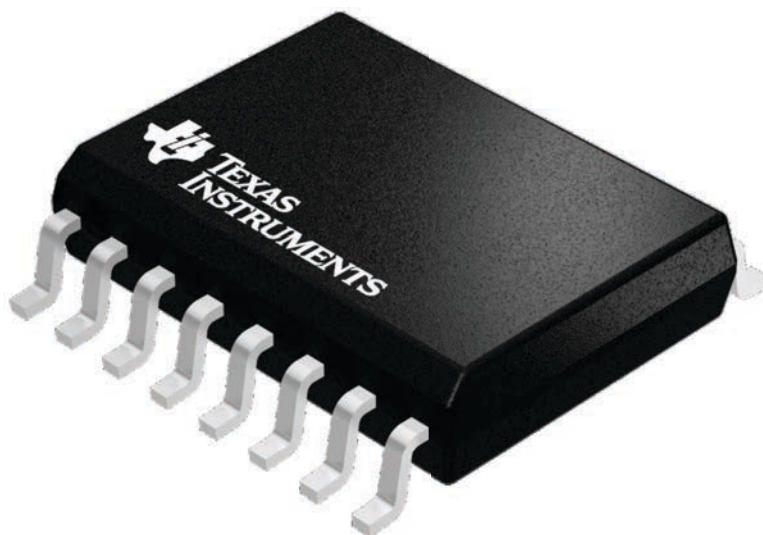
**DW 16**

**SOIC - 2.65 mm max height**

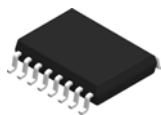
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

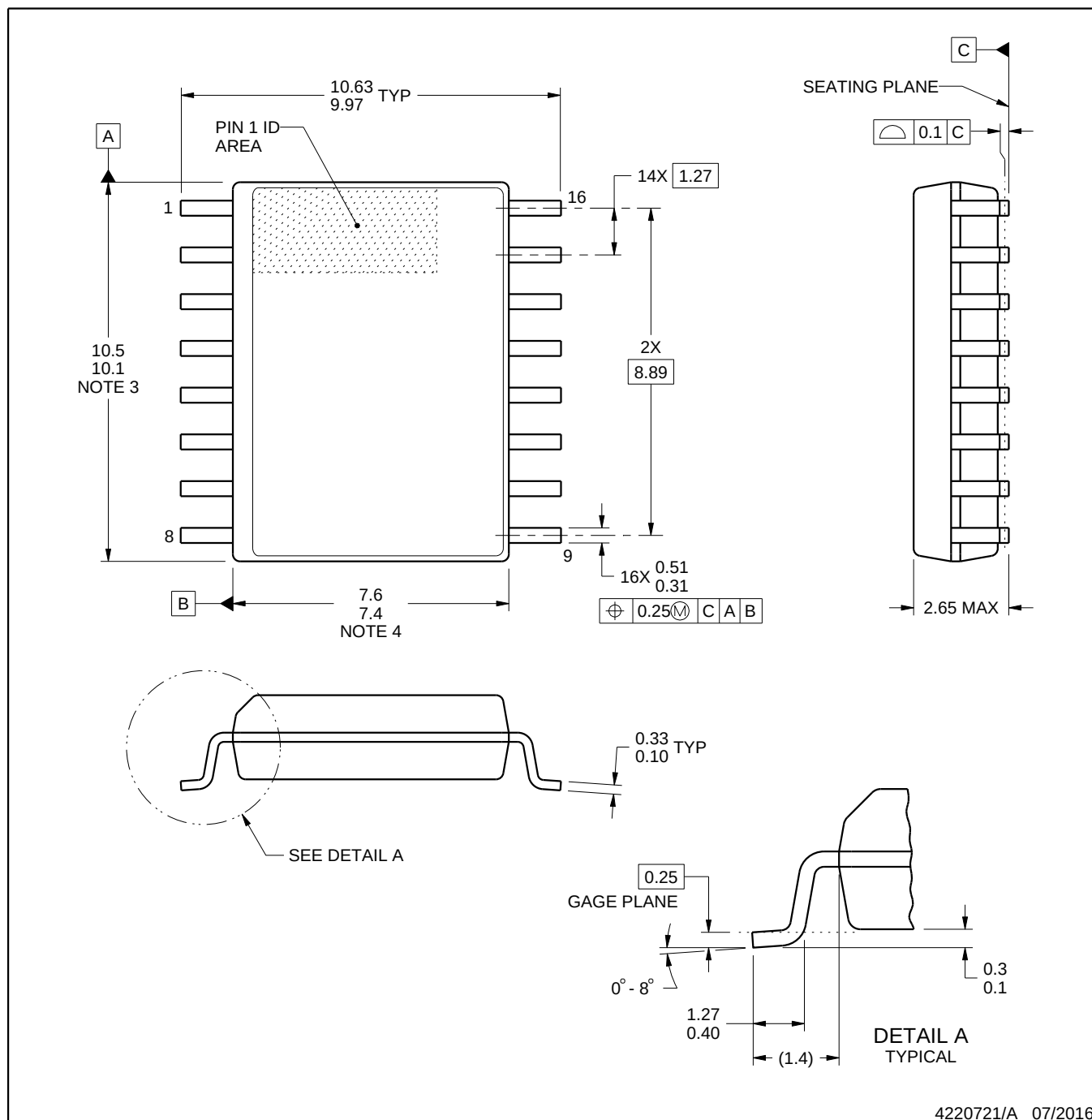


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

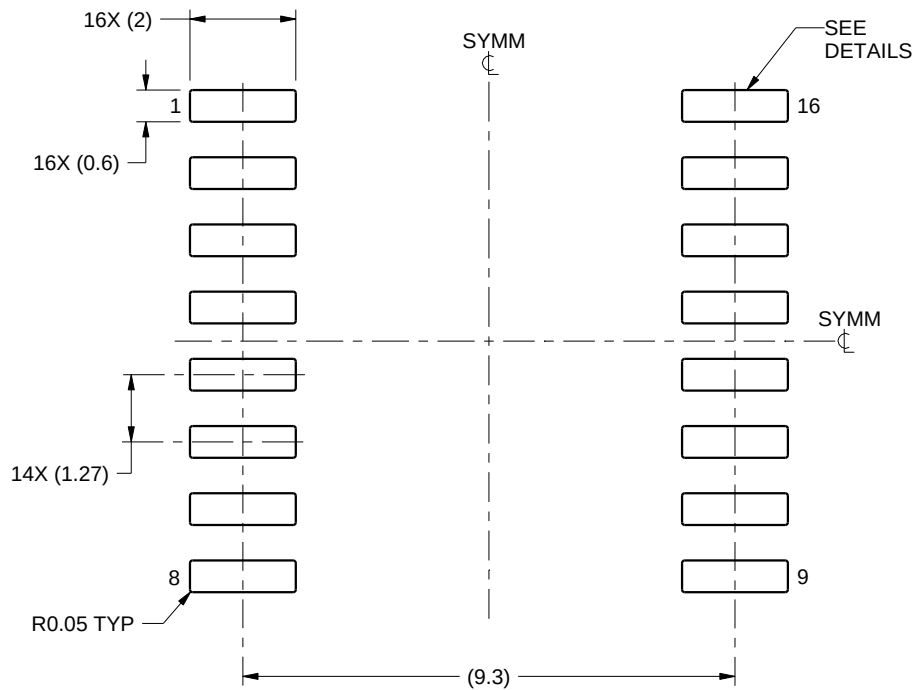
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

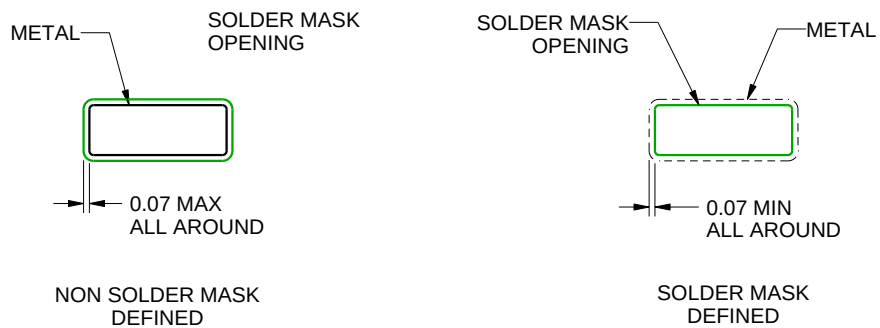
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

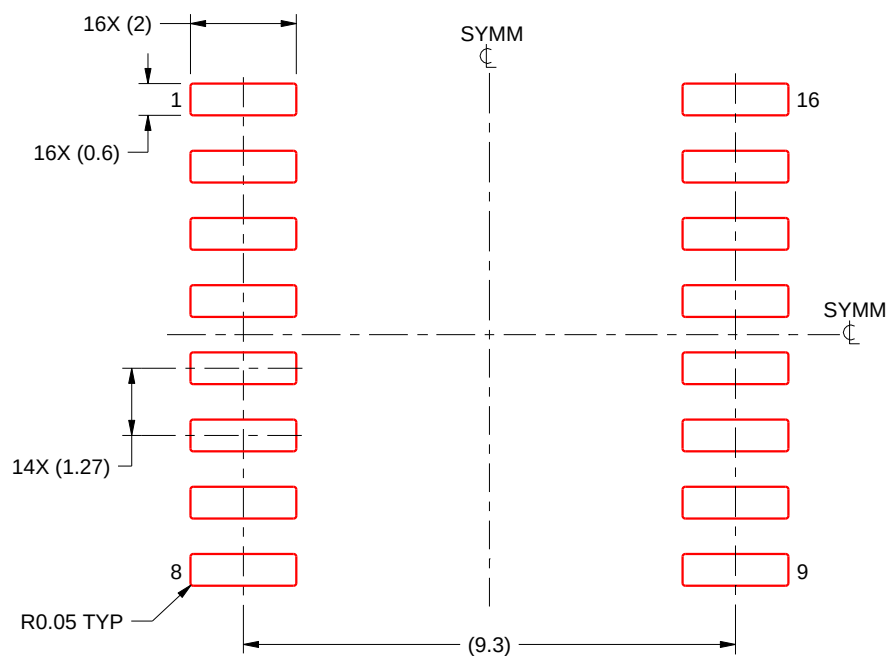
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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