DS89C21 Differential CMOS Line Driver and Receiver Pair

Check for Samples: DS89C21

FEATURES

- **Meets TIA/EIA-422-A (RS-422) and CCITT V.11 Recommendation**
- **LOW POWER Design—15 mW Typical**
- **Guaranteed AC Parameters:**
  - **Maximum Driver Skew 2.0 ns**
  - **Maximum Receiver Skew 4.0 ns**
- **Extended Temperature Range: −40°C to +85°C**
- **Available in SOIC Packaging**
- **Operates over 20 Mbps**
- **Receiver OPEN Input Failsafe Feature**

DESCRIPTION

The DS89C21 is a differential CMOS line driver and receiver pair, designed to meet the requirements of TIA/EIA-422-A (RS-422) electrical characteristics interface standard. The DS89C21 provides one driver and one receiver in a minimum footprint. The device is offered in an 8-pin SOIC package.

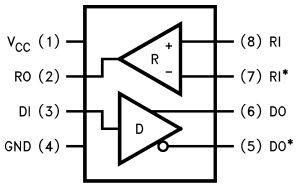
The CMOS design minimizes the supply current to 6 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 2.2 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 10 MHz.

The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

The DS89C21 is compatible with TTL and CMOS levels (DI and RO).

Connection Diagram



See Package Number D (R-PDSO-G8)

Truth Table Driver

Input	Outputs	
DI	**DO**	**DO***
H	H	L
L	L	H

Truth Table Receiver

Inputs	Output
RI–RI*	**RO**
V_{DIFF} ≥ +200 mV	H
V_{DIFF} ≤ −200 mV	L
OPEN(1)	H

(1) Non-terminated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Supply Voltage (V_{CC})	7V
Driver Input Voltage (DI)	−1.5V to V_{CC} + 1.5V
Driver Output Voltage (DO, DO *)	−0.5V to +7V
Receiver Input Voltage—V_{CM}	
(RI, RI*)	±14V
Differential Receiver Input	±14V
Voltage—V_{DIFF} (RI, RI*)	
Receiver Output Voltage (RO)	−0.5V to V_{CC} +0.5V
Receiver Output Current (RO)	±25 mA
Storage Temperature Range	
(T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	+260°C
(Soldering 4 sec.)	
Maximum Junction Temperature	150°C
Maximum Package Power Dissipation @+25°C	
D Package	714 mW
Derate D Package	5.7 mW/°C above +25°C

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) all pins ≥ 2000V.EIAJ (0Ω, 200 pF) ≥ 250V

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature (T_A)	−40	+85	°C
Input Rise or Fall Time (DI)		500	ns

Electrical Characteristics (1)(2)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
V_{IH}	Input Voltage HIGH			DI	2.0		V_{CC}	V
V_{IL}	Input Voltage LOW				GND		0.8	V
I_{IH}, I_{IL}	Input Current	$V_{IN} = V_{CC}$, GND, 2.0V, 0.8V				0.05	±10	µA
V_{CL}	Input Clamp Voltage	$I_{IN} = -18$ mA					−1.5	V
V_{OD1}	Unloaded Output Voltage	No Load		DO, DO*		4.2	6.0	V
V_{OD2}	Differential Output Voltage	$R_L = 100\Omega$			2.0	3.0		V
ΔV_{OD2}	Change in Magnitude of V_{OD2} for Complementary Output States					5.0	400	mV
V_{OD3}	Differential Output Voltage	$R_L = 150\Omega$			2.1	3.1		V
V_{OD4}	Differential Output Voltage	$R_L = 3.9\ k\Omega$				4.0	6.0	V
V_{OC}	Common Mode Voltage	$R_L = 100\Omega$				2.0	3.0	V
ΔV_{OC}	Change in Magnitude of V_{OC} for Complementary Output States					2.0	400	mV
I_{OSD}	Output Short Circuit Current	$V_{OUT} = 0V$			−30	−115	−150	mA
I_{OFF}	Output Leakage Current	$V_{CC} = 0V$	$V_{OUT} = +6V$			0.03	+100	µA
			$V_{OUT} = -0.25V$			−0.08	−100	µA
RECEIVER CHARACTERISTICS								
V_{TL}, V_{TH}	Differential Thresholds	$V_{IN} = +7V, 0V, -7V$		RI, RI*	−200	±25	+200	mV
V_{HYS}	Hysteresis	$V_{CM} = 0V$			20	50		mV
R_{IN}	Input Impedance	$V_{IN} = -7V, +7V$, Other = 0V			5.0	9.5		kΩ
I_{IN}	Input Current	Other Input = 0V, V_{CC} = 5.5V and V_{CC} = 0V	$V_{IN} = +10V$			+1.0	+1.5	mA
			$V_{IN} = +3.0V$		0	+0.22		mA
			$V_{IN} = +0.5V$			−0.04		mA
			$V_{IN} = -3V$		0	−0.41		mA
			$V_{IN} = -10V$			−1.25	−2.5	mA
V_{OH}	Output HIGH Voltage	$I_{OH} = -6$ mA	$V_{DIFF} = +1V$	RO	3.8	4.9		V
			V_{DIFF} = OPEN		3.8	4.9		V
V_{OL}	Output LOW Voltage	$I_{OL} = +6$ mA, $V_{DIFF} = -1V$				0.08	0.3	V
I_{OSR}	Output Short Circuit Current	$V_{OUT} = 0V$			−25	−85	−150	mA
DRIVER AND RECEIVER CHARACTERISTICS								
I_{CC}	Supply Current	No Load	DI = V_{CC} or GND	V_{CC}		3.0	6	mA
			DI = 2.4V or 0.5V			3.8	12	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Switching Characteristics (1)(2)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
t_{PLHD}	Propagation Delay LOW to HIGH	R_L = 100Ω	(Figure 2 Figure 3)	2	4.9	10	ns
t_{PHLD}	Propagation Delay HIGH to LOW	C_L = 50 pF		2	4.5	10	ns
t_{SKD}	Skew, $\|t_{PLHD} - t_{PHLD}\|$				0.4	2.0	ns
t_{TLH}	Transition Time LOW to HIGH		(Figure 2 Figure 4)		2.2	9	ns
t_{THL}	Transition Time HIGH to LOW				2.1	9	ns
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF	(Figure 5 Figure 6)	6	18	30	ns
t_{PHL}	Propagation Delay HIGH to LOW	V_{DIFF} = 2.5V		6	17.5	30	ns
t_{SK}	Skew, $\|t_{PLH} - t_{PHL}\|$	V_{CM} = 0V			0.5	4.0	ns
t_r	Rise Time		(Figure 7)		2.5	9	ns
t_f	Fall Time				2.1	9	ns

(1) All typicals are given for V_{CC} = 5.0V and T_A = 25°C.
(2) f = 1 MHz, t_r and t_f ≤ 6 ns.

Parameter Measurement Information

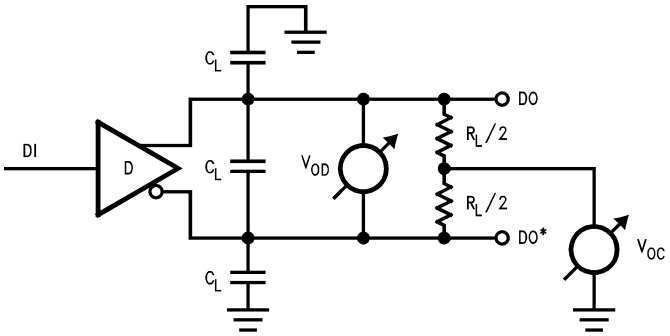
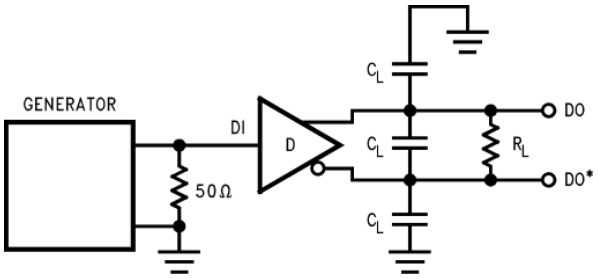


Figure 1. V_{OD} and V_{OC} Test Circuit



f = 1 MHz, tr and tf ≤ 6 ns.

Figure 2. Driver Propagation Delay Test Circuit

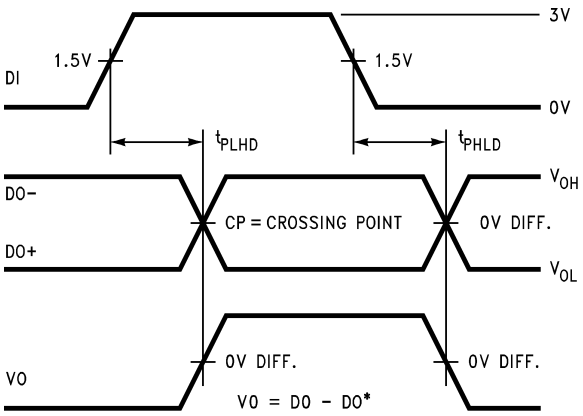


Figure 3. Driver Differential Propagation Delay Timing

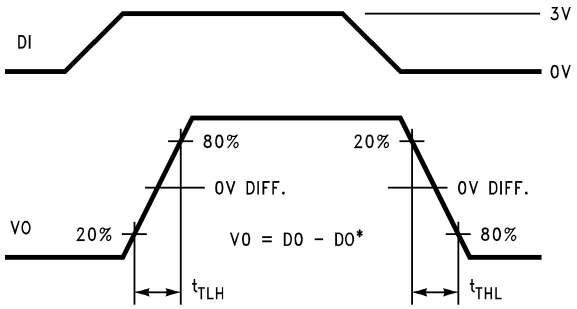
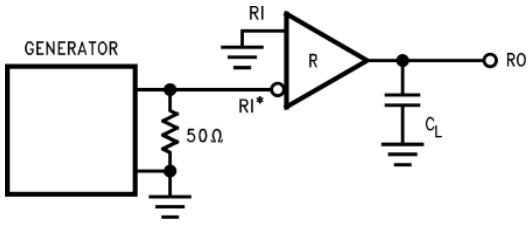


Figure 4. Driver Differential Transition Timing



f = 1 MHz, tr and tf ≤ 6 ns.

Figure 5. Receiver Propagation Delay Test Circuit

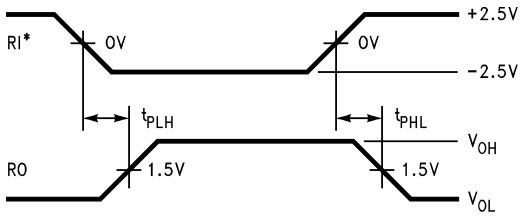


Figure 6. Receiver Propagation Delay Timing

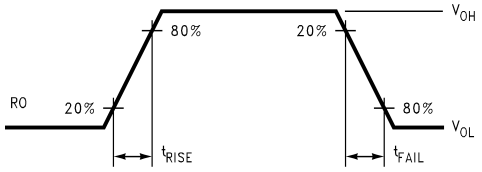


Figure 7. Receiver Rise and Fall Times

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS89C21TM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM
DS89C21TM/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM
DS89C21TMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM
DS89C21TMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS89C 21TM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

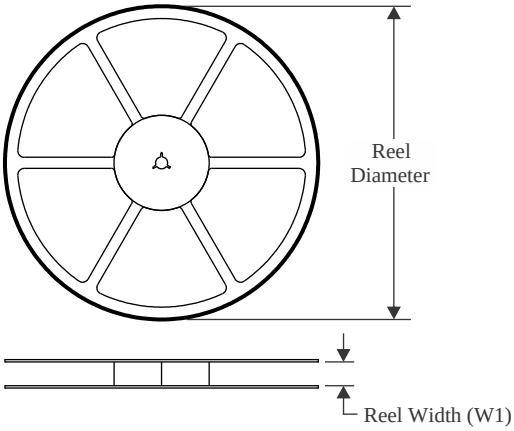
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

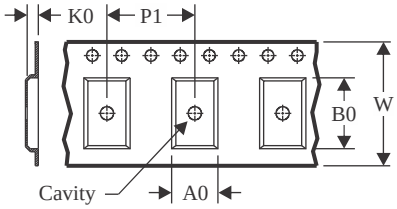
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

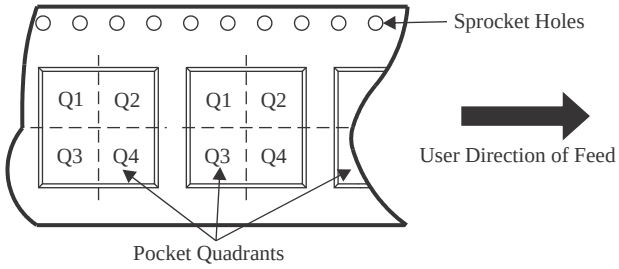


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

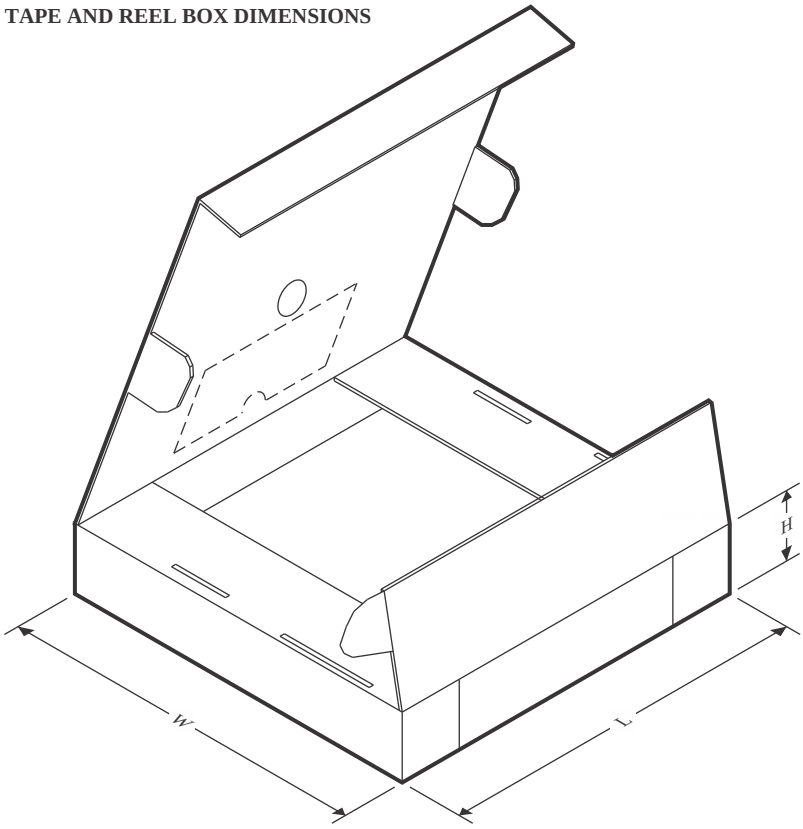
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS89C21TMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

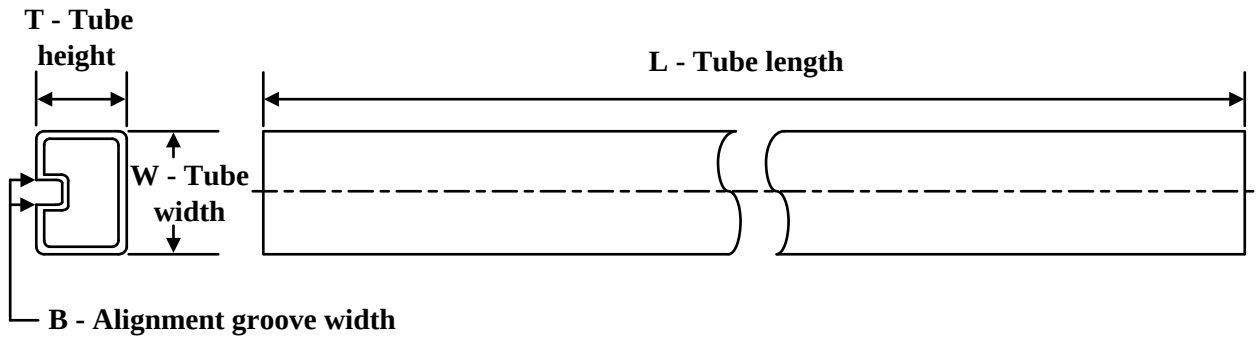
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

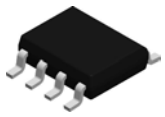
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS89C21TMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS89C21TM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS89C21TM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

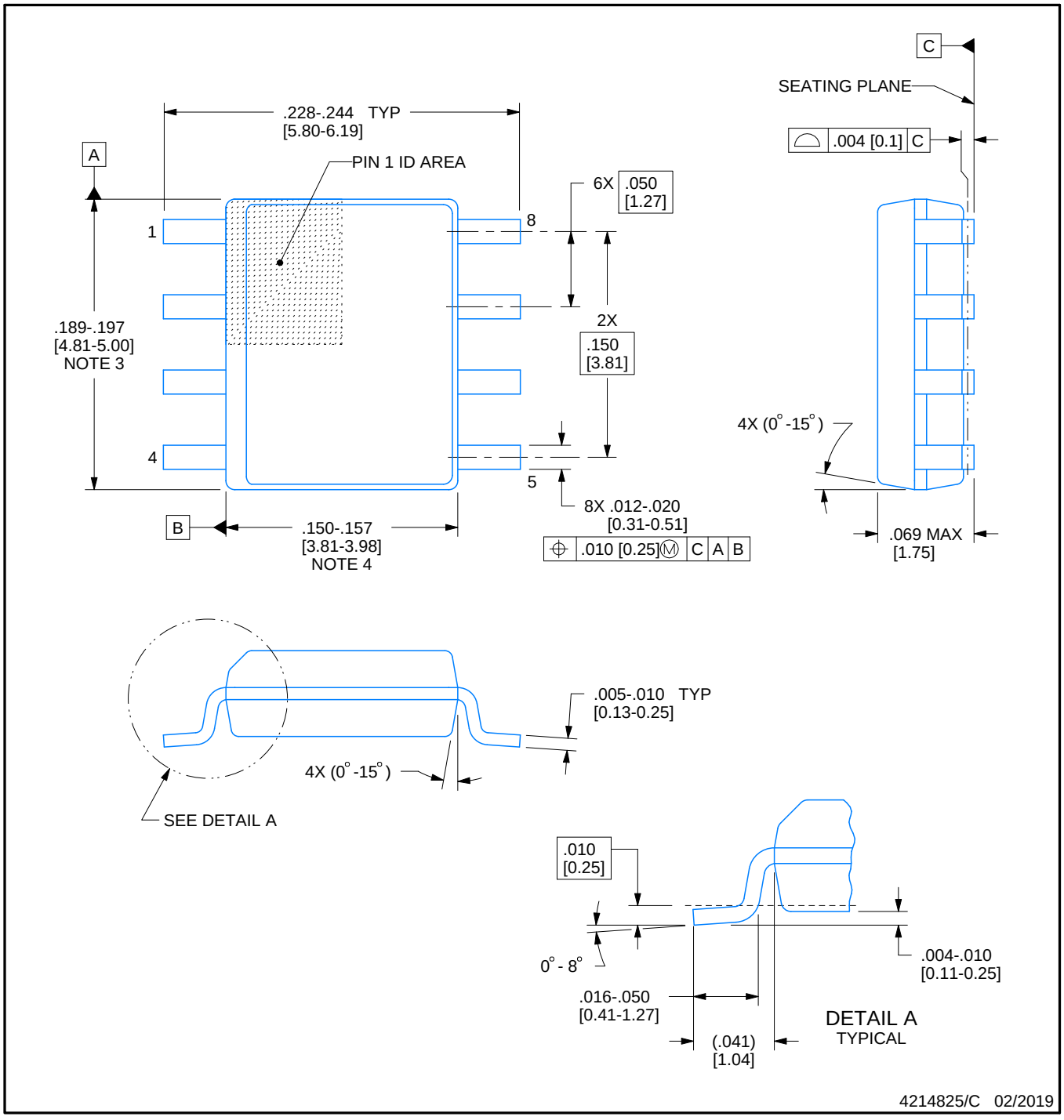


PACKAGE OUTLINE

D0008A

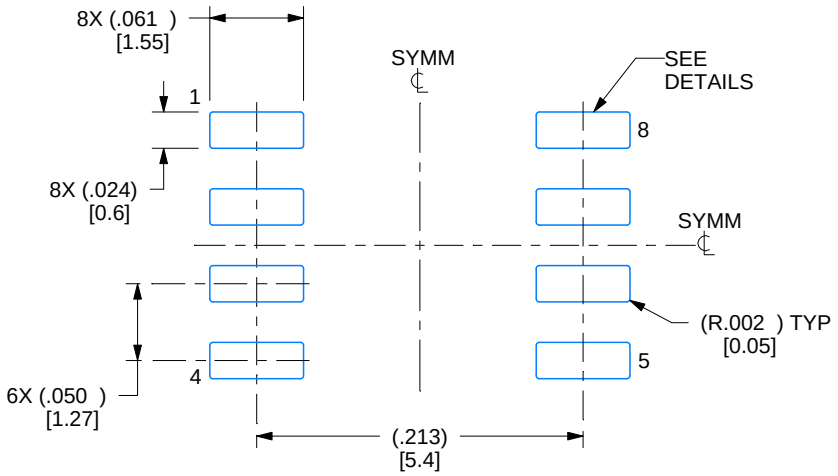
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

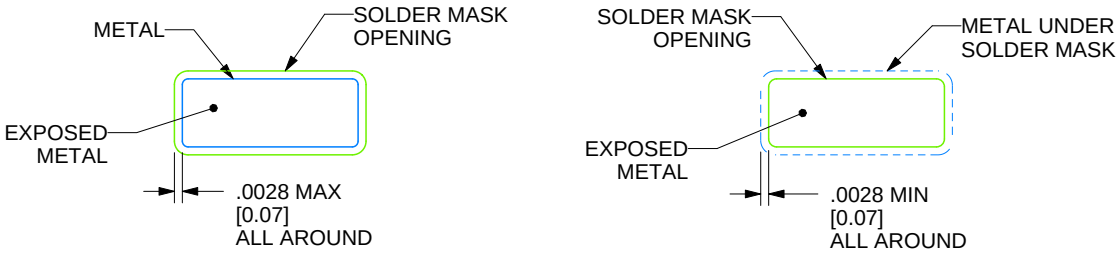


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

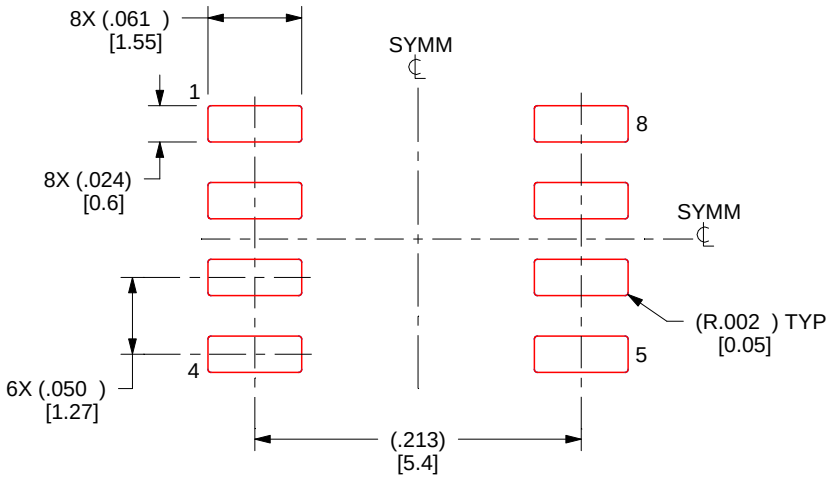
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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