SLUS539C − JUNE 2004 − REVISED OCTOBER 2008

HIGH-EFFICIENCY SECONDARY-SIDE SYNCHRONOUS BUCK PWM CONTROLLER

FEATURES

- **On-Chip Predictive Gate Drive™ for High-Efficiency Synchronous Buck Operation**
- **Dual ±3-A TrueDrive™ Outputs**
- **1-MHz High Frequency Operation with 70-ns Delay from SYNCIN to G1 Output**
- **Leading Edge Modulation**
- **Overcurrent Protection using a Parallel Average Current Mode Control Loop**
- **3 Modes to Support 2.7-V to 35-V Bias Operation**
- **Reverse Current Protection for Output Stage**
- **User Programmable Shutdown**
- **±1.0% Initial Tolerance Bandgap Reference**
- **High Bandwidth Error Amplifiers**
- **Thermally Enhanced HTSSOP 20-Pin PowerPAD™ Package**

APPLICATIONS

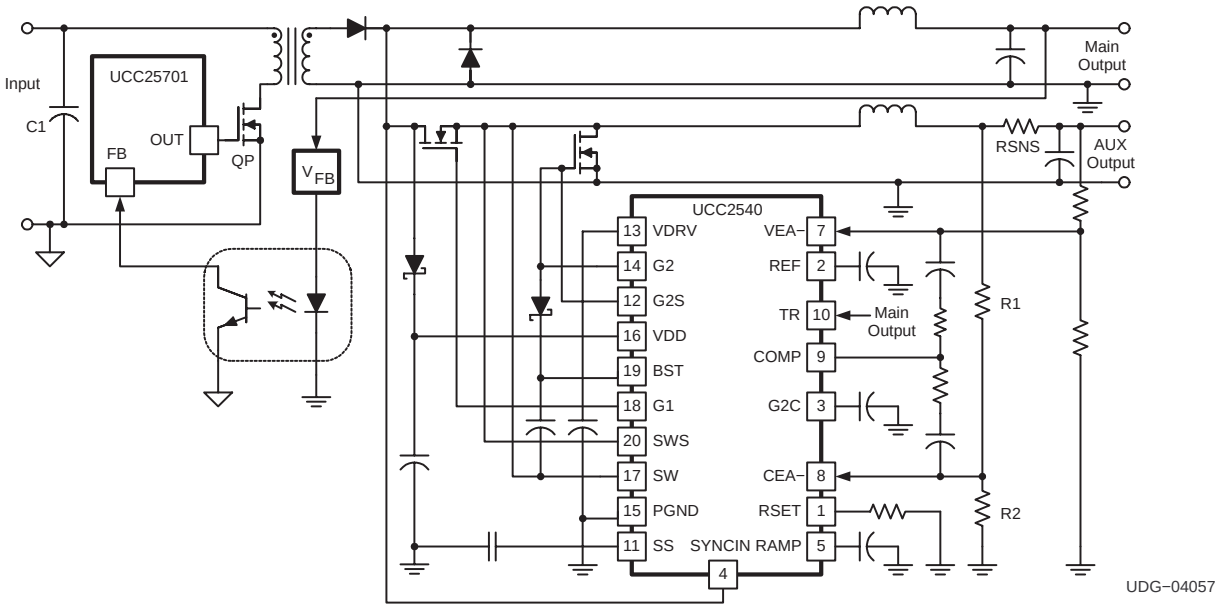
- **Secondary-Side Post Regulation (SSPR) for Multiple Output Power Supplies**
- **Cascaded Buck Converters**
- **Post Processing Converters for Bus Converter and DC Transformer Architectures**

DESCRIPTION

The UCC2540 is a secondary-side synchronous buck PWM controller for high current and low output voltage applications. It can be used either as the local secondary-side controller for isolated dc-to-dc converters using two-stage cascaded topologies or as a secondary-side post regulator (SSPR) for multiple output power supplies.

The UCC2540 runs with the synchronization signal from either the primary side or the high duty cycle quasi-dc output of bus converters or dc transformers. For higher efficiency, it also incorporates the Predictive Gate Drive™ technology that virtually eliminates body diode conduction losses in synchronous rectifiers.

SIMPLIFIED APPLICATION DIAGRAM



Predictive Gate Drive™, TrueDrive™, and PowerPAD™, are a trademarks of Texas Instruments Incorporated.

DESCRIPTION (CONT.)

The UCC2540 is available in the extended temperature range of –40°C to 105°C and is offered in thermally enhanced PowerPAD™ 20-pin HTSSOP (PWP) package. This space saving package with standard 20-pin TSSOP footprint has a drastically lower thermal resistance of 1.4°C/W θ_{JC} to accommodate the dual high-current drivers on board.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		UCC2540	UNIT
Supply voltage range, VDD		36	V
Supply current, I_{VDD}	VDD	50	mA
Analog input voltages	CEA−, COMP, G2C, RAMP, SS, TR, VEA−	−0.3 to 3.6	V
	VDRV	−0.3 to 9	
	G1, BST	SW−0.3 to SW+9	
	SW, SWS	−1 to 36	
	G2, G2S	−1 to 9	
	SYNCIN	−0.3 to 8.0	
Sink current (peak), I_{OUT_SINK}	G1, G2	3.5	A
Source current (peak), I_{OUT_SOURCE}	G1, G2	−3.5	
Operating junction temperature range, T_J		−55 to 150	°C
Storage temperature, T_{stg}		−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, VDD	Mode 1	8.5		35	V
Supply voltage, VDRV	Mode 2	4.75		8.00	
Supply voltage, REF	Mode 3	3.0	3.3	3.6	
Supply voltage bypass, C_{VDD}		1.0	2.2		µF
Reference bypass capacitor, C_{REF}		0.1	1.0	2.2	
VDRV bypass capacitor, C_{VDRV}		0.2			
BST−SW bypass capacitor, C_{BST-SW}		0.1			
Timer current resistor range, R_{RSET}		10		50	kΩ
PWM ramp capacitor range, C_{RAMP}		100		680	pF
Turn-off capacitor range, C_{G2C}		120		1000	
COMP pin load range, R_{LOAD}		6.5			kΩ
Junction operating temperature, T_J		−40		105	°C

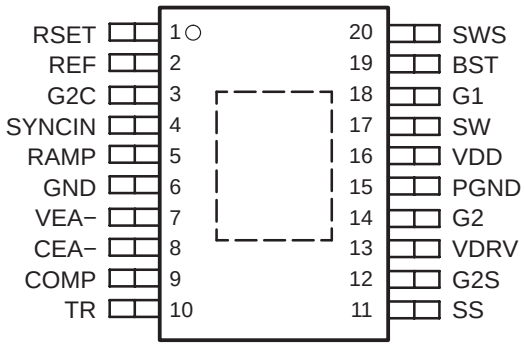
ORDERING INFORMATION

$T_A = T_J$	HTSSOP−20 (PWP)(1)
	Bulk
−40°C to +105°C	UCC2540PWP

(1) The PWP package is also available at 70 devices per tube and taped and reeled at 2,000 devices per reel. Add an R suffix to the device type (i.e., UCC2540PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

CONNECTION DIAGRAM

PWP PACKAGE
(TOP VIEW)



NOTE: The PowerPAD™ is not directly connected to any lead of the package. It is electrically and thermally connected to the substrate of the device which acts as ground and should be connected to PGND on the PCB. The exposed dimension is 1.3 mm x 1.7 mm. However, the tolerances can be +1.05 mm / −0.05 mm (+41 mils / −2 mils) due to position and mold flow variation.

THERMAL INFORMATION

PACKAGE FAMILY	PACKAGE DESIGNATOR	θ_{JA} (°C/W) (with PowerPAD)	θ_{JC} (°C/W) (without PowerPAD)	θ_{JC} (°C/W) (with PowerPAD)	MAXIMUM DIE TEMPERATURE
PowerPAD™ HTSSOP−20	PWP	22.3 to 32.6 (500 to 0 LFM)	19.9	1.4	125°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, f_{SYNCIN} = 200 kHz, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OVERALL							
I_{VDD}	Operating current	DC		8	11	13	mA
		f_S = 200 kHz,	C_{LOAD} = 2.2 nF	9	12	30	
UNDERVOLTAGE LOCKOUT							
V_{VDD}	Start threshold voltage	MODE 1		8.0	8.5	9.0	V
V_{VDD}	Stop threshold voltage	MODE 1		7.5	8.0	8.5	
V_{VDD}	Hysteresis	MODE 1		0.3	0.5	0.8	
V_{VDRV}	Start threshold voltage	MODE 2,	V_{VDD} = 4 V	4.30	4.65	4.85	
V_{VDRV}	Stop threshold voltage	MODE 2		4.0	4.3	4.6	
V_{VDRV}	Hysteresis	MODE 2		0.15	0.35	0.55	
V_{REF}	Start threshold voltage	MODE 3	V_{VDD}= V_{VDRV}= 2.7 V	2.75	3.00	3.20	
V_{REF}	Stop threshold voltage	MODE 3		2.25	2.50	2.70	
V_{REF}	Hysteresis	MODE 3		0.3	0.5	0.8	
VOLTAGE REFERENCE (REF)							
V_{REF}	Reference output voltage	T_A = 25°C		3.28	3.30	3.32	V
		Total variation		3.2	3.3	3.4	
I_{SC}	Short circuit current	V_{REF} = 0 V,	T_A = 25°C	10	13	20	mA
	Line regulation	5.25 V ≤ V_{REF} ≤ 7.2 V		0	1.5	15	mV
	Load regulation	0 mA ≤ I_{REF} ≤ 5 mA		0	30	70	
PWM (RAMP)							
D_{MIN}	Minimum duty cycle					0%	
V_{RAMP}	Offset voltage			0.10	0.25	0.45	V
	Timeout threshold voltage			2.3	2.5	2.8	
t_{DEAD}	G1 deadtime at maximum duty cycle ratio	f_{SYNC} = 200 kHz		150	175	200	ns
I_{RAMP}	Ramp charge current	R_{RSET} = 10 kΩ		−325	−300	−275	µA
CURRENT ERROR AMPLIFIER							
V_{CEA+}	Offset voltage	Total variation		45	50	55	mV
GBW	Gain bandwidth(3)			3	4		MHz
V_{OL}	Low-level output voltage	I_{COMP} = 0 A, V_{VEA-} = 2.0 V	V_{CEA-} = 3.3 V,			0.1	V
		I_{COMP} = 200 µA, V_{VEA-} = 1 V	V_{CEA-} = 1.5 V	0	0.60	0.83	
V_{OH}	High-level output voltage	I_{COMP} = 0 A, V_{VEA-} = 1 V	V_{CEA-} = 0 V,	2.2	2.5	3.0	V
A_{VOL}	Open loop			60	100	140	dB
I_{BIAS}	Bias current			−200	−80	−10	nA
I_{SINK}	Sink current	V_{COMP} = 1.0 V, V_{VEA-} = 0 V	V_{CEA-} = 1.5 V,	0.35	0.80	1.70	mA
CMR	Common mode input range(3)			0		2	V

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, f_{SYNCIN} = 200 kHz, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE ERROR AMPLIFIER						
V_{SS_OFF}	Offset voltage from soft-start input	$I_{COMP} = V_{VEA-}$, V_{SS-} = 1.5 V	0.40	0.75	1.00	V
V_{TR_OFF}	Offset voltage from tracking input	V_{TR} = 1.0 V, $V_{COMP} = V_{VEA-}$	25	48	70	mV
V_{VEA+}	Threshold voltage (from VEA− to COMP)	0°C ≤ T_A ≤ 105°C	1.485	1.500	1.515	V
		Total variation	1.47	1.50	1.53	
GBW	Gain bandwidth(3)		3	4		MHz
V_{OL}	Low-level output voltage	I_{COMP} = 0 A, V_{CEA-} = 1.75 V, V_{VEA-} = 2.0 V,			0.1	V
		I_{COMP} = 200 µA, V_{CEA-} = 0 V, V_{VEA-} = 1 V, V_{TR} = 0 V	0	0.60	0.83	
V_{OH}	High-level output voltage	I_{COMP} = 0 A, V_{CEA-} = 0 V, V_{VEA-} = 1 V	2.2	2.5	3.0	
A_{VOL}	Open loop		60	100	140	dB
I_{BIAS}	Bias current		−300	−150	−50	nA
I_{SINK}	Sink current(4)	V_{COMP} = 1.0 V, V_{CEA-} = 0 V, V_{VEA-} = 1.5 V	0.35	0.80	1.70	mA
CURRENT SET						
I_{OUT}	Output current	R_{RSET} = 10 kΩ	−158	−150	−142	µA
V_{RSET}	R_{SET} voltage	R_{RSET} = 10 kΩ	1.42	1.50	1.58	V
SYNCHRONIZATION AND SHUTDOWN TIMER (SYNCIN, G2C)						
	Timer threshold		2.3	2.5	2.7	V
	SYNCIN threshold		1.50	1.65	1.80	
$I_{CHG(G2C)}$	Shutdown timer charge current	R_{RSET} = 10 kΩ	−325	−300	−275	µA
SOFT-START (SS)						
$I_{CH(SS)}$	Charge current	R_{RSET} = 10 kΩ	−230	−200	−170	µA
$I_{DSCH(SS)}$	Discharge current	R_{RSET} = 10 kΩ	50	70	100	
	Discharge/shutdown threshold		0.35	0.45	0.55	V
DRIVE REGULATOR (VDRV)						
V_{VDRV}	Output voltage	V_{VDD} = 8.5 V	6.87	7.20	7.53	V
	Line regulation	9 V ≤ V_{VDD} ≤ 35 V	0	50	100	mV
	Load regulation	−5 mA ≤ I_{VDRV} ≤ 0 mA	0	50	100	
I_{SC}	Short-circuit current		15	30	50	mA
G2S GATE DRIVE SENSE						
	G2S rising threshold voltage	V_{SWS} = 0 V	1.90	2.25	3.10	V
	G2S falling threshold voltage	V_{SWS} = 0 V	1.00	1.25	1.30	
I_{G2S}	Current	V_{G2S} = 0 V	−0.70	−0.50	−0.37	mA
SWS GATE DRIVE SENSE						
	SWS rising threshold voltage	V_{G2S} = 0 V	1.90	2.25	2.90	V
	SWS falling threshold voltage	V_{G2S} = 0 V	1.0	1.2	1.3	
I_{SWS}	Current	V_{SWS} = 0 V	−1.8	−1.3	−0.9	mA
	Negative threshold voltage		−0.5	−0.3	−0.1	V

(3) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from BST to SW, 1-µF capacitor from REF to GND, 0.1-µF and 2.2-µF capacitors from VDRV to PGND, f_{SYNCIN} = 200 kHz, $T_A = T_J$ = −40°C to 105°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
G1 MAIN OUTPUT								
R_{SINK}	Sink resistance	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 0.5 V	0.3	0.7	1.3	Ω
R_{SRC}	Source resistance	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 5.7 V	10	25	45	Ω
I_{SINK}	Sink current(3)	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 3.0 V		3		A
I_{SRCE}	Source current(3)	V_{SW} = 0 V,	V_{BST} = 6 V,	V_{G1} = 3.0 V		−3		A
t_{RISE}	Rise time	C_{LOAD} = 2.2 nF, from G1 to SW				12	25	ns
t_{FALL}	Fall time	C_{LOAD} = 2.2 nF, from G1 to SW				12	25	ns
G2 SYNCHRONOUS RECTIFIER OUTPUT								
R_{SINK}	Sink resistance	V_{G2} = 0.3 V			5	15	30	Ω
I_{SINK}	Sink current(3)	V_{G2} = 3.25 V				3		A
I_{SRC}	Source current(3)	V_{G2} = 3.25 V				−3		A
t_{RISE}	Rise time	C_{LOAD} = 2.2 nF, from G2 to PGND				12	25	ns
t_{FALL}	Fall time	C_{LOAD} = 2.2 nF, from G2 to PGND				12	25	ns
V_{OH}	High-level output voltage, G2	V_{SW} = GND			6.2	6.7	7.5	V
DEADTIME DELAY (see Figure 1)								
$t_{ON(G1)}$	RAMP rising to G1 rising				90	115	130	ns
$t_{OFF(G1)}$	SYNCIN falling to G1 falling				50	70	90	ns
$t_{ON(G2)}$ $t_{OFF(G2)}$	Delay control resolution				3.5	5.0	6.5	ns
$t_{ON(G2)}$	G2 on-time minimum	wrt G1 falling				−24		ns
$t_{ON(G2)}$	G2 on-time maximum	wrt G1 falling				62		ns
$t_{OFF(G2)}$	G2 off-time minimum	wrt G1 rising				−68		ns
$t_{OFF(G2)}$	G2 off-time maximum	wrt G1 rising				10		ns

(3) Ensured by design. Not production tested.

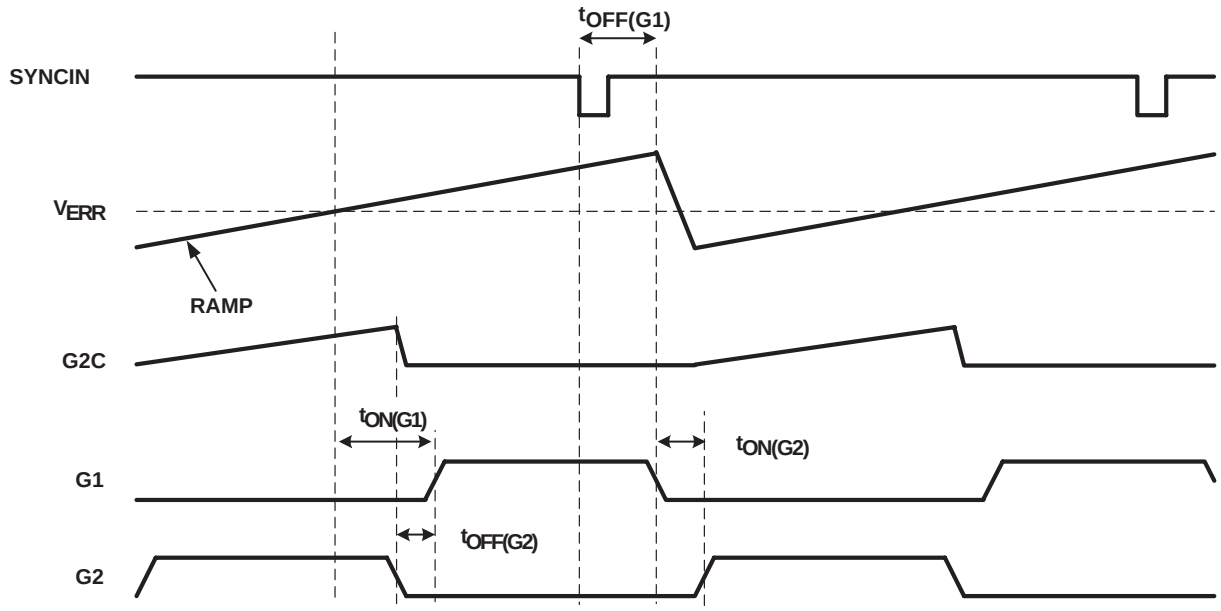
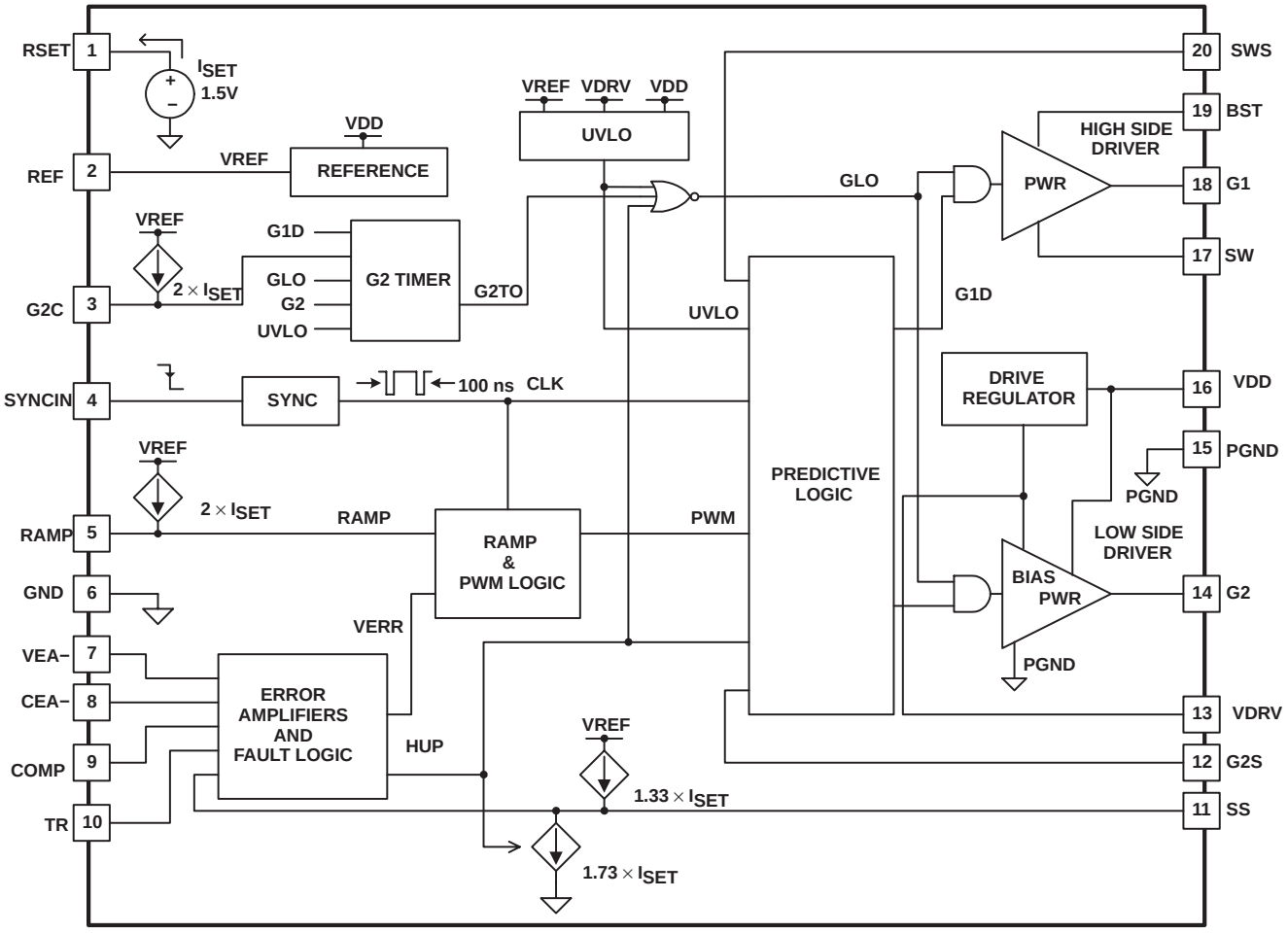


Figure 1. Predictive Gate Drive Timing Diagram

FUNCTIONAL BLOCK DIAGRAM



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PIN ASSIGNMENTS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BST	19	I	Floating G1 driver supply pin. VHI is fed by an external Schottky diode during the SR MOSFET on time. Bypass BST to SW with an external capacitor.
CEA−	8	I	Inverting input of the current error amplifier used for output current regulation.
COMP	9	I	Output of the voltage and current error amplifiers for compensation.
G1	18	O	High-side gate driver output that swings between SW and BST.
G2	14	O	Low-side gate driver output that swings between PGND and VDRV.
G2C	3	I	Timer pin to turn off synchronous rectifier. The capacitor connected to this pin programs the maximum duration that G2 is allowed to stay HIGH.
G2S	12	I	Used by the predictive deadtime controller for sensing the SR MOSFET gate voltage to set the appropriate dead-time.
GND	6	−	Ground for internal circuitry. GND and PGND should be tied to the pc-board ground plane with vias.
PGND	15	−	Ground return for the G2 driver. Connect PGND to the pc-board ground plane with several vias.
RAMP	5	I	Input pin to connect capacitor to GND to generate the PWM ramp and serve as a maximum duty ratio timer.
REF(1)	2	I/O	3.3-V reference pin. All internal circuits are powered from this 3.3-V rail. Bypass this pin with at least 0.1 μF of capacitance for REF loads that are 0 mA to −1 mA. Bypass this pin with at least 1 μF of capacitance if it is used as an input (Mode 3) or if it has large or pulsating loads.
RSET	1	I	Pin to program timer currents for G2C, RAMP, SS charge and SS discharge. This pin generates a current proportional to the value of the external resistor connected from RSET pin to GND. RSET range is 10 kΩ to 50 kΩ (giving a programmable nominal ISET range of 30 μA to 150 μA, respectively).
SS	11	I	Soft start and shutdown pin. Connect a capacitor to GND to set the soft-start time. Add switch to GND for immediate shutdown functionality.
SYNCIN	4	I	Input pin for timing signal.
SW	17	−	G1 driver return connection.
SWS	20	I	Used by the predictive controller to sense SR body-diode conduction. Connect to SR MOSFET drain close to the MOSFET package.
TR	10	I	Tracking input to the voltage error amplifier. Connect to REF when not used.
VDD	16	I	Power supply pin to the device and input to the internal VDRV drive regulator. Normal V_{DD} range is from 4.5 V to 36 V. Bypass the pin with at least 1 μF of capacitance.
VDRV	13	I	Output of the drive regulator and power supply pin for the G2 driver. VDRV is also the supply voltage for the internal logic and control circuitry.
VEA−	7	I	Inverting input of the voltage error amplifier used for output voltage regulation.

(1) REF is an input in Mode 3 only.

APPLICATION INFORMATION

The UCC2540 is a high-efficiency synchronous buck controller that can be used in many point-of-load applications. It can be used as a local controller for cascaded techniques such as post processing converters for isolated integrated bus converters (IBC) and dc transformer architectures. It can also be used as a general purpose secondary-side post regulator for high-accuracy multiple-output power supplies.

Using UCC2540 as the Secondary-Side PWM Controller in the Cascaded Push-Pull Buck Two Stage Converter

The two-stage cascaded push-pull buck topology converts higher-input bus voltage such as 48-V telecom voltage to sub 2-V output voltages.

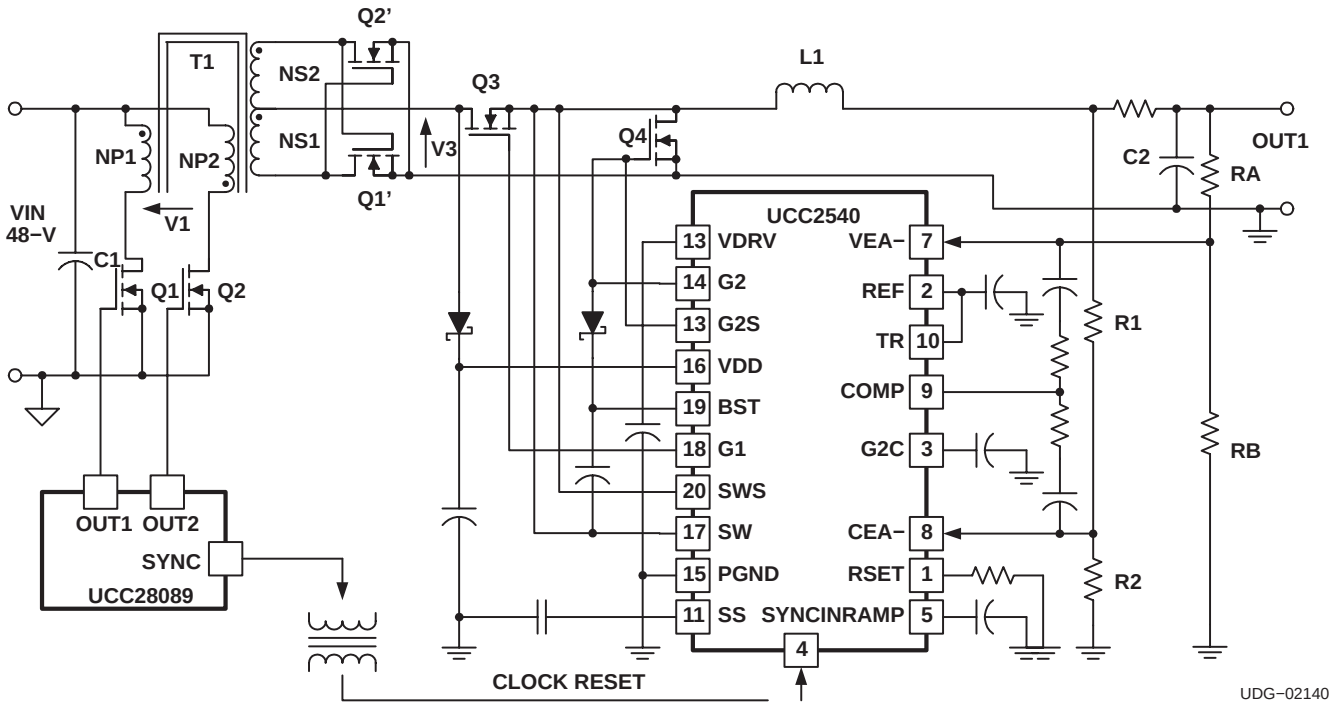

Figure 2. Secondary-Side Controlled Cascaded Push-Pull/Buck Converter

The primary-side power stage is an open loop push-pull converter that provides voltage step-down, and galvanic isolation. This takes the high bus voltage and converts it into an intermediate voltage such as 7 V. The primary-side push-pull gate drive signals can come from either off-the-shelf oscillators or a fully integrated 50% duty dual-output oscillator such as the UCC28089.

The secondary-side power stage is a buck converter that is optimized for low-output voltage regulation. The clock reset pulse signal from the primary side is transmitted using a signal transformer.

APPLICATION INFORMATION

There are many advantages to this secondary-side control circuit. The simple isolated power stage does not require any feedback across the isolation boundary. Since the primary-side oscillator is free running, there is no need for an isolated start-up power supply. This high-frequency circuit provides soft-switching operation (for all six MOSFET switches), optimum transformer core utilization, and minimizes filter requirements because there are no additional high-current inductors.

The push-pull primary side permits simple direct drive control of the input stage MOSFETs. In exchange, it requires that the input MOSFETs are rated to at least twice the peak input line voltage. This configuration works well for 36-V to 72-V input line applications, because there are many suitable power MOSFETs available in the range of 150 V. For applications with larger input voltages, a half bridge or full bridge with alternating modulation might be more suitable for an input stage. Thus, the cascaded topology has a large degree of flexibility with input power stages. The cascaded topology also has flexibility in the output stages, as well.

For additional information on this topology refer to Power Supply Seminar SEM−1300 Topic 1: *Unique Cascaded Power Converter Topology for High Current Low Output Voltage Applications [1].* The topic discusses the operating principles, design trade-offs, and critical design procedure steps.

UCC2540 in Multiple Output Power Supplies

One such flexibility is an ability to easily add independently regulated auxiliary outputs. A multiple output implementation of the cascaded push-pull/buck power converter is shown in Figure 3.

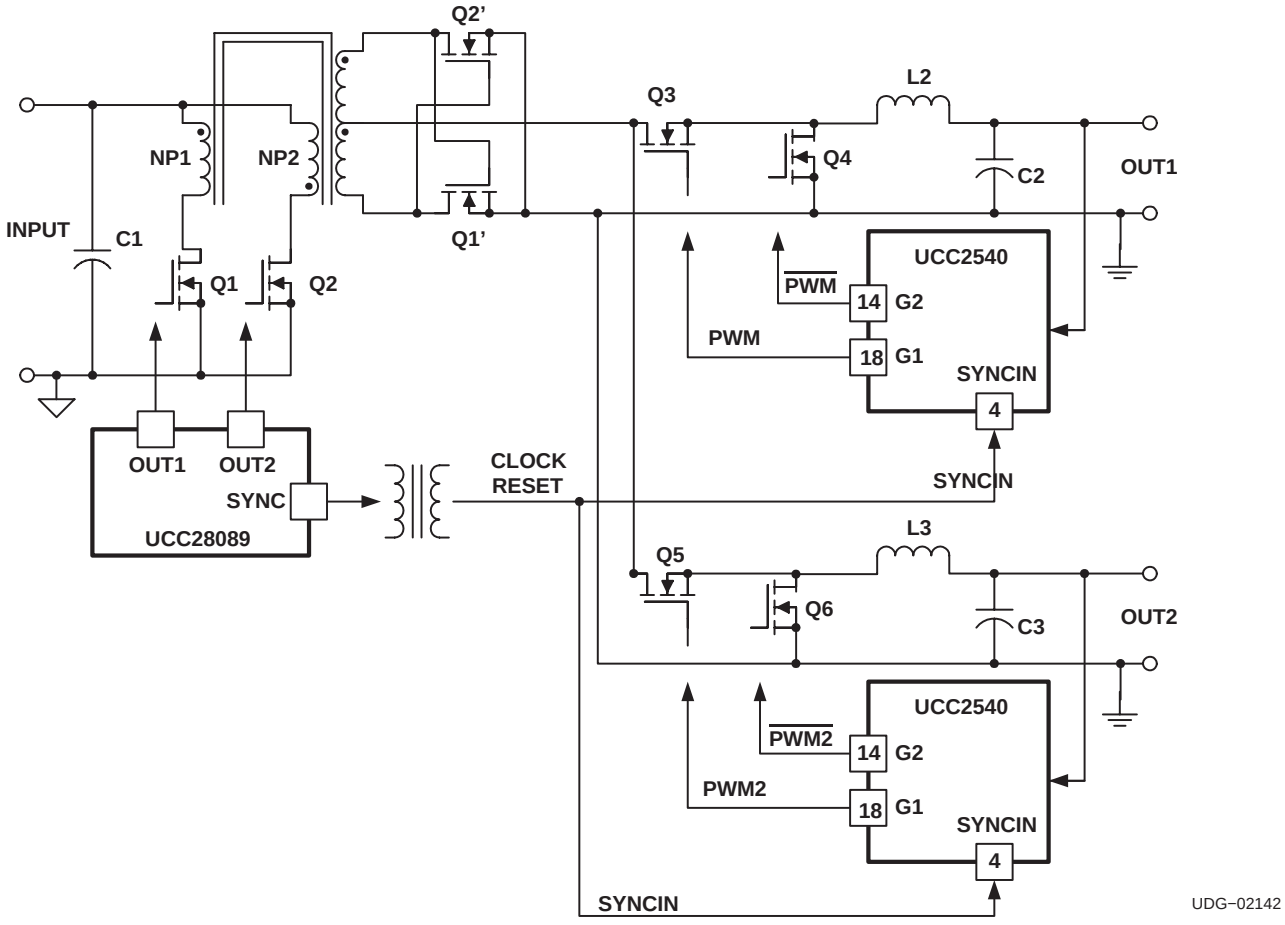

Figure 3. Multiple Output Implementation of Push-Pull/Buck Cascaded Converter

APPLICATION INFORMATION

Using UCC2540 as the Secondary-Side Post Regulator

UCC2540 can also be used as a secondary-side post regulator (SSPR) for precision regulation of the auxiliary voltages of multiple output power supplies, as shown in Figure 4. The UCC2540 uses leading-edge modulation so that it is compatible with either voltage-mode or current-mode primary-side control converters using any topology such as forward, half-bridge or push-pull.

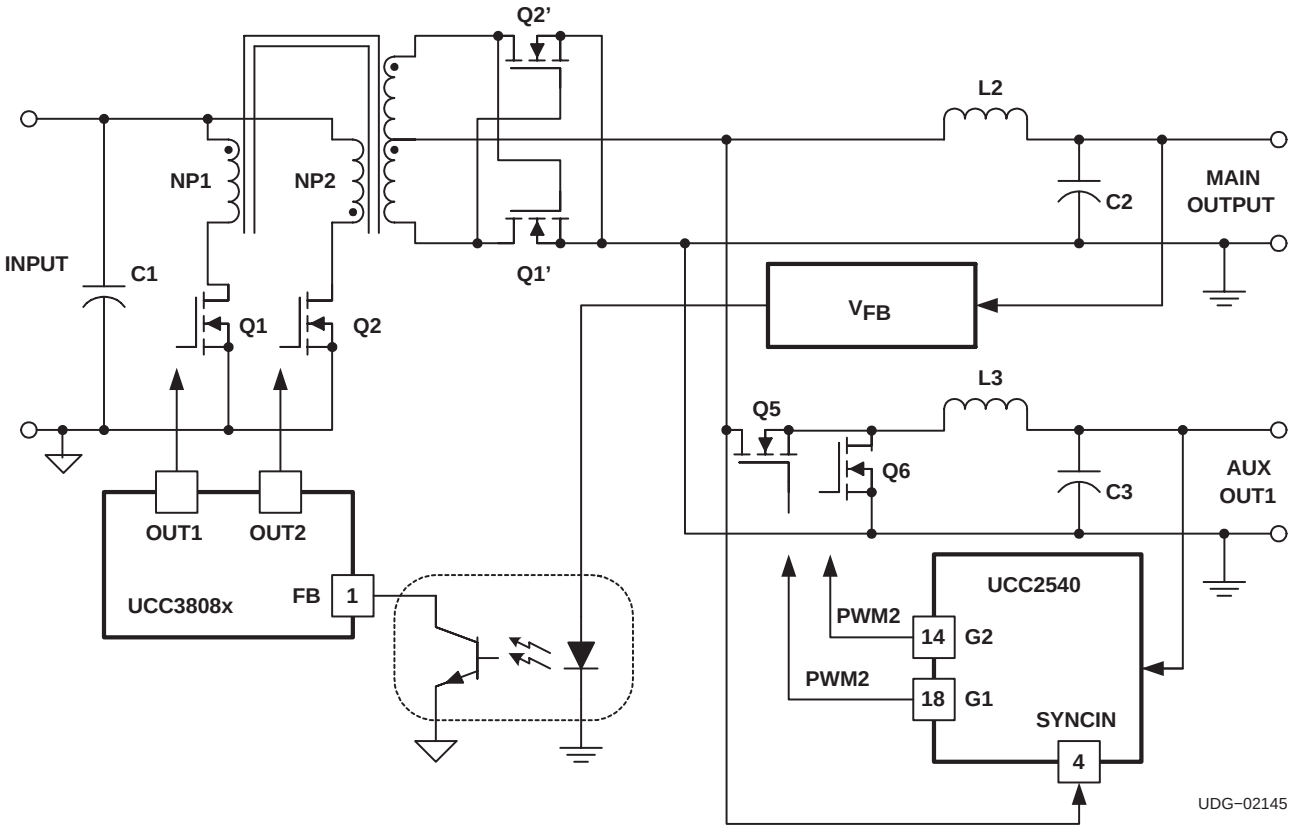

Figure 4. Multiple Output Converter with Primary Side Push−Pull Converter

APPLICATION INFORMATION

CEA− and VEA− pins: Current Limit and Hiccup Mode

Typical power supply load voltage versus load current is shown in Figure 5. This figure shows steady state operation for no-load to overcurrent shutdown (soft-start retry is not depicted in the diagram). During the voltage regulation conditions, the voltage error amplifier output is lower than the current error amplifier, allowing the voltage error amplifier to control operation. During the current limit conditions, the current error amplifier output is lower than the voltage error amplifier, allowing the current error amplifier to control operation. The boundary between voltage and current control occurs when the difference between CEA− and VEA− tries to exceed 50 mV.

Current limiting begins to occur when the difference between CEA− and VEA− exceeds 50 mV. For currents that exceed this operating condition, the UCC2540 controls the converter to operate as a pure current source until the output voltage falls to half of its rated steady state level. Then the UCC2540 sets both G1 and G2 outputs to LOW and it latches a fault that discharges the soft-start voltage at 30% of its charging rate. The UCC2540 inhibits a retry until the soft-start voltage falls below 0.5 V. A functional diagram of the voltage and current error amplifiers is shown in Figure 6.

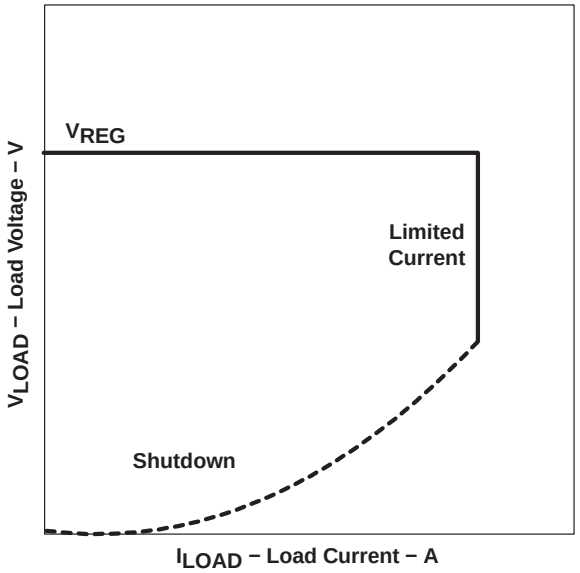

Figure 5. Typical Power Supply Load Voltage vs Current

APPLICATION INFORMATION

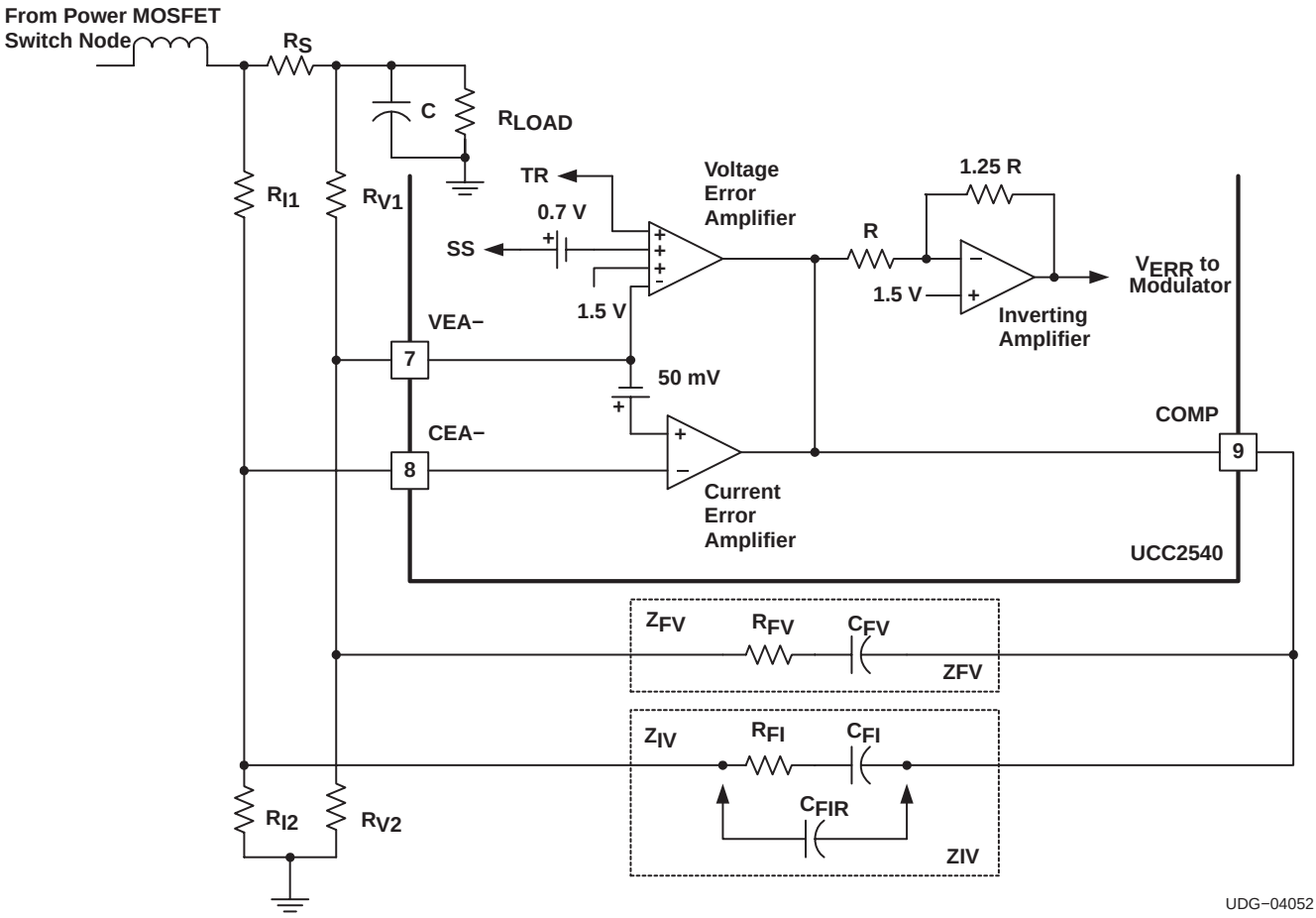

Figure 6. Error Amplifier Configuration

Component selection includes setting the voltage regulation threshold, then the current limit threshold, as described below.

Voltage vs. Current Programming (refer to Figure 6):

1. Determine the ratio $\frac{R_{V1}}{R_{V2}} = \frac{V_{LOAD(reg)}}{V_{VEA-} + \text{Threshold Voltage}} - 1\ V = \frac{V_{LOAD(reg)}}{1.5\ V\ (typ)} - 1\ V$
2. Sense resistor $R_S = \left(1 + \frac{R_{V1}}{R_{V2}}\right) \times \frac{V_{CEA+}\,\text{offset voltage}}{I_{S(max)}}$, where $I_{S(max)}$ is the current limit level, V_{CEA+}offset = 50 mV (typ).
3. Arbitrarily select either R_{V1} or R_{V2} so that the smallest of the two resistors is between 6.5 kΩ and 20 kΩ. Then calculate the value of the other resistor using the equation in the first step.

If the converter is in a current-limit condition and the output voltage falls below half of the regulated output voltage, the UCC2540 enters into a hiccup (restart-retry) mode. Figure 7 shows typical signals during hiccup mode.

APPLICATION INFORMATION

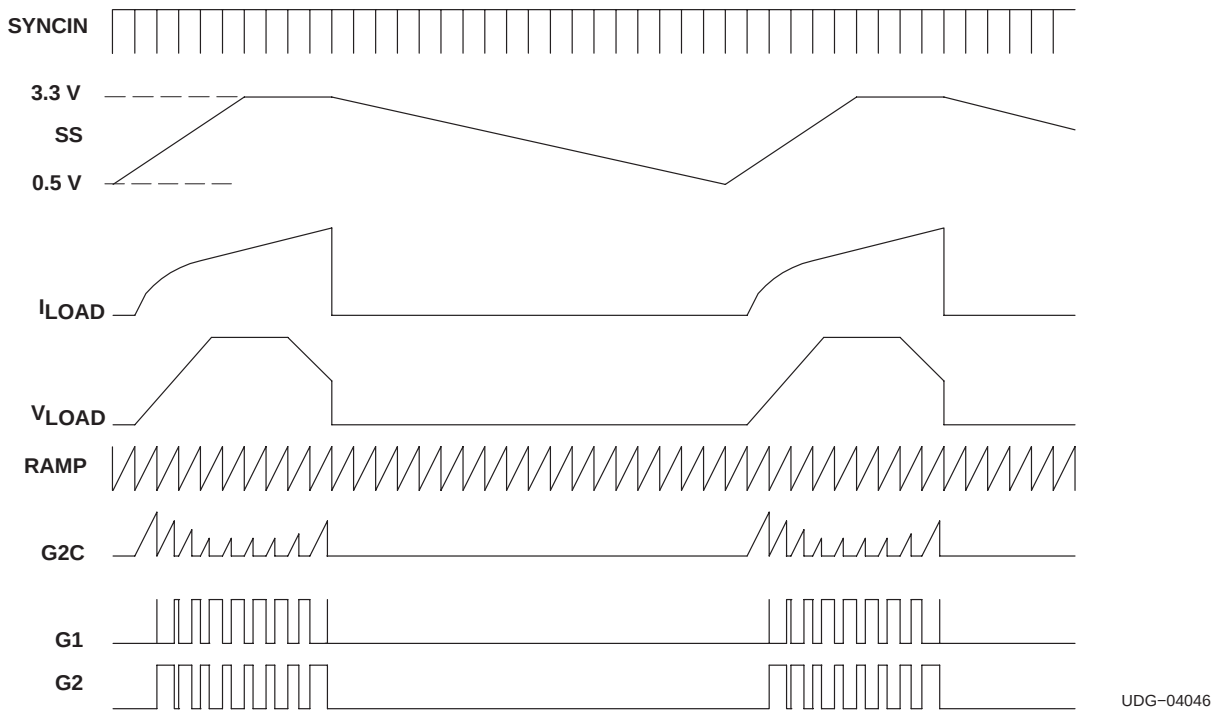

Figure 7. Typical Hiccup Mode waveforms

COMP, VEA− and CEA− pins: Voltage and Current Error Amplifiers

From no-load to full rated load operating conditions, the UCC2540 operates as a voltage mode controller. Above the programmed rated current, there are two levels of over current protection; constant current limit and overcurrent reset/retry. This section gives suggestions on how to design the voltage controller and current controller so that they interact with one another in a stable fashion. Refer to the functional diagram of the voltage and current error amplifiers in Figure 6. The voltage error amplifier in the figure shows three non-inverting inputs. The lowest of the three non-inverting inputs (1.5 V, SS and TR) is summed with the non-inverting input to achieve the voltage error signal. The lowest of the two outputs drives the inverting stage which in turn, drives the modulator.

During steady state voltage control operation, the feedback elements in the current loop have no effect on the loop stability. When current limit occurs, the voltage error amplifier effectively shuts OFF and the current error amplifier takes control. During steady state current limit operation, the negative feedback elements in the voltage error amplifier loop become positive feedback elements in the current error amplifier loop. In order for the current error amplifier to be stable, the impedances in the feedback path of the current error amplifier must be lower than the impedances in the feedback path of the voltage error amplifier. This means that resistors in the current error amplifier negative feedback path must be less than the resistors in the voltage error amplifier negative feedback path. Also capacitors in the current error amplifier negative feedback path must be larger than capacitors in the negative feedback path of the voltage error amplifier negative feedback path. (Capacitance is really an admittance value rather than an impedance value). This concept is illustrated in Figure 6.

In order for the current loop to be stable in Figure 6, $||Z_{IV}||$ must be less than $||Z_{FV}||$ over all frequencies. This can be achieved if $R_{FI} < R_{FV}$ and $C_{FI} > C_{FV}$.

APPLICATION INFORMATION

Another issue that can occur during current limit operation is modulator stability. In order for the modulator to be stable, the rising slope of the current ripple measured at the COMP pin must be smaller than the rising slope that is measured at the RAMP pin. This can be met either in the selection of the ratio of $||Z_{IV}||$ to $||Z_{FV}||$, or by the addition of a capacitor in parallel to R_{FI} and C_{FI}, such as C_{FIR}, in Figure 6.

Stable Dynamic Current Loop Design (refer to Figure 6):

1. Using any favorite approach, design the voltage error amplifier for stable voltage mode design. Use at least 15 kΩ for any resistors in the negative feedback path of the voltage error amplifier (between pins 9 and 7). This does not apply to resistance values between the power supply output voltage and pin 7; it also does not apply to resistance values between ground and pin 7.
2. The goal is to design the current limit control loop so that it drives the converter to maintain 50 mV between the VEA− pin and the CEA− pin during current-limit conditions. Select the current sense element and the voltage divider ratios for the VEA− pin to ground and the CEA− pin to ground to provide the desired current limit level.
3. Place the same configuration of components in the negative feedback path of the current error amplifier (between pins 9 and 8), that are in the negative feedback path of the voltage error amplifier (between pins 9 and 7). However, use resistors with values that are 67% of the corresponding resistors that are between pins 9 and 7 and use capacitors that are 150% of the corresponding capacitors that are between pin 9 and pin 7.
4. Check the COMP signal. If it is unstable, place a capacitor (or increase the capacitance) between pins 9 and 8 in order to attenuate the current ripple. Raise the value of the capacitor until the COMP pin voltage becomes stable. Compare the COMP voltage with the RAMP voltage. With stable operation, the rising slope of the COMP voltage ripple is less than the rising slope of the RAMP pin.

APPLICATION INFORMATION

RSET, RAMP, G2C, SS pins: Programming the Timer Currents

Set the base current to the timers with a resistor between RSET and GND. The block diagram of the UCC2540 shows the interaction of the RSET pin and the dependent current sources for the RAMP, G2C and SS features. The RSET pin is a voltage source; the current of the RSET pin is reflected and multiplied by a gain and distributed to the RAMP (gain = 2), G2C (gain = 2) and SS (charge gain = 1.33, net discharge gain = 0.4). The resistance applied to the RSET pin and GND should be in the range of 10 kΩ < R_{RSET} < 50 kΩ. RAMP, G2C and SS timers are programmed by the selection of capacitors tied between each of their respective pins and GND.

G2C pin: G2 Timer

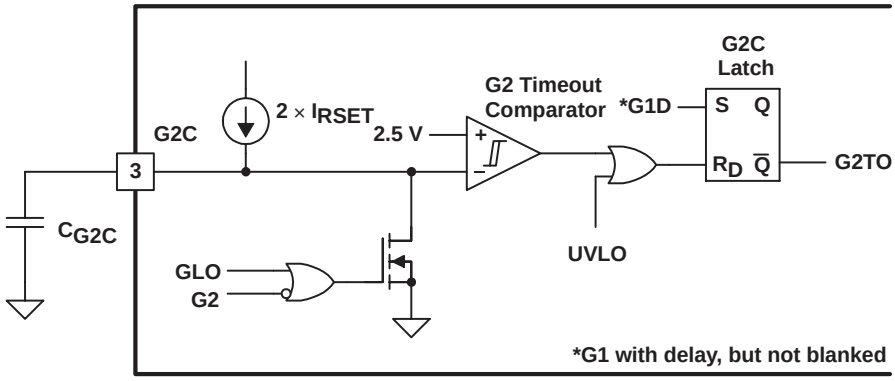

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Figure 8. Functional diagram of the G2 Timer

The G2C pin programs the maximum duration of the synchronous rectifier to facilitate low or zero duty ratio operation. FIgure 8 shows the functional diagram. This function is programmed by connecting a capacitor between the G2C pin and GND. The capacitor on G2C should be slightly larger than the capacitor on the RAMP pin. For best results, program the typical G2 time limit to be between 1.5 and 3 times the switching period (T). Notice that when the G2 timer reaches its limit, both G1 and G2 are forced to a LOW output. This feature prevents the current in the output inductor from excessive negative excursions during zero-duty ratio conditions. Program the G2 time-out (G2TO) duration using equation (1):

$$C_{G2C} = \frac{2 \times V_{RSET}}{R_{RSET}} \times \frac{\text{G2 Timeout Duration}}{\text{G2C Timer Threshold}}, \text{ Farads} \quad (1)$$

where

- V_{RSET} = 1.5 V(typ)
- 1.5 T < G2 Timeout Duration < $3T_S$
- G2C Timer Threshold = 2.5 V (typ)

APPLICATION INFORMATION

RAMP pin: PWM Modulator and G1 Timer

The RAMP pin serves two purposes: (1) programming the gain of the PWM modulator and (2) programming the time-out duration of G1 in case the main power stage has not caused a SYNC pulse to occur. A diagram of the PWM modulator and G1 timer is shown in Figure 9. The UCC2540 has a leading edge modulator that compares the error output with the RAMP voltage. The modulator frequency is externally driven through the SYNCIN pin. The RAMP pin provides both a sawtooth wave for the PWM comparator and it functions as G1 time-out protection that is programmed by R_{SET} and the value of the RAMP capacitor.

A switching cycle begins with the falling edge of the SYNCIN signal, which must be LOW for at least 50 nanoseconds. The falling edge of SYNCIN generates a 100 ns discharge strobe (CLK), to the RAMP function and then, allows the RAMP capacitor to charge from the $2 \times I_{RSET}$ current source.

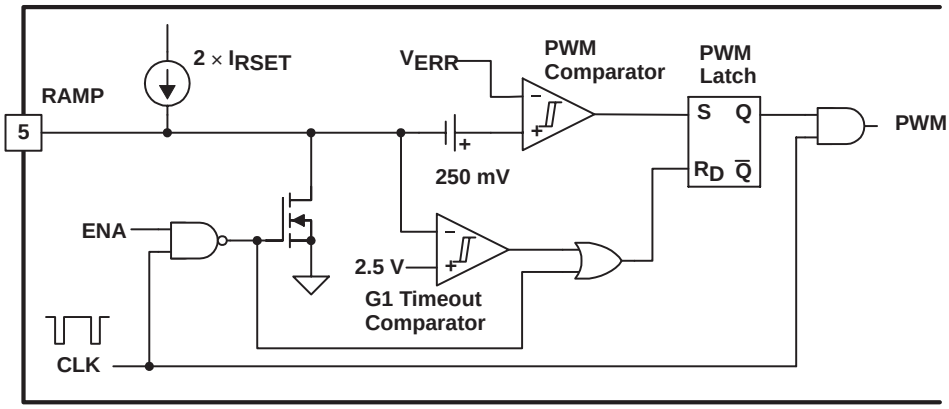


Figure 9. PWM Modulator and G1 Time-Out Comparator

Low-line or brownout conditions can cause the primary side duty ratio to approach 100% where parasitic converter impedances may temporarily impair the quality of the SYNCIN pulse. The RAMP timing function terminates the G1 pulse when the RAMP voltage exceeds 2.5 V. The duration of the RAMP timing function should be set as follows:

$$C_{RAMP} \geq \frac{\left(2 \times \frac{V_{RSET}}{R_{RSET}}\right) \times T_S}{PWM_{RAMP} \text{ timeout threshold voltage}} \quad (2)$$

where

- T_S = switching period
- V_{RSET} = 1.5 (typ)
- $PWM_{(RAMP)}$ = 2.5 V (typ)

$$R_{SET}C_{RAMP} \geq \frac{1.2}{f_S} \Rightarrow \text{Gain (PWM modulator)} \geq 0.4 \quad (3)$$

In order to use the G1 Timer feature, the peak RAMP voltage at the end of a switch cycle should be as close to 2.5 V as the C_{RAMP} and R_{RSET} tolerances allow. In other words, the PWM modulator gain should be programmed to be equal to, or slightly greater than 0.4 inverse-V.

APPLICATION INFORMATION

SYNCIN pin

A falling edge applied to the SYNCIN pin generates a narrow pulse that is the base timer for internal UCC2540 functions. The SYNCIN pulse must be HI for at least 100 ns preceding the falling edge and LOW for at least 50 ns in order to be registered as a valid pulse. Due to the critical nature of the timing, avoid filtering the falling edge of the SYNCIN signal in order to avoid signal delay. The peak SYNCIN voltage can easily range from between 2.5 V and 6.6 V, which allows a simple resistive divider to scale the secondary transformer voltage in post regulator applications.

Situations where the line voltage varies more extensively or there is extensive ringing may call for clamping and/or additional gain.

Ground Clamping

In applications where a ring or a spike causes SYNCIN to fall below GND, protect the pin with a Schottky diode (cathode = SYNCIN, anode = GND).

Overvoltage Clamping

The SYNCIN signal may require overvoltage clamping in applications where the peak SYNCIN voltage is perilously close to the absolute maximum level of 8 V, due to either ringing or voltage levels. The REF or VDRV can be used as clamp voltages, as in Figure 10. Make sure that REF or VDRV always sources current. The reason is that both REF and VDRV are used to detect the mode of operation when they are back-driven and they could latch into the wrong operating mode at start-up.

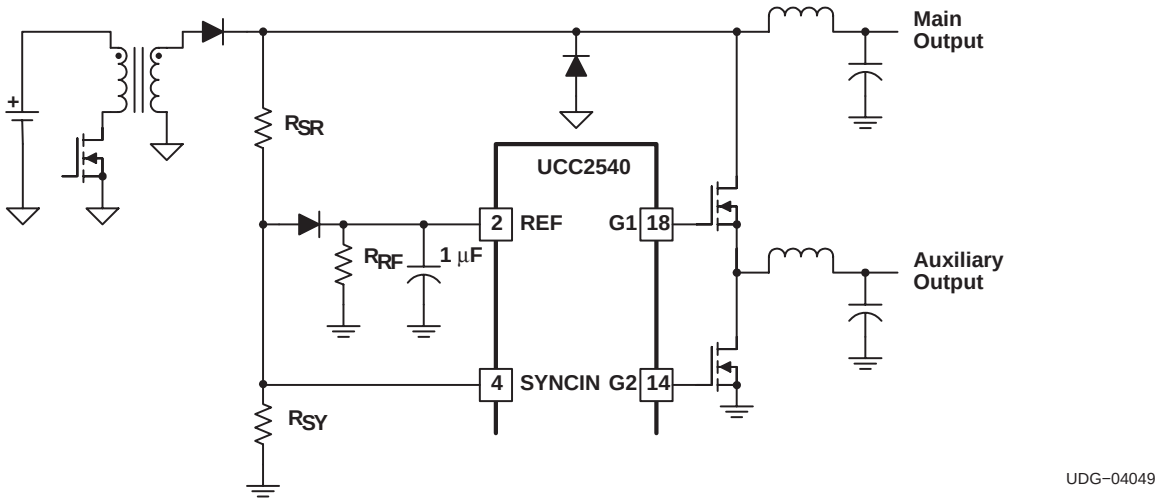


Figure 10. REF Clamp for SYNCIN. Note the REF Load Resistor.

APPLICATION INFORMATION

Another overvoltage clamping option is to directly clamp the SYNCIN pin. Unfortunately, Zener diodes have excessive junction capacitance which causes too much delay in the signal. However, a base-emitter clamp that achieves the desired clamping action can be employed with minimal delay to the SYNCIN signal. See Figure 11. Simply select R_{SR} and (R_{CB} + R_{BE}) to give the appropriate 0 V to 3.3 V signal at low-line conditions. Then, select the ratio of R_{CB} to R_{BE} to cause the transistor to turn-on when SYNCIN exceeds 4 V.

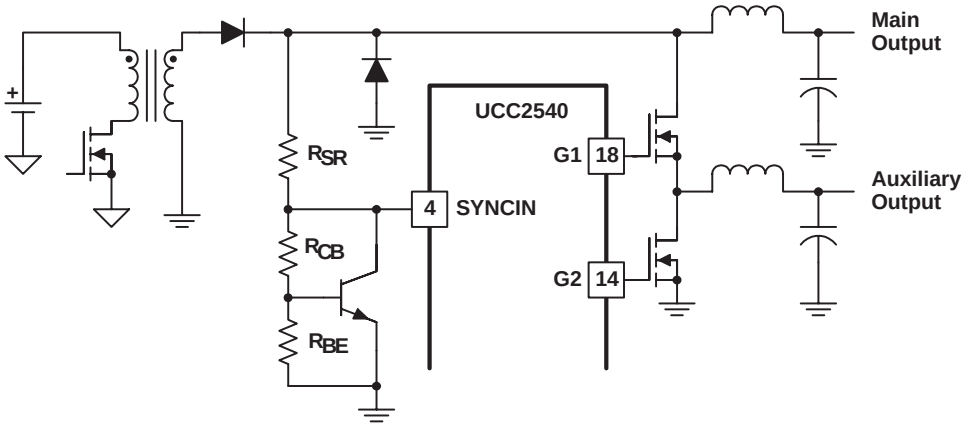


Figure 11. VBE Clamp for SYNCIN

SYNCIN Clamping for the Isolated Cascaded Buck Topology

The UCC2540 is ideally suited as a secondary side controller for the cascaded buck topology, when it is partnered with the UCC28089 primary side start-up controller. The primary side controller transmits a pulse edge during its dead time. The UCC2540 uses the primary-side pulse in order to provide zero voltage conditions for primary- and secondary-side switches. The predictive delay feature tunes the secondary-side transition to minimize reverse recovery losses in the synchronous rectifier. The pulse-edge information can vary with the primary side bias voltage and therefore, it must be clamped. The circuit shown in Figure 12 includes the appropriate pulse-edge shaping circuit, clamping and 1500-V isolation. The recommended transformer, COEV part # MGBBT−00011−01, is smaller than many opto-isolators.

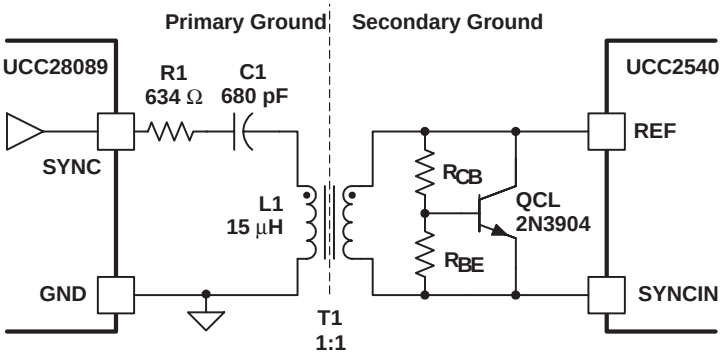


Figure 12. Isolation and Clamping the SYNCIN Signal for Cascaded Buck Converters

APPLICATION INFORMATION

VDD, VDRV, VREF and BST pins: Modes of Operation

Depending on the available bias voltage for the UCC2540, the startup, shutdown, and restart conditions are different. There are three distinct configurations or modes of biasing the UCC2540. The mode is detected and latched into an internal register during power-up when VREF crosses 2 V. The register is cleared when VDD, VDRV and VREF are simultaneously less than 1 V. All modes are compatible with either cascaded buck or with secondary-side post regulator (SSPR) topologies. The main bias voltage of Modes 1 and 2 can be implemented with a diode and a capacitor from an ac-voltage such as the secondary winding of the transformer. A summary of the modes and their programming requirements are listed in Table 1.

Table 1. Modes and Programming Requirements

Mode	V_{BIAS} Range (V)	Bias Pin	UVLO ON (V)	UVLO OFF (V)	Mode Requirement at Power-Up and V_{VREF} = 2 V	Remarks
1	8.5 to 36	VDD [16]	V_{VDD} = 8.5	V_{VDD} = 8.0	$V_{VDD} > (V_{VDRV}$ and $V_{REF})$	Widest line operation
2	4.75 to 8.5	VDRV [13]	V_{VDRV} = 4.65	V_{VDRV} = 4.3	$V_{VDRV} > (V_{VDD}$ and $V_{REF})$	
3	3.0 to 3.6	VREF [2]	V_{REF} = 3.0	V_{REF}= 2.5	$V_{REF} > (V_{VDD}$ and $V_{VDRV})$	Needs regulated bias and low V_{TH} power MOSFETs

- Mode 1, or normal operation requires the availability of a bias of 8.5 V or higher for the device. Here, the bias drives the VDD pin. The low-side drive bias, V_{VDRV} = 7 V, is generated from an internal linear regulator and it directly draws current from the VDD pin. The high-side driver bias is a flying capacitor that is charged from the VDRV pin through the G2 pin, when G2 is HI, via a diode between G2 and BST. The UCC2540 operates in Mode 1 if $V_{VDD} > (V_{VDRV}$ and $V_{VREF})$ when V_{VREF} rises above 2 V. Mode 1 permits the widest range of bias voltages, operational from 8.5 V < V_{VDD} < 35 V. This mode is compatible with systems that have a 12 V_{DC} bias supply already available. Alternatively, Mode 1 is particularly useful for applications where the input line voltage varies over a wide range and the bias is to be derived directly from the reflected line voltage, such as in Fig. 13.
- Mode 2 is suitable for applications where the bias is typically 5 V (between 4.5 V and 8.0 V). The bias voltage is applied to the VDRV terminal of the UCC2540. The high-side driver bias is a flying capacitor that is charged from the VDRV pin through the G2 pin, when G2 is HI. Bias voltage to the VDD pin is obtained through an external voltage-doubler charge pump. If the system uses low threshold voltage power MOSFETs, VDD can be directly tied to the VDRV pin. The bias voltage could be either a bus converter output or an auxiliary supply, or the reflected converter input voltage that originates from a regulated source.
- Mode 3 is for synchronous buck converter applications where the bias voltage is a regulated 3.3-V source. This is a common main output voltage in multiple output power converters. The bias voltage is applied to the VREF pin of the UCC2540. The UCC2540 operates in Mode 3 if it detects ($V_{VREF} > V_{VDRV}$ and VDD) when V_{VREF} rises above 2 V.

Assorted combinations of modes and biasing schemes are shown in Figure 13 through Figure 18. In Mode 1 and Mode 2, the bias voltage can either be an independent auxiliary supply or it can be generated by rectifying and filtering the reflected line voltage, as shown in Figure 13 through Figure 16. A regulated auxiliary supply must be used with Mode 3 because the tolerance of the VREF voltage is the control tolerance of the UCC2540. In Mode 3, the regulated auxiliary supply can be independent of the power supply input voltage (as shown in Figure 18) or, the regulated auxiliary supply can be the same source as the power supply input voltage.

APPLICATION INFORMATION

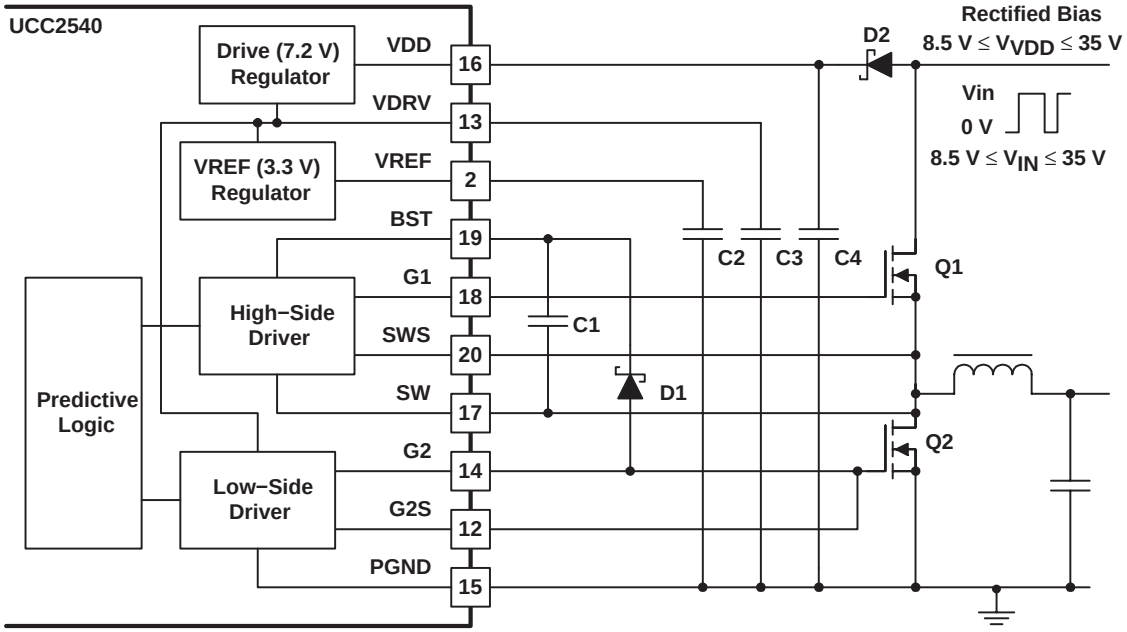


Figure 13. Mode 1 With Rectified Biasing for Input Voltages Between 8.5 V and 35 V

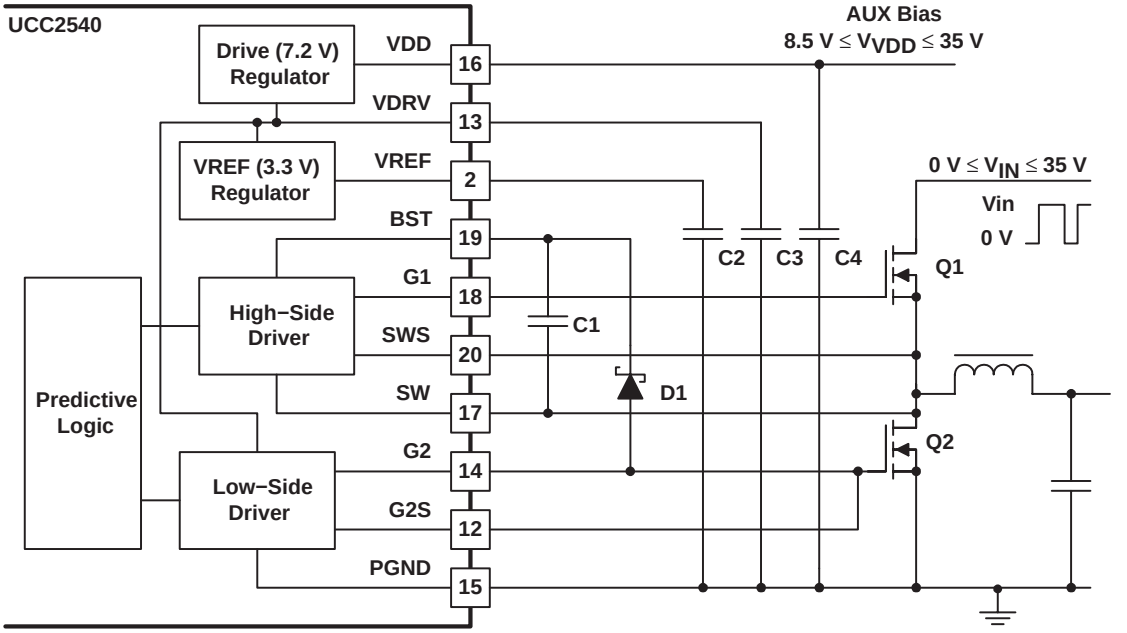


Figure 14. Mode 1 With Auxiliary Biasing for Bias Voltages Between 8.5 V and 35 V

APPLICATION INFORMATION

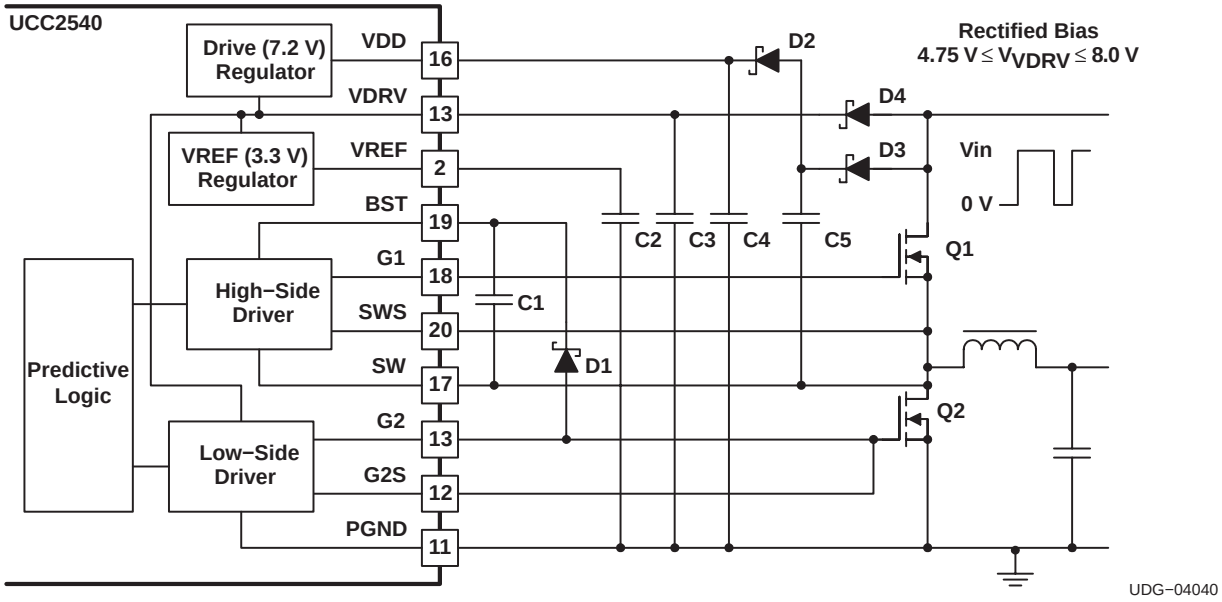


Figure 15. Mode 2 With Rectified Biasing for Input Voltages Between 4.75 V and 8.0 V

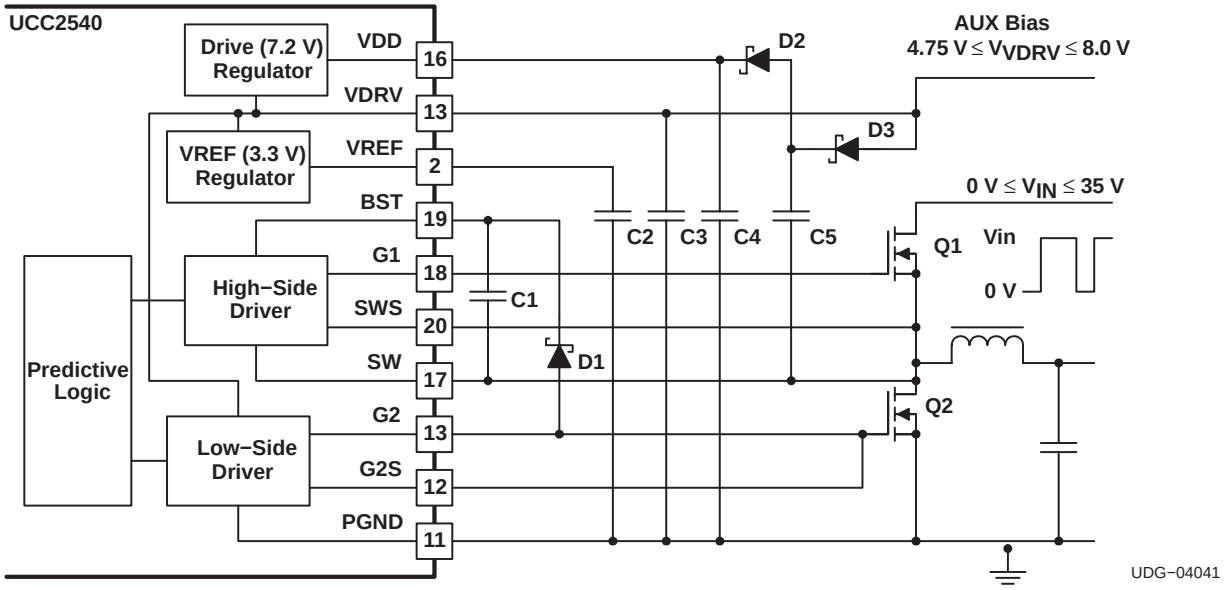


Figure 16. Mode 2 With Auxiliary Biasing for Bias Voltages Between 4.75 V and 8.0 V

APPLICATION INFORMATION

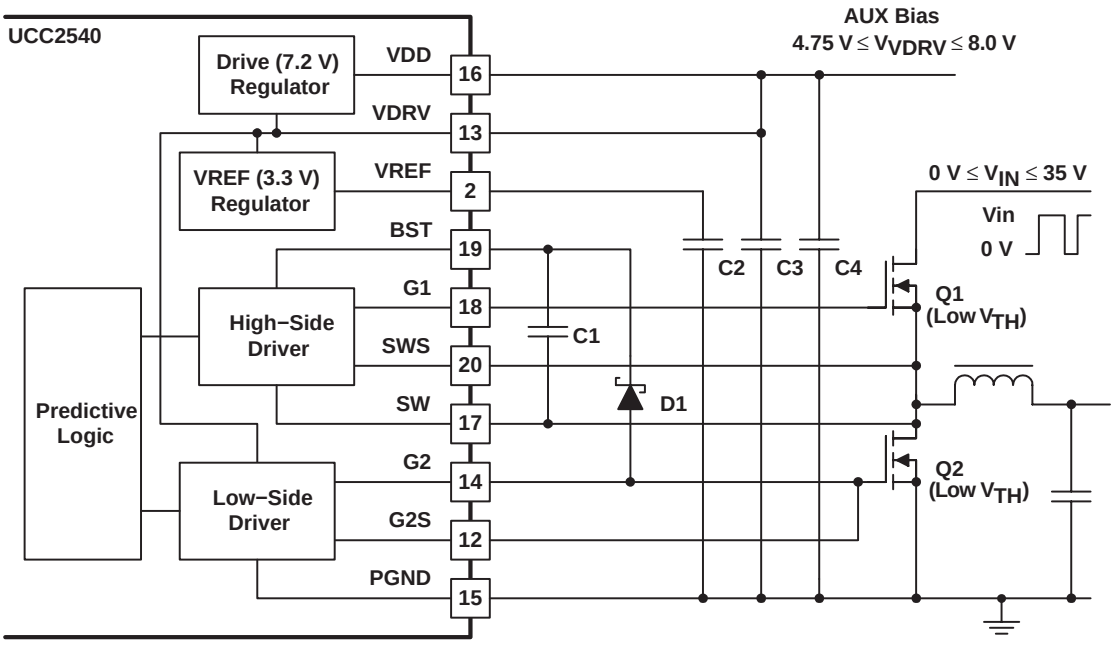


Figure 17. Mode 2 With Auxiliary Biasing for Bias Voltages Between 4.75 V and 8.0 V and Low Threshold Power MOSFET Transistors

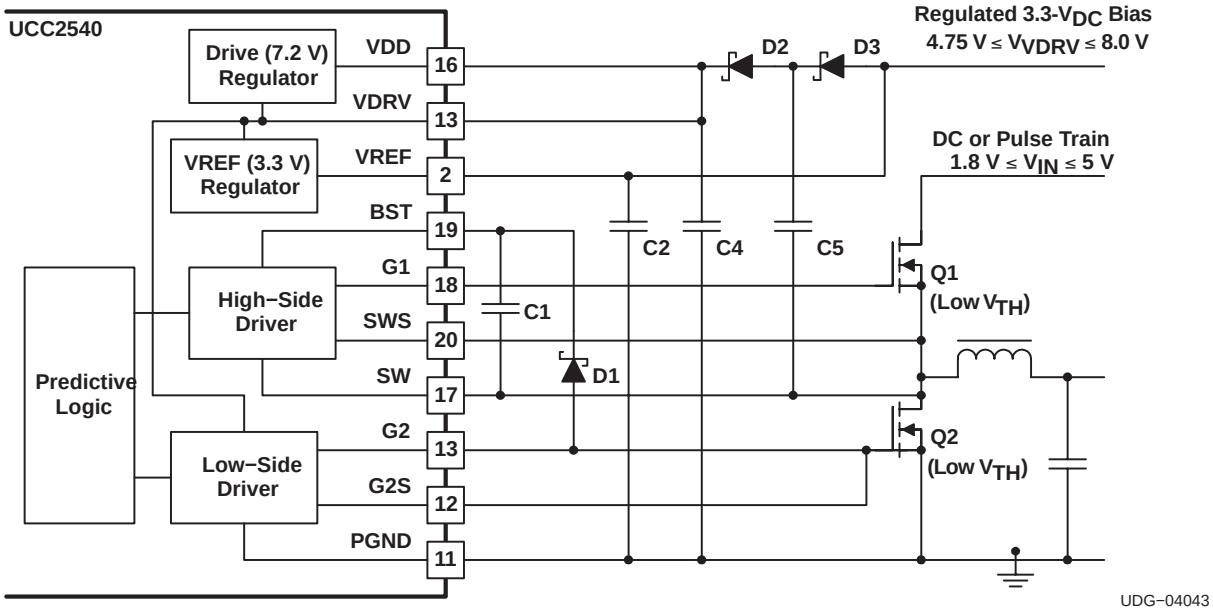


Figure 18. Mode 3 With Regulated 3.3-V_{DC} Bias

APPLICATION INFORMATION

Charge Pump Capacitor Selection

Capacitors C1 through C5 are all part of a charge distribution network that allows the UCC2540 to pass charge to the MOSFET gates of Q1 and Q2 (all reference designators in this section refer to the schematics in Figure 13 through Figure 18). This section gives guidelines on selecting the values of C1 through C5 so that the converter functions properly. Specific capacitor values may need to be larger than the recommended value due to MOSFET characteristics, diode D1 – D4 characteristics and closed-loop converter performance. All three modes of operation require a charge pump capacitor and diode, C1 and D1, in order to drive the high-side power MOSFET. Modes 2 and 3 require additional charge pump capacitors and diodes in order to supply voltage to VDD. In general, all charge pump diodes should be Schottky diodes in order to have low forward voltage and high speed. The charge pump capacitors should be ceramic capacitors with low effective series resistance (ESR), such as X5R or X7R capacitors.

The value of the charge pump capacitor C1 depends on the power MOSFET gate charge and capacitance, the voltage level of the Miller plateau threshold, the forward drop of D1 and the closed-loop response time. The unloaded high-side gate driver typically draws 2 nC of charge per rising edge plus 30 μA of direct current from C1. Usually, the unloaded high−side gate driver load is miniscule compared to the gate charge requirements of the high-side power MOSFET, Q1. Typical values for C1 are approximately 50 to 100 times the input capacitance (C_{ISS}) of MOSFET Q1. This usually allows for transient operation at extremely large duty ratio, where C1 does not have sufficient time to fully recharge. If C1 is excessively large, its ESR and ESL prevents it from recharging during transients, including the start-up transient.

Capacitors C2 through C5 are then selected based on the direction of charge transfer and the requirements of the UCC2540. Selection guidelines are shown in Table 2. Keep in mind that each converter design may require adjustments for larger capacitor ratios than those that are suggested in Table 2. The selection process begins at the left side of Table 2 and progresses towards the right side of the table, which is the reverse order of the charge flow during the first few cycles of start-up. If iteration is required in the design process, review the progression of the capacitors in the order from left to right that is shown in the table.

Table 2. Charge Pump and Bias Capacitor Selection Guidelines

Mode	High-Side Drive Capacitor (≥ 0.1 μF)	VDRV Filter Capacitor	VREF Filter Capacitor	VDD Filter Capacitor	VDD Charging Capacitor
1	C1 ≥ 50 C_{ISS}	C3 ≥ 2 × C1	C2 ≥ 0.1 μF	C4 ≥ 1 μF	n/a
2	C1 ≥ 50 C_{ISS}	C3 ≥ 2 × C1	C2 ≥ 0.1 μF	C4 ≥ 1 μF, 2 × C3	C5 ≥ 2 × C4
3	C1 ≥ 50 C_{ISS}	C4 ≥ 1 μF 2 × C1	C2 ≥ 1.0 μF	C4 ≥ 1 μF, 2 × C1	C5 ≥ 2 × C4

For Modes 2 and 3, the VDD filter capacitor, C4, in Table 2 must supply the I_{VDD} idle current to the UCC2540 (approximately 11 mA) plus the charge to drive the gates G1 and G2. Capacitor C4 must be large enough to sustain adequate operating voltages during start-ups and other transients under the full operational I_{VDD} current. Knowing the operating frequency and the MOSFET gate charges (Q_G), the average I_{VDD} current can be estimated as:

$$I_{VDD} = I_{VDD(idle)} + \left(Q_{G1} + Q_{G2}\right) \times f_S \quad (4)$$

- where f_S is switching frequency

In order to prevent noise problems, C4 must be at least 1 μF. Furthermore, it needs to be large enough to pass charge along to the power MOSFET gates. Thus C4 often needs to have at least twice the capacitance of the VDRV filter capacitor, as shown in Table 2.

APPLICATION INFORMATION

Output Stage

The UCC2540 includes dual gate drive outputs and each is capable of ±3-A peak current. The pull-up/ pull-down circuits of the driver are bipolar and MOSFET transistors in parallel. High-side and low-side dual drivers provide a true 3-A high-current capability at the MOSFET's Miller Plateau switching region where it is most needed. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

The output drivers can switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external-schottky-clamp diodes are not required. The outputs are also designed to withstand 500-mA reverse current without either damage to the device or logic upset.

For additional information on drive current requirements at MOSFET's Miller plateau region, refer to the Power Supply Seminar SEM−1400[2] and the UCC37323/4/5 datasheet[3].

Predictive Gate Drive™ Technology

The Predictive Gate Drive™ technology maximizes efficiency by minimizing body diode conduction. It utilizes a digital feedback system to detect body diode conduction, and adjusts the deadtime delays to minimize the conduction time interval. This closed loop system virtually eliminates body diode conduction while adjusting for different MOSFETs, temperature, and load dependent delays. Since the power dissipation is minimized, a higher switching frequency can be utilized, allowing for a smaller component size. Precise gate timing at the nanosecond level reduces the reverse recovery time of the synchronous rectifier MOSFET body diode, which reduces reverse recovery losses seen in the main (high-side) MOSFET. Finally, the lower power dissipation results in increased reliability.

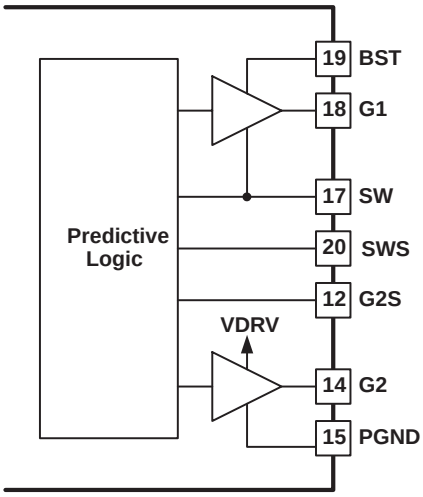


Figure 19.

For additional information on Predictive Gate Drive™ control and efficiency comparisons to earlier adaptive delay and adaptive control techniques, refer to the UCC27223 datasheet [3].

APPLICATION INFORMATION

VDD and IDD

Although quiescent VDD current is low, total supply current is higher, depending on output gate drive requirements and the programmed oscillator frequency. Total VDD current (I_{VDD}) is the sum of quiescent VDD current and the average output currents of G1 and G2, as described in equation (3). Knowing the operating frequency and the MOSFET gate charge (Q_G), average driver output current, per gate, can be calculated from:

$$I_G = Q_G \times f_S \quad (5)$$

where

- f_S is switching frequency

To prevent noise problems, connect a 1-µF ceramic capacitor between the VDD and GND pins. Place the 1-µF ceramic capacitor as close to the UCC2540 as possible. This capacitor is in addition to any electrolytic energy storage capacitors that may be used in the bias supply design.

Soft-Start and Tracking Features

Separate pins are provided for the soft-start feature and the tracking feature. Soft-start or tracking (sequencing) can be easily implemented with this configuration using a minimum number of external components. During a power-up transient, the converter output tracks the lower of the SS voltage, the TR voltage or a 1.5-V internal reference, provided the system is not in current limit. In other words, the voltage control loop is closed during power-up, provided the system is not current limited. Figure 20 shows the UCC2540 configured for soft-start operation. For applications that do not use the tracking feature, connect the TR pin to either SS or REF, as shown in the figure. Remote shutdown and sequential power-up can be easily implemented as a transistor switch across C_{SS}.

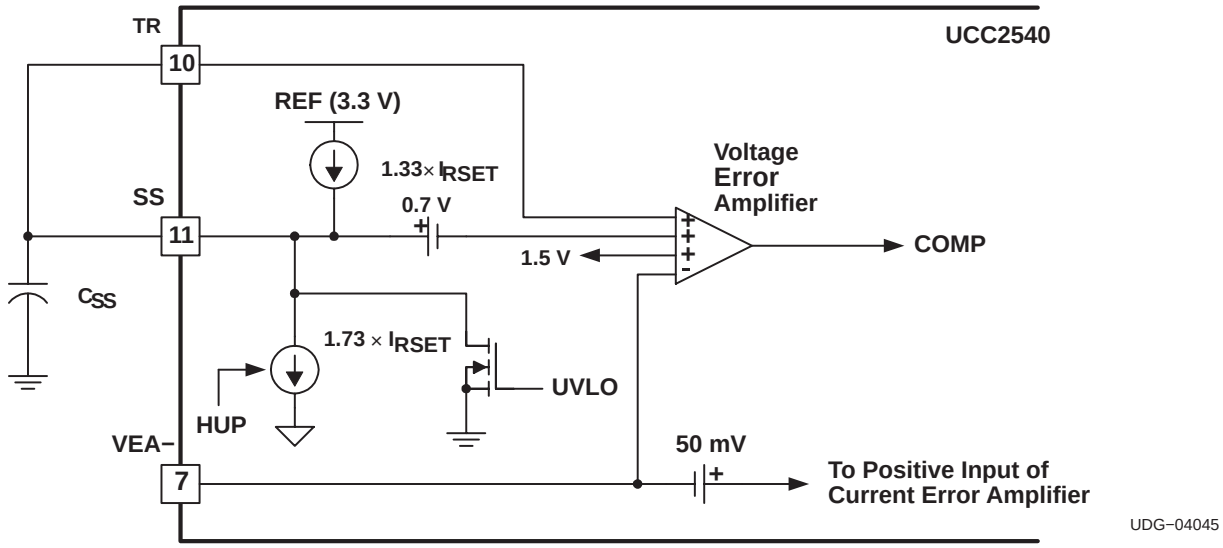


Figure 20. Using the Soft-Start Feature

APPLICATION INFORMATION

The soft-start interval begins when the UCC2540 recognizes that the appropriate voltage (see Mode 1, 2 or 3) is above the UVLO level. The voltage of C_{SS} then linearly increases until it is clamped at the REF voltage of 3.3V. Regulation should be reached when the soft-start voltage reaches about 2.2 V (1.5 V plus a diode drop). Select a C_{SS} capacitor value using equation (5) to program a desired soft-start duration, Δt_{SS}.

$$C_{SS} = 1.33 \times \frac{V_{RSET}}{R_{SET}} \times \frac{\Delta t_{SS}}{\Delta V_{SS}} = 1.33 \times \frac{1.5\ V}{R_{SET}} \times \frac{\Delta t_{SS}}{2.2\ V}\ \text{Farads} \quad (6)$$

If a UVLO fault is encountered, both outputs of the UCC2540 are disabled and the soft-start pin (SS) is discharged to GND. The UCC2540 does not retry until the UVLO fault is cleared.

Using the TR pin, the UCC2540 can be programmed to track another converter output voltage. If the voltage to be tracked is between 0 V and 3.3 V, simply connect the TR pin to the voltage to be tracked with a resistor that is approximately equal to the DC impedance that is connected to the VEA− terminal ($R_{V1} \parallel R_{V2}$, in Figure 6). If the voltage is above that range, use a voltage divider, again with an equivalent resistance that approximately equals the DC impedance that is connected to the VEA− terminal. Other strategies can be used to achieve sequential, ratiometric or simultaneous power supply tracking[14].

An implementation of sequential sequencing of a multiple output power supply[5] is shown in Figure 21. Applications where the loads include a processor with a core voltage of 1.5 V and I/O ports that require 3.3 V can require sequential sequencing in order to resolve system level bus contention problems during start-up. In this circumstance the core must power-up first, then after an initialization period of 130 ms, the ports are allowed to power-up.

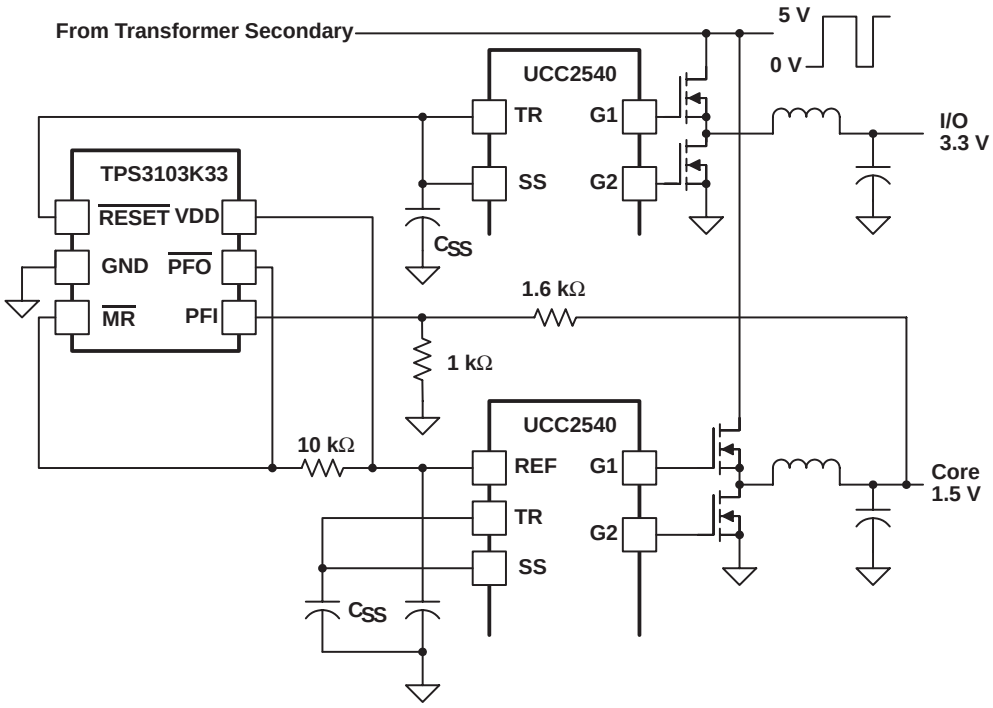


Figure 21. Sequencing a Multiple Output Post Regulated Power Supply

APPLICATION INFORMATION

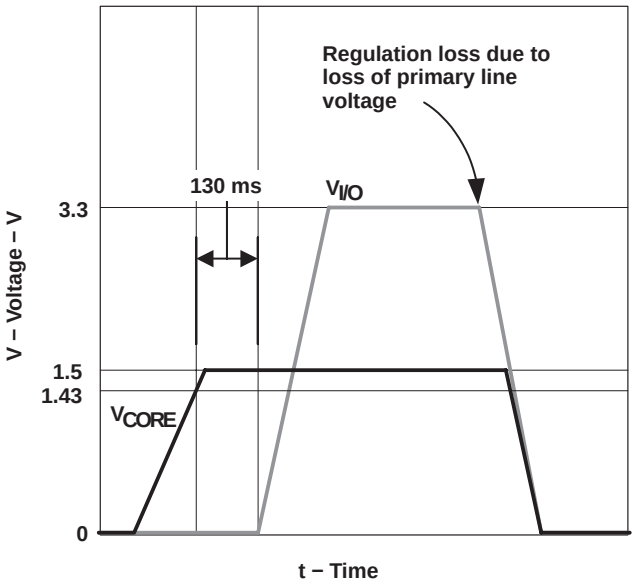


Figure 22.

Using the TR pin, the UCC2540 can be programmed to ratio-metrically track another converter output voltage[5]. Ratio-metric tracking is when the ratio of the output voltages is constant from zero volts to the point where one or more of the outputs lock into regulation. The TR pin is easier to use for tracking than the SS pin because the external currents that would be applied to the SS pin may interfere with SS discharge currents and fault recovery. It should be understood that the voltage that is being tracked must lag the bias voltages (VDD, VDRV and REF) on start-up and lead the bias voltages during shutdown. Furthermore, the output that is being tracked must not reach its steady state DC level before the output that is tracking reaches its steady state DC level. Figure 23 illustrates the concept of programming an output voltage V_C, to ratio-metrically track another output, V_M.

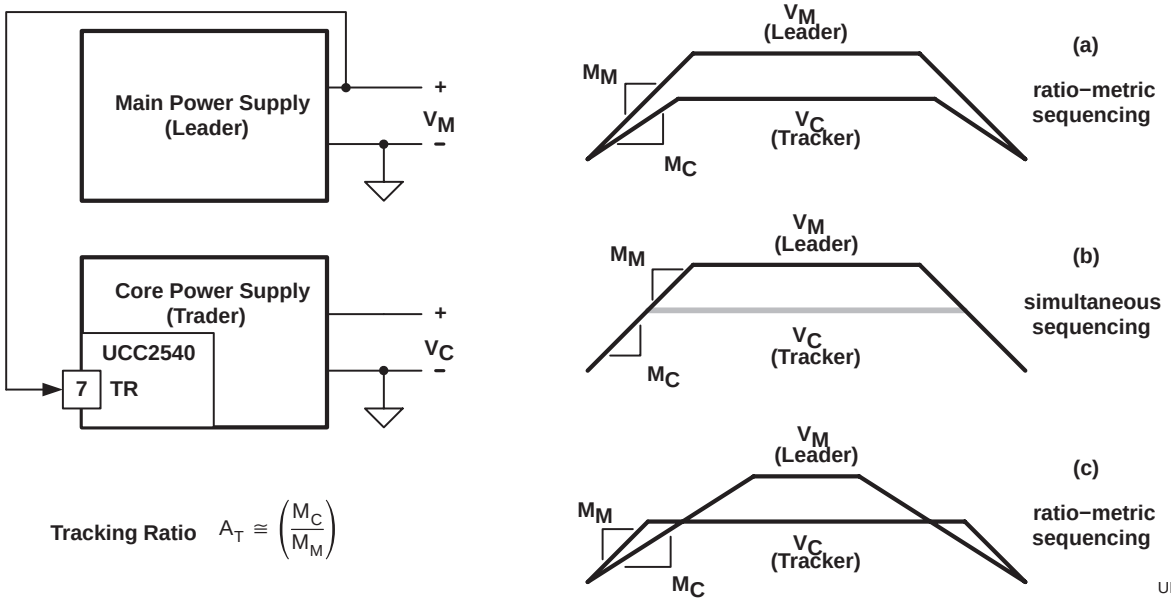


Figure 23. Ratio−Metric Tracking

APPLICATION INFORMATION

The general circuit to program the UCC2540 to track the leader supply voltage by the tracking ratio A_T is shown in Figure 24. To program the tracking profile gains G_{T1} and G_{T2}, follow the ratio-metric tracking design procedure that is listed below. The special case of simultaneous sequencing for $V_M > 1.5V$ is the simplest to design; set $R_{T1} = R_{V1}$ and $R_{T2} = R_{V2}$, G_{T2} is not needed. In many other cases, the circuit can be simplified with the removal of the operational amplifier for G_{T2} and the Zener clamping diode. If an operational amplifier is necessary, it should be capable of rail to rail operation and usually low voltage bias; the TLV271 is an inexpensive solution for both of those requirements. Notice that the tracking circuit in Figure 24 also has a soft-start capacitor, C_{SS}. The soft-start capacitor is useful for limiting the time between short-circuit retry attempts and it can prevent overshoot when recovering from a fault that is experienced in only the tracking supply but not the main supply.

Ratio-Metric Tracking Design Procedure (see Figures 21 and 22)

1. Determine the tracking ratio, A_T.

$$A_T = \frac{M_C}{M_M} \tag{7}$$

where M_C and M_M are the soft-start slopes of V_C and V_M, respectively.

2. Determine G_V.

$$G_V = \frac{R_{V2}}{R_{V1} + R_{V2}} \tag{8}$$

where R_{V2} and $R_{V1}$are selected when designing the voltage control loop.

3. Test G_{T2} if necessary when $V_M \leq 1.5$ V or $A_T G_V > 1$.

   a. If G_{T2} is needed, set GT2 so that both equations (8) and (9) apply.

$$G_{T2} = 1 + \frac{R_{F1}}{R_{F2}} \tag{9}$$

   so that both of the following apply:

$$G_{T2} = \left(\frac{1.5\ V}{V_M \times G_{T1}}\right) \quad \text{and} \quad G_{T2} > \left(A_T \times G_V\right) \tag{10}$$

   b. If G_{T2} is not needed, set $G_{T2} = 1$.

4. Set G_{T1} .

$$G_{T1} = \frac{A_T \times G_V}{G_{T2}} = \frac{R_{T2}}{R_{T1} + R_{T2}} \tag{11}$$

5. Select R_{T1} and R_{T2} so that $R_{T1} \parallel R_{T2} \approx R_{V1} \parallel R_{V2}$ to minimize offset differences.

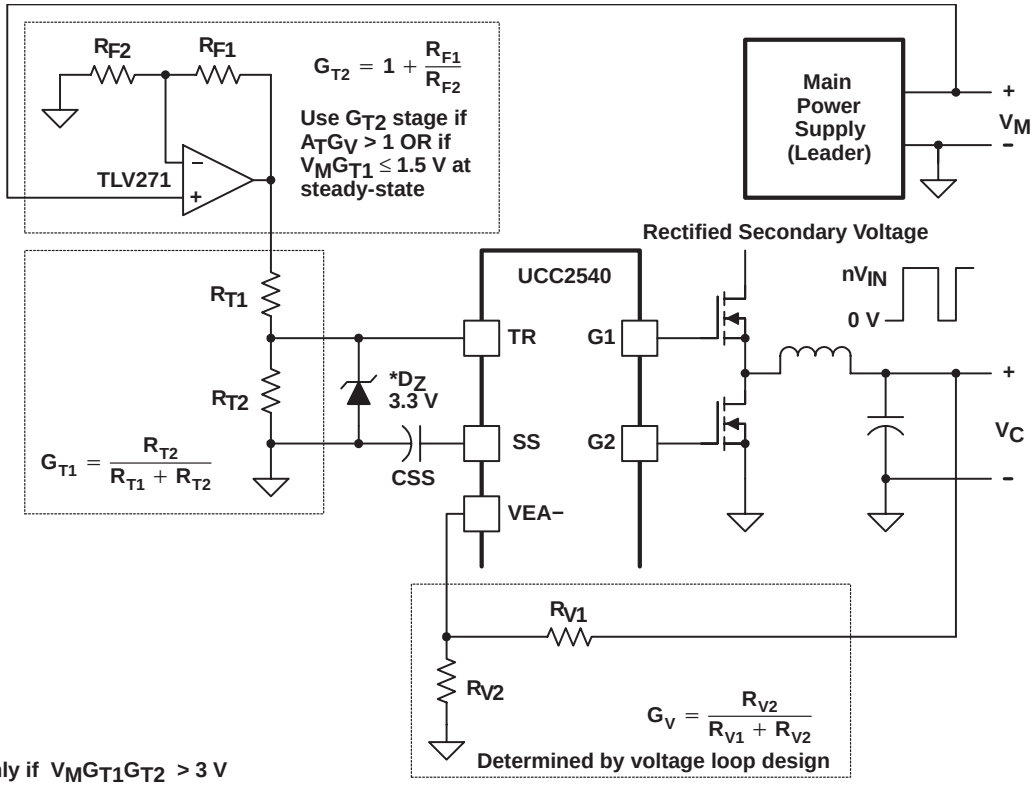


Figure 24. Programming the UCC2540 to Track Another Output

More elaborate power supply sequencing and tracking can easily be implemented by extending the above techniques. Consult reference [5] for further information

THERMAL INFORMATION

The useful temperature range of a controller that contains high-current output drivers is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2540 is available in the 20-pin HTSSOP PowerPAD™ package.

The PowerPAD™ HTSSOP-20 (PWP) offers the most effective means of removing the heat from the semiconductor junction and therefore long term reliability improvement. As illustrated in [5], the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the device package, reducing the θjc down to 2°C/W. Data is presented in [5] to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in [6] to realize a significant improvement in heat−sinking over standard non-PowerPAD surface mount packages.

TYPICAL CHARACTERISTICS

OUTPUT REFERENCE VOLTAGE vs TEMPERATURE

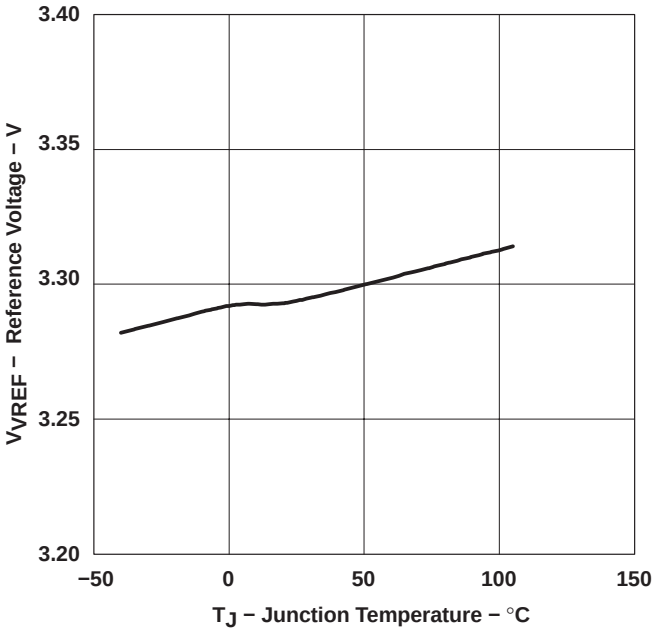


Figure 25

RAMP CURRENT vs TEMPERATURE

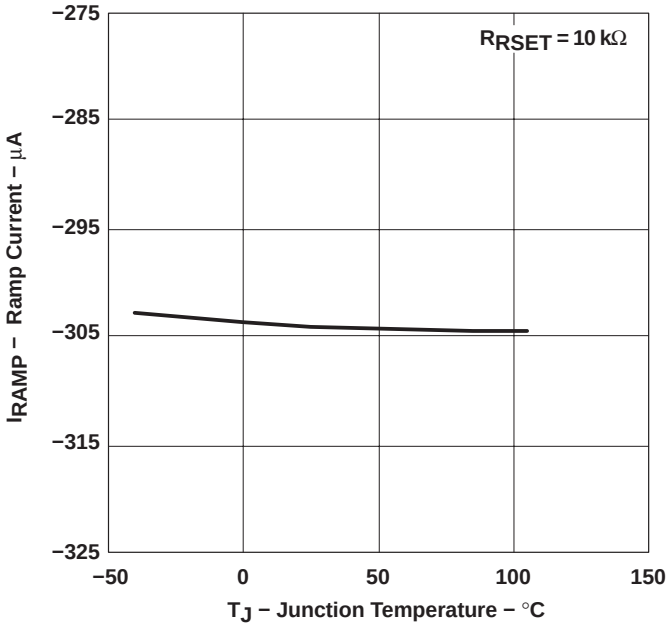


Figure 26

IG2C/IRAMP AND ISS/IRAMP vs TEMPERATURE

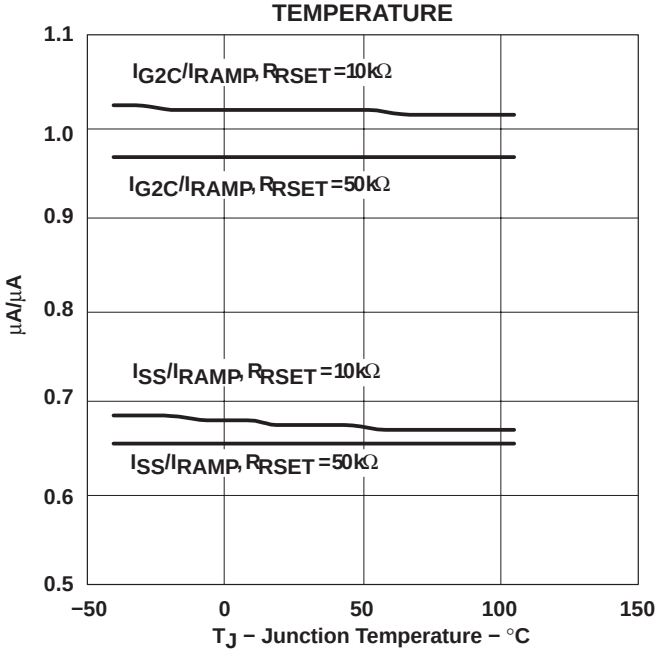


Figure 27

REGULATOR OUTPUT VOLTAGE vs TEMPERATURE

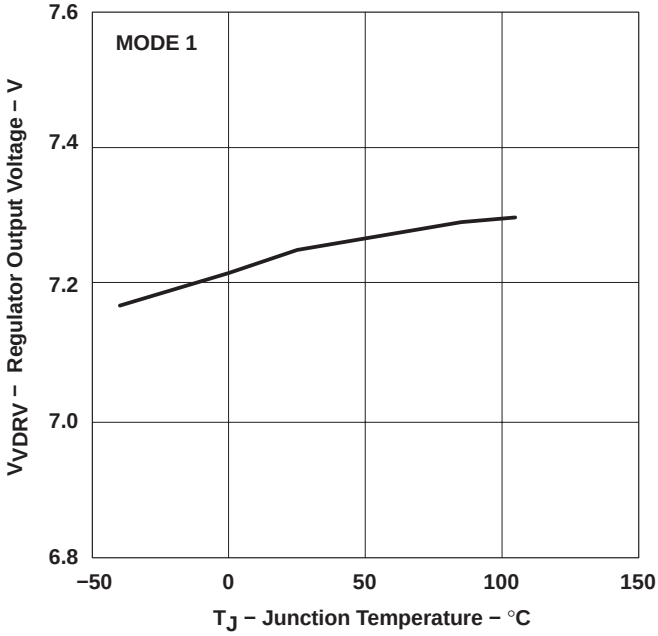


Figure 28

TYPICAL CHARACTERISTICS

TRACKING TO VOLTAGE ERROR AMPLIFIER OFFSET vs TEMPERATURE

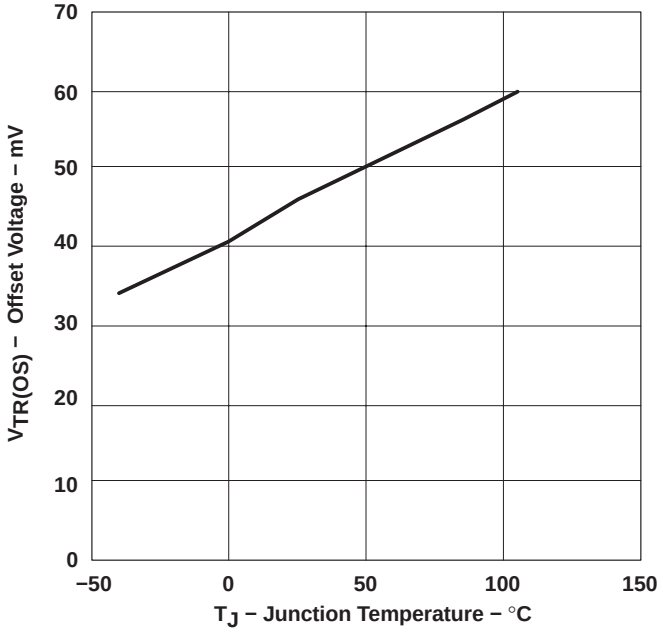


Figure 29

CURRENT ERROR AMPLIFIER OFFSET vs TEMPERATURE

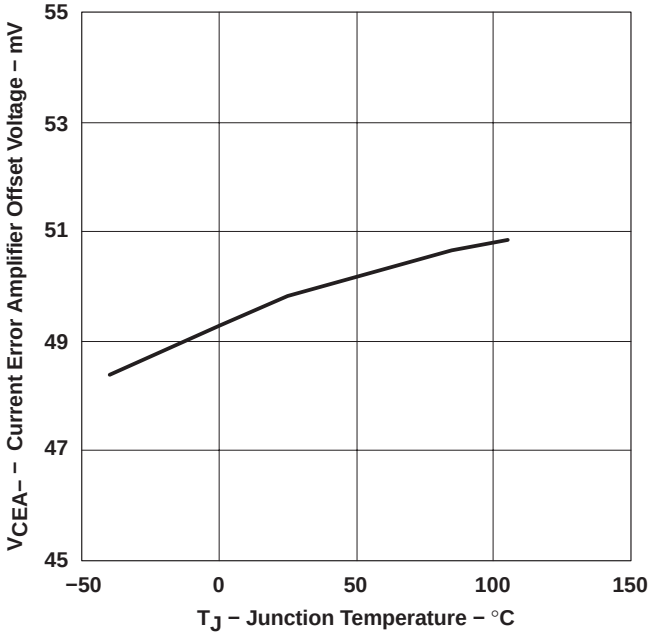


Figure 30

SYNCIN THRESHOLD VOLTAGE vs TEMPERATURE

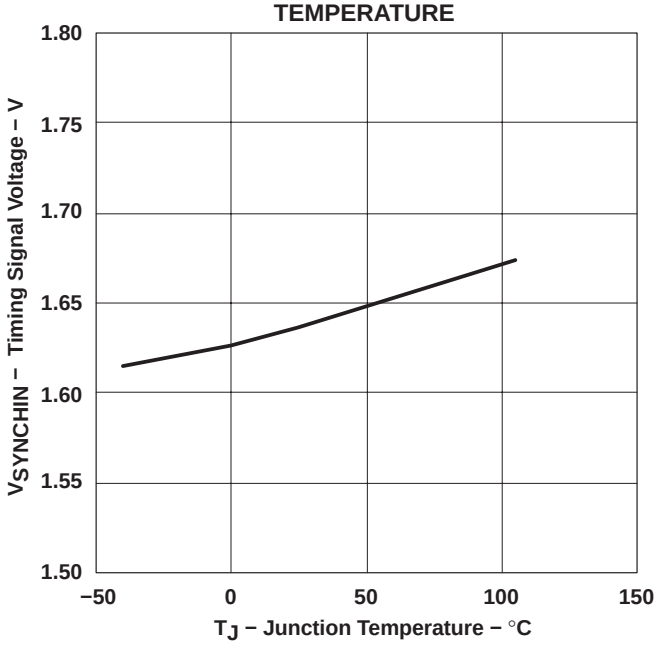


Figure 31

INVERTING AMPLIFIER GAIN AND PHASE vs FREQUENCY

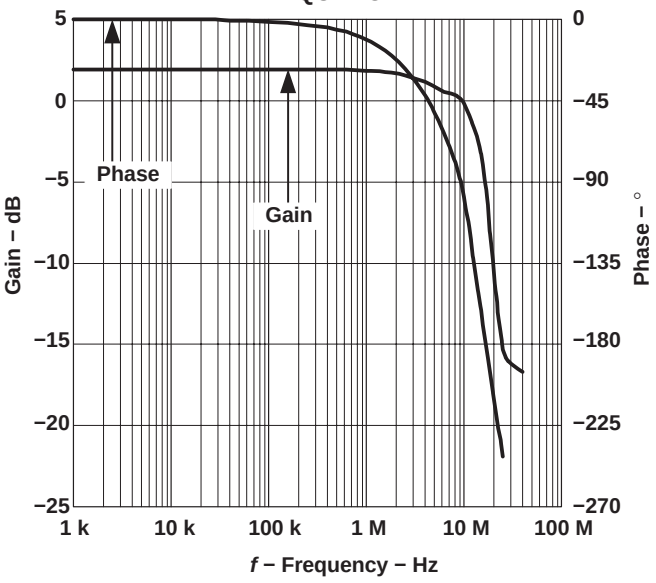


Figure 32

TYPICAL CHARACTERISTICS

CURRRENT ERROR AMPLIFIER GAIN AND PHASE
vs
FREQUENCY

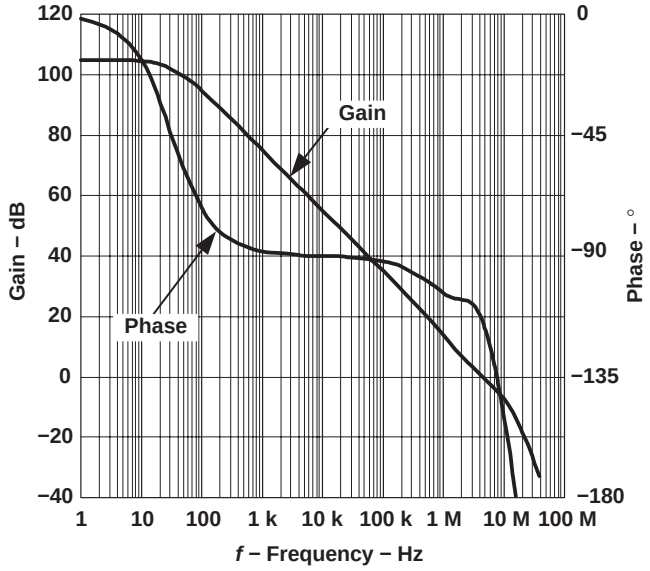


Figure 33

VOLTAGE ERROR AMPLIFIER GAIN AND PHASE
vs
FREQUENCY

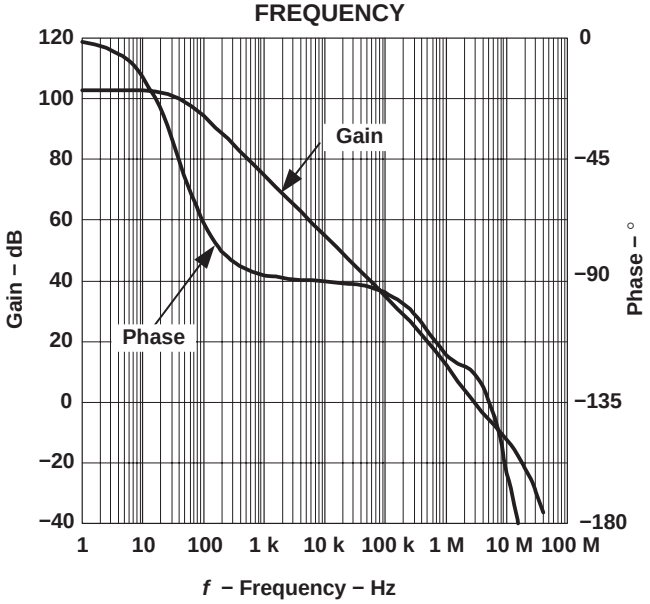


Figure 34

OPERATING CURRENT (DC)
vs
BIAS VOLTAGE

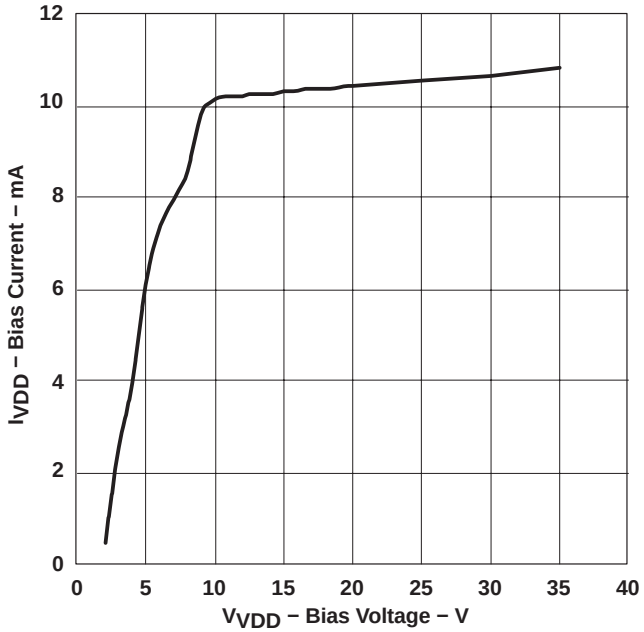


Figure 35

TYPICAL CHARACTERISTICS

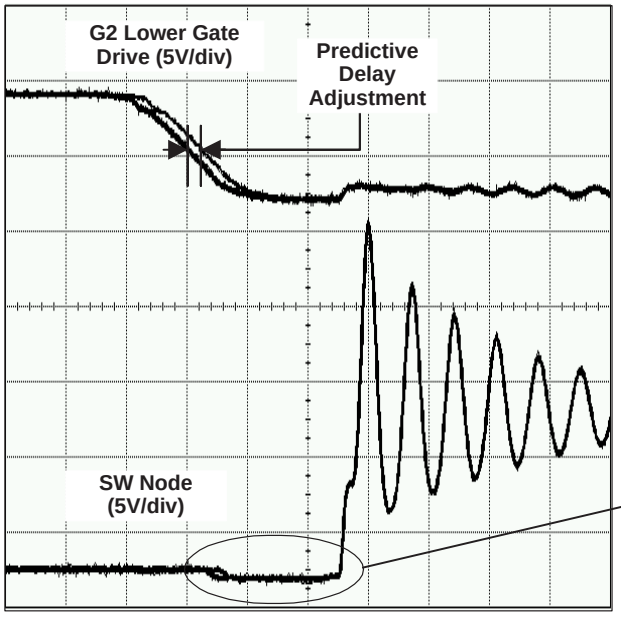


Figure 36. Predictive Gate Drive − G2 Falling

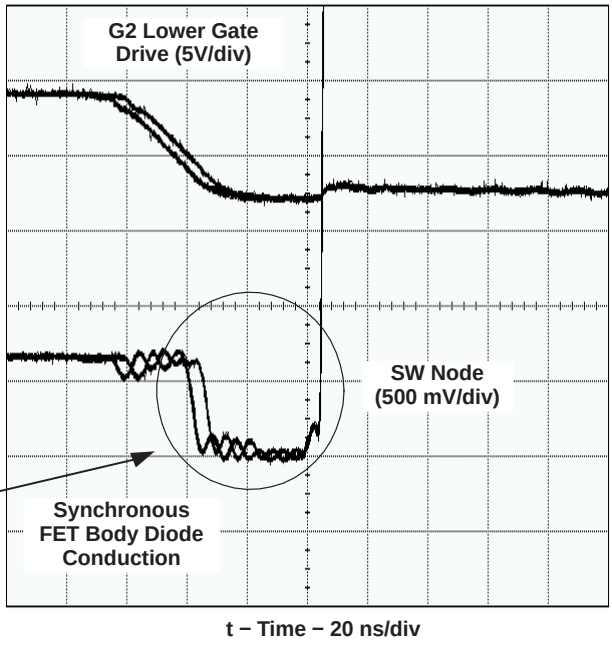


Figure 37. Predictive Gate Drive − G2 Falling

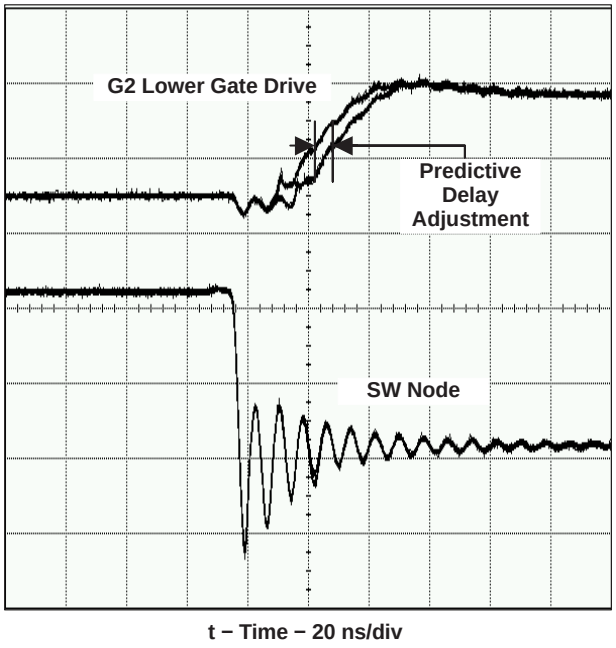


Figure 38. Predictive Gate Drive − G2 Falling

RELATED PRODUCTS

- UCC28089 Primary Side Push-Pull Oscillator
- UCC27223 High Efficiency Predictive Synchronous Buck Driver with Enable
- UCC3583 Switch Mode Secondary Side Post Regulator
- UCC25701 Advanced Voltage Mode Pulse Width Modulator
- UCC3808A Low-Power Currrent-Mode Push-Pull PWM
- UCC38083/4/5/6 8-Pin Current-Mode Push-Pull PWM with Programmable Slope Compensation

REFERENCES

1. Power Supply Seminar SEM−1300 Topic 1: *Unique Cascaded Power Converter Topology for High Current Low Output Voltage Applications*, by L. Balogh, C. Bridge, and B. Andreycak, (SLUP118)
2. Power Supply Seminar SEM−1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by L. Balogh, (SLUP133)
3. Datasheet, *UCC27223 High Efficiency Predictive Synchronous Buck Driver*, (SLUS558)
4. Datasheet, *UCC37323/4/5 Dual 4−A Peak High Speed Low−Side Power MOSFET Drivers*, (SLUS492A)
5. Power Supply Seminar SEM1600 Topic 2: Sequencing Power Supplies in Multiple Voltage Rail Environments, by D. Daniels, D. Gehrke, and M. Segal, (SLUP224)
6. Technical Brief, *PowerPAD Thermally Enhanced Package*, (SLMA002)
7. Application Brief, *PowerPAD Made Easy*, (SLMA004)
8. Datasheet, *TPS3103K33 Ultra-Low Supply Current/Supply Voltage Supervisory Circuits*, (SLVS363)
9. Application Note, *A Revolutionary Power Management Solution for Highly Efficient, Multiple Output Applications*, by Bill Andreycak, (SLUA255)
10. Application Note, *Predictive Gate Drive™ FAQ*, by Steve Mappus (SLUA285)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2540PWPR	NRND	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2540
UCC2540PWPR.A	NRND	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2540

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

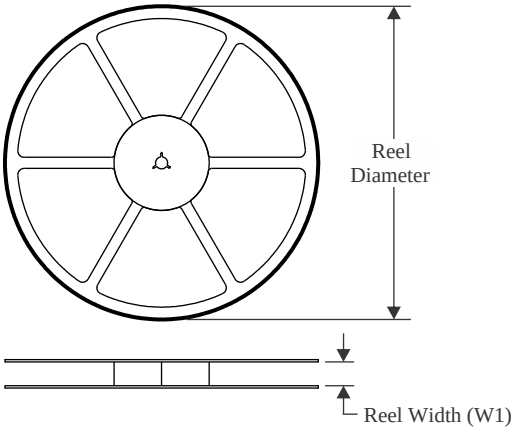
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

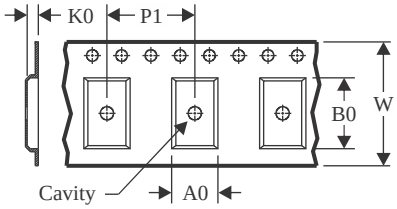
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

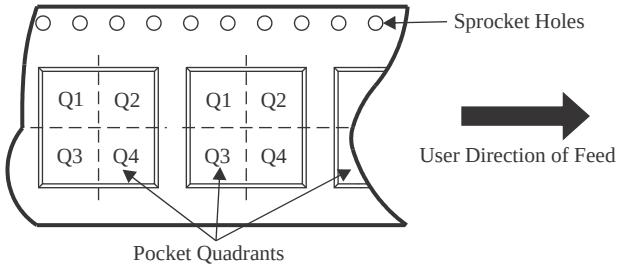


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

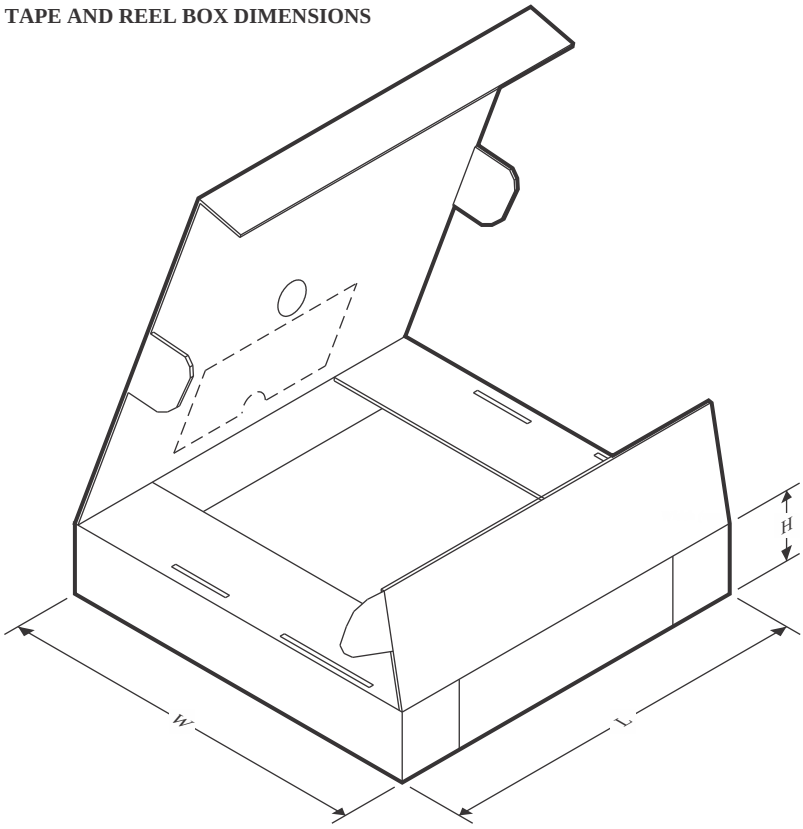
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2540PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2540PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

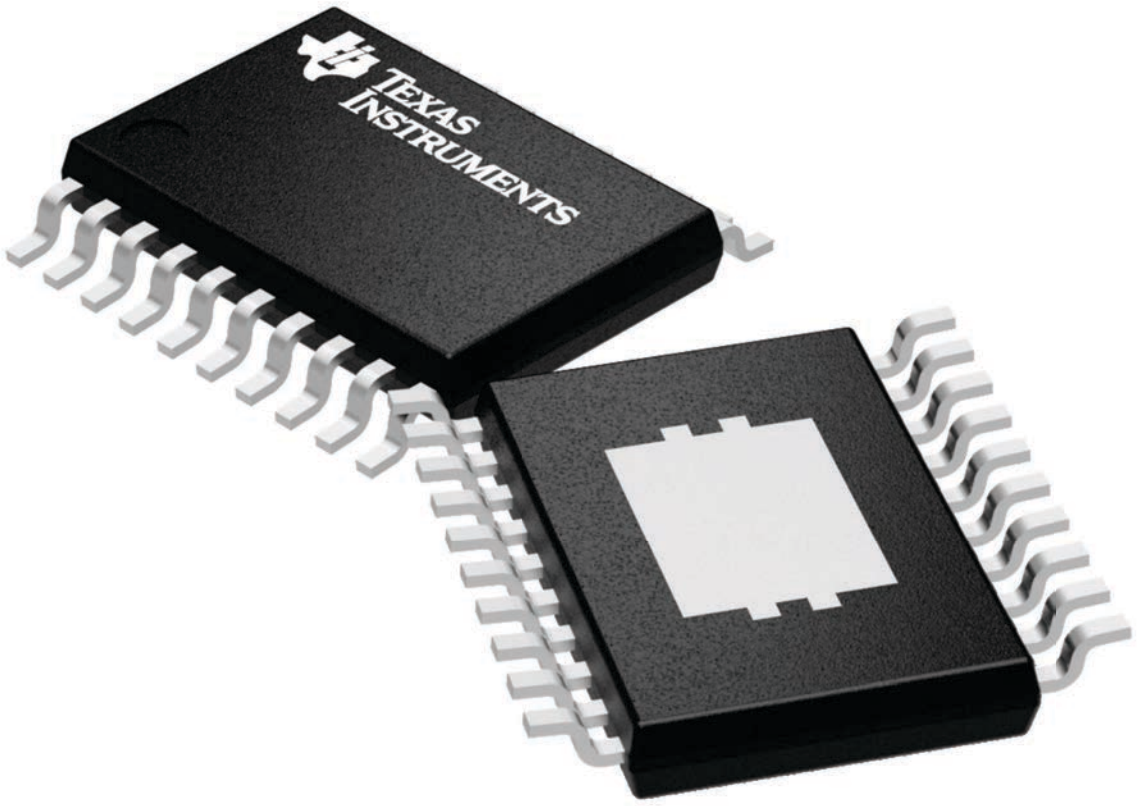
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

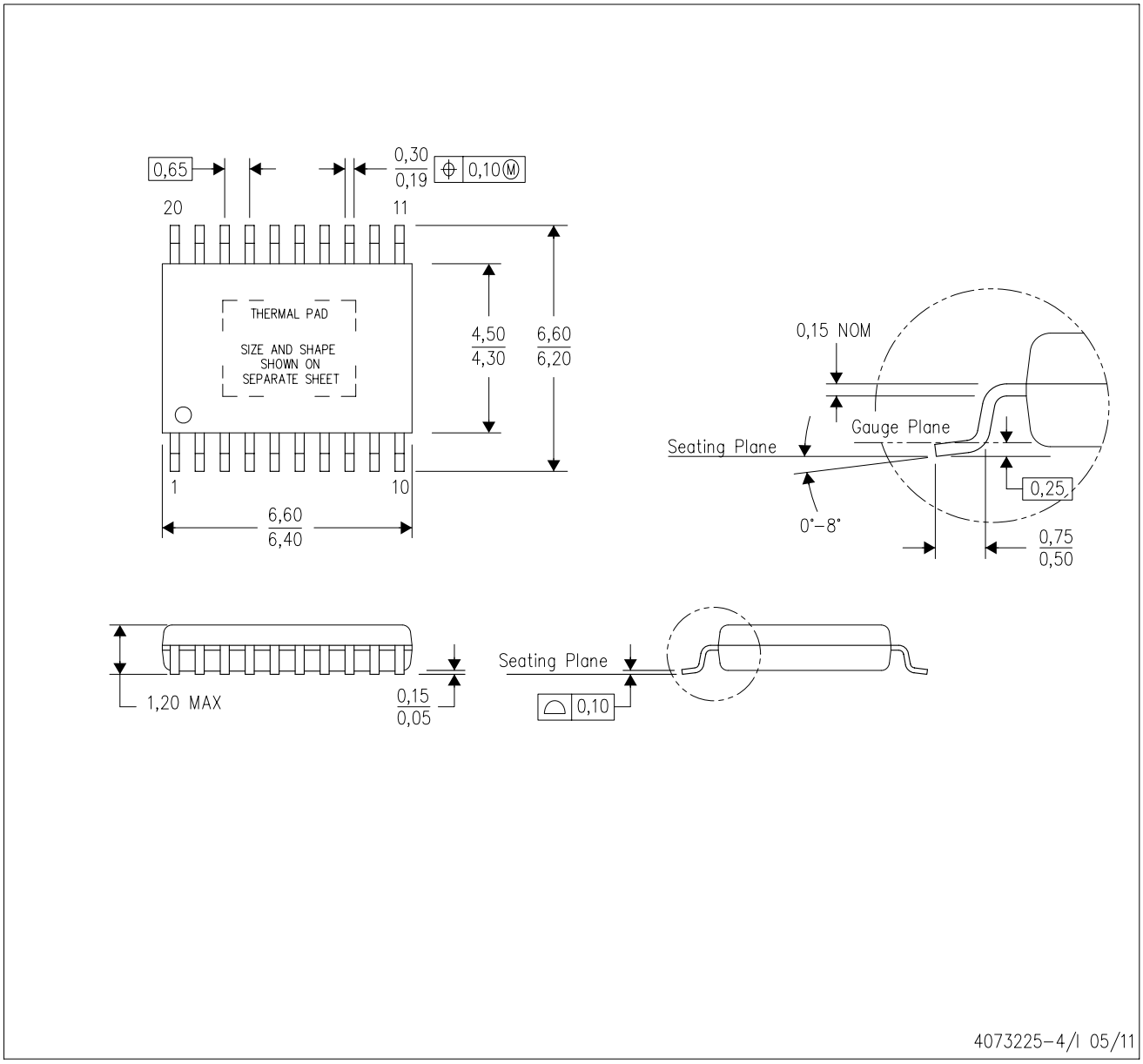
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

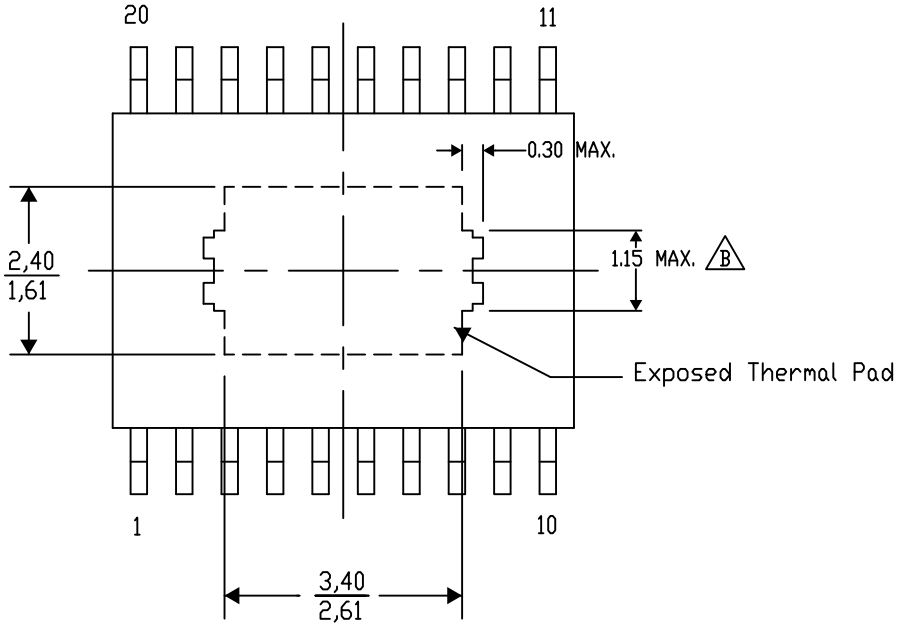
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

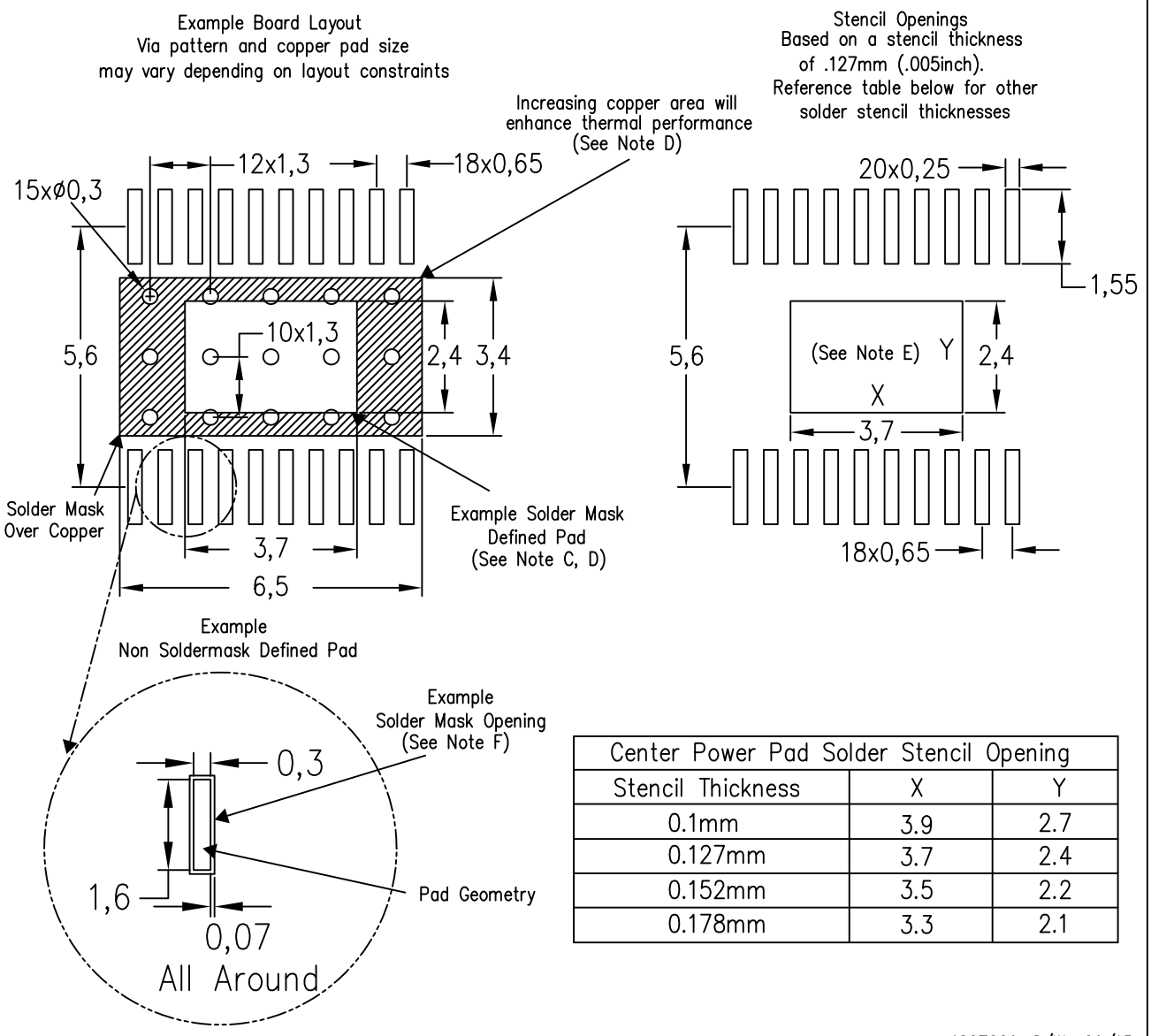
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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