DLP301S 0.3-Inch 3.6-Megapixel DMD for TI DLP® 3D Printers

1 Features

- 0.3-Inch (7.93-mm) diagonal micromirror array
  - 1280 × 720 array of aluminum micrometer-sized mirrors, in an orthogonal layout
  - 3.6 Megapixels, 2560 × 1440 pixels on the resin
  - 5.4-micron micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Side illumination for optimal efficiency and optical engine size
  - Polarization independent aluminum micromirror surface
- 8-Bit SubLVDS input data bus
- Dedicated DLPC1438 3D print controller and DLPA200x or DLPA300x PMIC/LED driver for reliable operation

2 Applications

- TI DLP® 3D Printer
  - Additive manufacturing
  - Vat polymerization
  - Masked stereolithography (mSLA 3D printer)
- Dental DLP 3D printer
- Light exposure: programmable spatial and temporal light exposure

3 Description

The DLP301S digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DMD displays a very crisp and high-quality image. This DMD is a component of the chipset comprising the DLP301S DMD, DLPC1438 3D Print controller, and DLPA200x/DLPA300x PMIC/LED driver. The compact physical size of this DMD coupled with the controller and the PMIC/LED driver provides a complete system solution that enables high output optical engines for fast, high resolution, reliable DLP 3D printers.

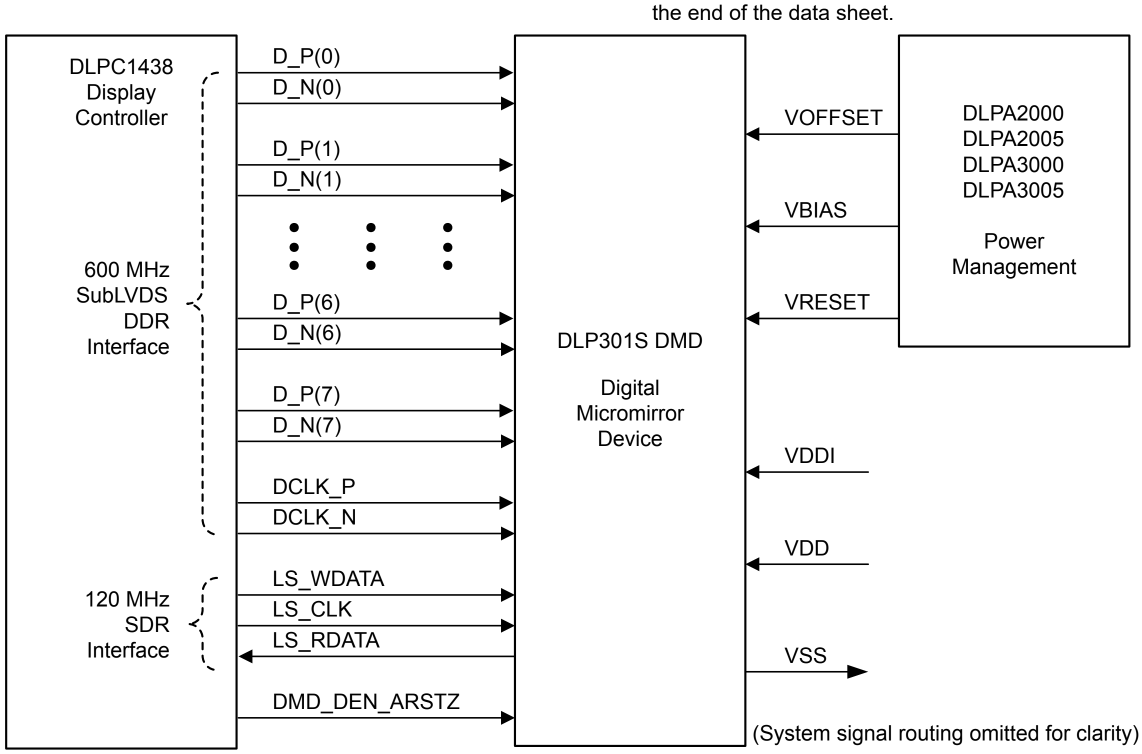
Learn more about TI DLP(R) 3D printing technology on the 3D printing and direct imaging products page.

The DLP advanced light control resources on ti.com accelerate time to market, which include reference designs, optical modules manufacturers, and DLP design network partners.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP301S	FQS (99)	19.25 mm × 7.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (September 2022)	Page
• Changed the device status from *Advance Information* to *Production Data*	1
• Updated the Absolute Maximum Ratings disclaimer to the latest TI standard	7
• Updated *Micromirror Array Optical Characteristics*	18
• Changed Micromirror tilt angle tolerance to ±1.4° in Section 6.11	18
• Changed Micromirror crossover and switching time specification in Section 6.11 to match actual operation values	18
• Added *Third-Party Products Disclaimer*	35

5 Pin Configuration and Functions

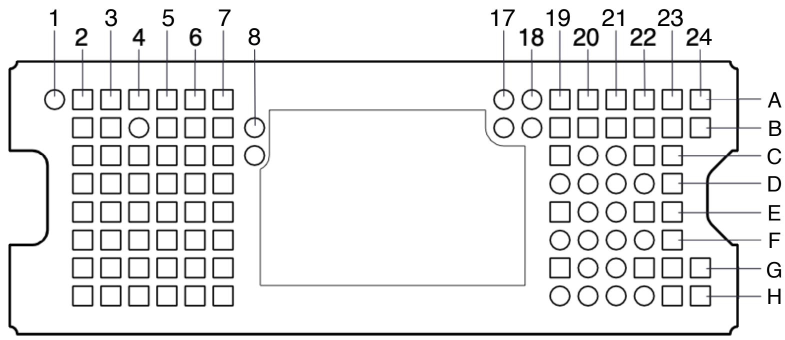


Figure 5-1. FQS Package 99-Pin LGA (Bottom View)

Table 5-1. Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	C6	I	SubLVDS	Double	Data, Negative	3.15
D_P(0)	C5	I	SubLVDS	Double	Data, Positive	3.09
D_N(1)	D7	I	SubLVDS	Double	Data, Negative	3.24
D_P(1)	D6	I	SubLVDS	Double	Data, Positive	3.29
D_N(2)	D5	I	SubLVDS	Double	Data, Negative	2.00
D_P(2)	D4	I	SubLVDS	Double	Data, Positive	1.97
D_N(3)	F7	I	SubLVDS	Double	Data, Negative	3.96
D_P(3)	F6	I	SubLVDS	Double	Data, Positive	4.04
D_N(4)	F5	I	SubLVDS	Double	Data, Negative	1.39
D_P(4)	F4	I	SubLVDS	Double	Data, Positive	1.39
D_N(5)	G6	I	SubLVDS	Double	Data, Negative	2.85
D_P(5)	G5	I	SubLVDS	Double	Data, Positive	2.90
D_N(6)	H5	I	SubLVDS	Double	Data, Negative	2.37
D_P(6)	H4	I	SubLVDS	Double	Data, Positive	2.37
D_N(7)	H7	I	SubLVDS	Double	Data, Negative	3.22
D_P(7)	H6	I	SubLVDS	Double	Data, Positive	3.26
DCLK_N	E6	I	SubLVDS	Double	Clock, Negative	2.33
DCLK_P	E5	I	SubLVDS	Double	Clock, Positive	2.33
CONTROL INPUTS						
LS_WDATA	B3	I	LPSDR(1)	Single	Write data for low speed interface.	17.1
LS_CLK	B5	I	LPSDR	Single	Clock for low-speed interface	15.28
DMD_DEN_ARSTZ	B2	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	17.91
LS_RDATA	B7	O	LPSDR	Single	Read data for low-speed interface	12.29
POWER (3)						
VBIAS	A6	Power			Supply voltage for positive bias level at micromirrors	
VBIAS	A22	Power				

Table 5-1. Pin Functions – Connector Pins[(1)] (continued)

PIN NAME	PIN NO.	TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[(2)] (mm)
VOFFSET	B21	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	
VOFFSET	G2	Power				
VRESET	A5	Power			Supply voltage for negative reset level at micromirrors.	
VRESET	A23	Power				
VDD	C2	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
VDD	A19	Power				
VDD	A20	Power				
VDD	A21	Power				
VDD	B20	Power				
VDD	C2	Power				
VDD	D2	Power				
VDD	D3	Power				
VDD	D23	Power				
VDD	E2	Power				
VDD	F2	Power				
VDD	F3	Power				
VDD	F23	Power				
VDDI	B6	Power			Supply voltage for SubLVDS receivers.	
VDDI	B19	Power				
VDDI	C3	Power				
VDDI	C23	Power				
VDDI	E3	Power				
VDDI	E23	Power				
VDDI	G3	Power				
VDDI	G23	Power				
VSS	A2	Ground			Common return. Ground for all power	
VSS	A3	Ground				
VSS	A4	Ground				
VSS	A7	Ground				
VSS	A24	Ground				
VSS	B22	Ground				
VSS	B23	Ground				
VSS	B24	Ground				
VSS	C4	Ground				
VSS	C7	Ground				
VSS	C19	Ground				
VSS	C22	Ground				
VSS	E4	Ground				
VSS	E7	Ground				

Table 5-1. Pin Functions – Connector Pins[(1)] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[(2)] (mm)
NAME	NO.					
VSS	E19	Ground			Common return. Ground for all power	
VSS	E22	Ground				
VSS	G4	Ground				
VSS	G7	Ground				
VSS	G19	Ground				
VSS	G22	Ground				
VSS	G24	Ground				
VSS	H2	Ground				
VSS	H3	Ground				
VSS	H23	Ground				
VSS	H24	Ground				

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQS ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.
(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

Table 5-2. Pin Functions – No Connect

NUMBER	SYSTEM BOARD
TEST PADS	
A1	Do not connect.
A17	Do not connect.
A18	Do not connect.
B8	Do not connect.
B17	Do not connect.
B18	Do not connect.
C8	Do not connect.
UNUSED PINS	
B4	Do not connect.
C20	Do not connect.
C21	Do not connect.
D19	Do not connect.
D20	Do not connect.
D21	Do not connect.
D22	Do not connect.
E20	Do not connect.
E21	Do not connect.
F19	Do not connect.
F20	Do not connect.
F21	Do not connect.
F22	Do not connect.
G20	Do not connect.
G21	Do not connect.
H19	Do not connect.
H20	Do not connect.

Table 5-2. Pin Functions – No Connect (continued)

NUMBER	SYSTEM BOARD
H21	Do not connect.
H22	Do not connect.

6 Specifications

6.1 Absolute Maximum Ratings

See [1]

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic[2] Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers[2]	–0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode[2] [3]	–0.5	11	V
	VBIAS	Supply voltage for micromirror electrode[2]	–0.5	19	V
	VRESET	Supply voltage for micromirror electrode[2]	–15	0.5	V
	| VDDI–VDD |	Supply voltage delta (absolute value)[4]		0.3	V
	| VBIAS–VOFFSET |	Supply voltage delta (absolute value)[5]		11	V
	| VBIAS–VRESET |	Supply voltage delta (absolute value)[6]		34	V
Input voltage	Input voltage for other inputs LPSDR[2]		–0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS[2] [7]		–0.5	VDDI + 0.5	V
Input pins	| VID |	SubLVDS input differential voltage (absolute value)[7]		810	mV
	IID	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		560	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational [8]	–20	90	°C
		Temperature – non-operational[8]	–40	90	°C
	T_{DP}	Dew Point Temperature - operating and non-operating (non-condensing)		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1[9]		30	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated in Section 7.6) or of any point along the Window Edge as defined in Section 7.6. The locations of thermal test points TP2 and TP3 in Section 7.6 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Section 7.6. The window test points TP2 and TP3 shown in Section 7.6 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operational in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing)(1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(3)					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode(4)	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
|VDDI–VDD|	Supply voltage delta (absolute value)(5)			0.3	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value)(6)			10.5	V
|VBIAS–VRESET|	Supply voltage delta (absolute value)(7)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(8)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(9)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(9)					
$\|V_{ID}\|$	SubLVDS input differential voltage (absolute value) Figure 6-9, Figure 6-10	150	250	350	mV
V_{CM}	Common mode voltage Figure 6-9, Figure 6-10	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage Figure 6-9, Figure 6-10	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance Figure 6-11	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(10) (11) (12)	0		40	°C
	Array Temperature - short-term operational, 25 hr max(11) (13)	–20		–10	
	Array Temperature - short-term operational, 500 hr max(11) (13)	–10		0	
$\lvert T_{DELTA} \rvert$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (14)			15	°C
T_{WINDOW}	Window temperature – operational(15)			85	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(16)			24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(17)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	Months
$Q_{AP\text{-}ILL}$	Illumination overfill in critical area(19) (20)			0	W/cm^2
ILL_{UV}	Illumination wavelengths < 380 nm(10)			2	mW/cm^2
$ILL_{380 - 390\ nm}$	Illumination wavelengths between 380 nm and 390 nm			55	mW/cm^2
$ILL_{390 - 400\ nm}$	Illumination wavelengths between 390 nm and 400 nm			450	mW/cm^2
$ILL_{400 - 550\ nm}$	Illumination wavelengths between 400 nm and 550 nm			3	W/cm^2
$ILL_{> 550\ nm}$	Illumination wavelengths > 550 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(18)			55	deg

(1) Section 6.4 is applicable after the DMD is installed in the final product.
(2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by Section 6.4. No level of performance is implied when operating the device above or below the *Section 6.4* limits.
(3) All voltage values are with respect to the ground pins (VSS).
(4) VOFFSET supply transients must fall within specified maximum voltages.
(5) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(6) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(8) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(9) Refer to the SubLVDS timing requirements in Section 6.7.
(10) Simultaneous exposure of the DMD to the maximum limits in Section 6.4 for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Section 7.6 and the Package Thermal Resistance using Section 7.6.
(12) Long-term is defined as the usable life of the device.
(13) Short-term is the total cumulative time over the useful life of the device.
(14) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Section 7.6. The window test points TP2 and TP3 shown in Section 7.6 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(15) Window temperature is the highest temperature on the window edge shown in Section 7.6. The locations of thermal test points TP2 and TP3 in Section 7.6 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a higher temperature, that point should be used.
(16) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(17) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(18) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
(19) The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.
(20) Applies to the region in red in Figure 6-1, at the inside plane of the glass window where the physical aperture is located.

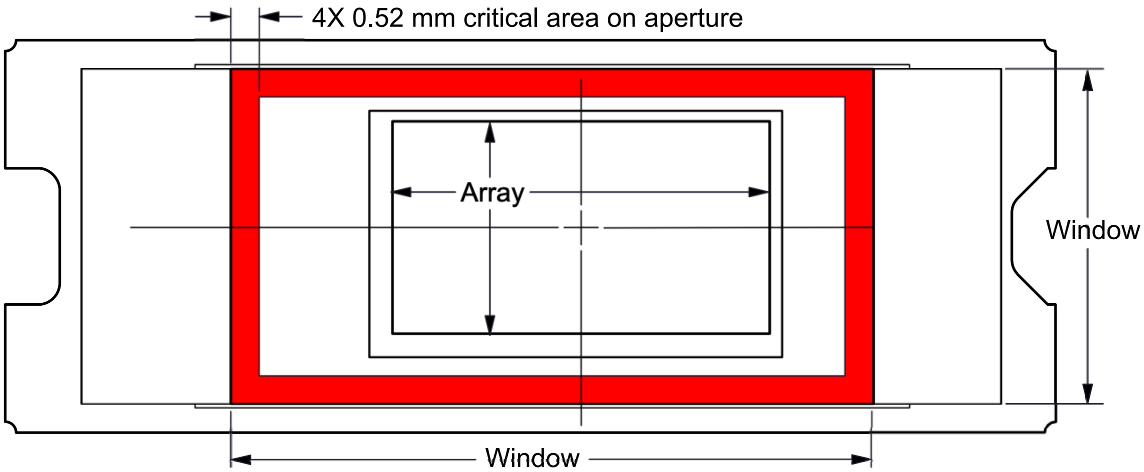


Figure 6-1. Illumination Overfill Diagram—Critical Area

6.5 Thermal Information

THERMAL METRIC[(1)]		DLP301S FQS (LGA) 99 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)[(1)]	2.7	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the Section 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[(10)]

PARAMETER		TEST CONDITIONS[(2)]	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD[(3)] [(5)]	VDD = 1.95 V			60.5	mA
		VDD = 1.8 V		54		
I_{DDI}	Supply current: VDDI[(3)] [(5)]	VDDI = 1.95 V			16.5	mA
		VDD = 1.8 V		11.3		
I_{OFFSET}	Supply current: VOFFSET[(4)] [(6)]	VOFFSET = 10.5 V			2.2	mA
		VOFFSET = 10 V		1.5		
I_{BIAS}	Supply current: VBIAS[(4)] [(6)]	VBIAS = 18.5 V			0.6	mA
		VBIAS = 18 V		0.3		
I_{RESET}	Supply current: VRESET[(6)]	VRESET = –14.5 V			2.4	mA
		VRESET = –14 V		1.7		
POWER[(1)]						
P_{DD}	Supply power dissipation: VDD[(3)] [(5)]	VDD = 1.95 V			118	mW
		VDD = 1.8 V		95		
P_{DDI}	Supply power dissipation: VDDI[(3)] [(5)]	VDDI = 1.95 V			32	mW
		VDD = 1.8 V		20		

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(10)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
P_{OFFSET}	Supply power dissipation: VOFFSET(4) (6)	VOFFSET = 10.5 V			23	mW
		VOFFSET = 10 V		15		
P_{BIAS}	Supply power dissipation: VBIAS(4) (6)	VBIAS = 18.5 V			11	mW
		VBIAS = 18 V		6		
P_{RESET}	Supply power dissipation: VRESET(6)	VRESET = –14.5 V			35	mW
		VRESET = –14 V		24		
P_{TOTAL}	Supply power dissipation: Total			160	219	mW
LPSDR INPUT(7)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage(9)		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	Figure 6-12	0.1 × VDD		0.4 × VDD	V
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(8)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			10	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(1) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(5) Supply power dissipation based on non-compressed commands and data
(6) Supply power dissipation based on three global resets in 200 µs
(7) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(8) LPSDR specification is for pin LS_RDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) Device electrical characteristics are over Section 6.4 unless otherwise noted.

6.7 Timing Requirements

Device electrical characteristics are over Section 6.4 unless otherwise noted.

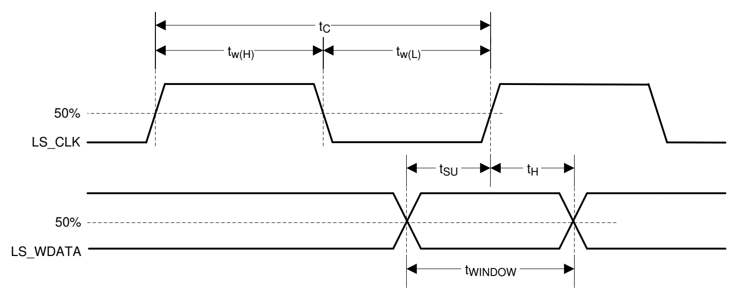
			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × VDD, Figure 6-3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × VDD, Figure 6-3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × VDD, Figure 6-4	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × VDD, Figure 6-4	0.25			V/ns
t_c	Cycle time LS_CLK,	Figure 6-2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, Figure 6-2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, Figure 6-2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, Figure 6-2	1.5			ns

6.7 Timing Requirements (continued)

Device electrical characteristics are over Section 6.4 unless otherwise noted.

			MIN	NOM	MAX	UNIT
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, Figure 6-2	1.5			ns
t_{WINDOW}	Window time(1) (4)	Setup time + Hold time, Figure 6-2	3			ns
$t_{DERATING}$	Window time derating(1) (4)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, Figure 6-6		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, Figure 6-5	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, Figure 6-5	0.7	1		V/ns
t_c	Cycle time DCLK,	Figure 6-7	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, Figure 6-7	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, Figure 6-7	0.79			ns
t_{su}	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, Figure 6-7				
t_h	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, Figure 6-7				
t_{WINDOW}	Window time	Setup time + Hold time, Figure 6-7, Figure 6-8			0.3	ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(3)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 6-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 6-4.
(3) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
(4) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.



Low-speed interface is LPSDR and adheres to the Section 6.6 and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 6-2. LPSDR Switching Parameters

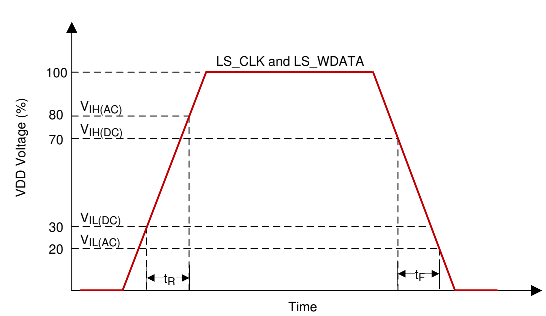


Figure 6-3. LPSDR Input Slew Rate

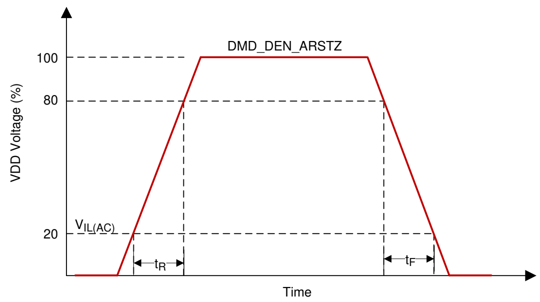


Figure 6-4. LPSDR Input Slew Rate

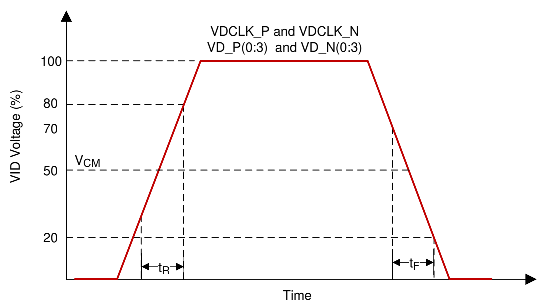


Figure 6-5. SubLVDS Input Rise and Fall Slew Rate

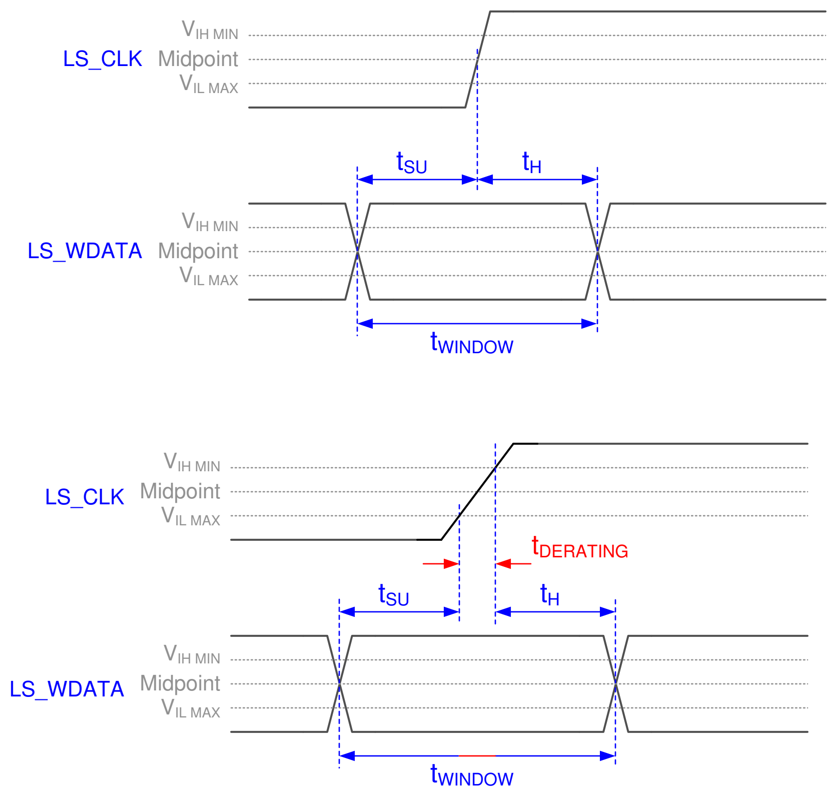


Figure 6-6. Window Time Derating Concept

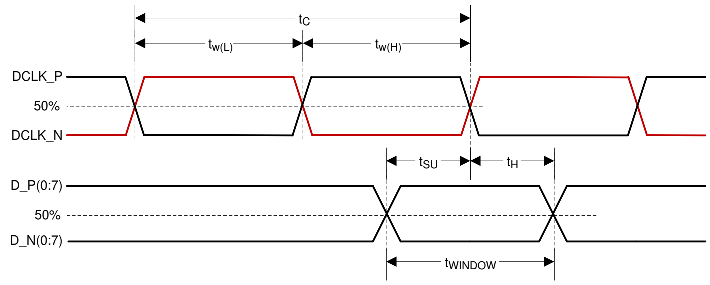
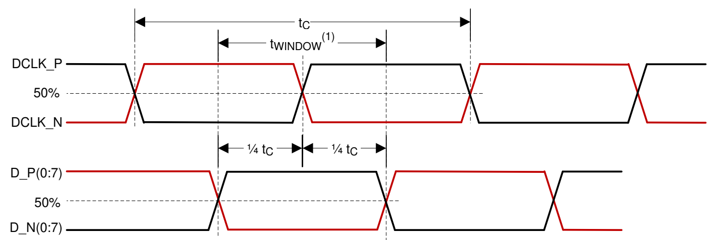


Figure 6-7. SubLVDS Switching Parameters



(1) High-speed training scan window
(2) Refer to Section 7.3.3 for details

Figure 6-8. High-Speed Training Scan Window

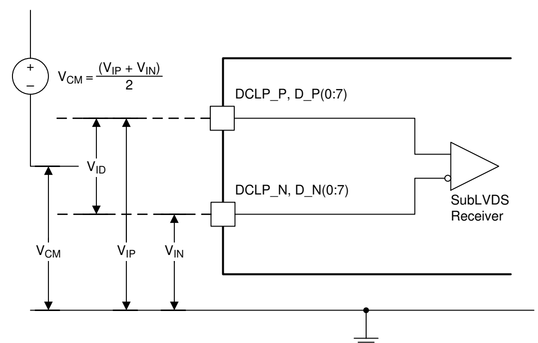


Figure 6-9. SubLVDS Voltage Parameters

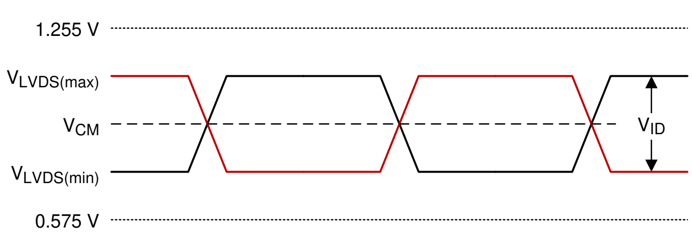


Figure 6-10. SubLVDS Waveform Parameters

$$V_{SubLVDS(max)} = V_{CM(max)} + ½ \times |V_{ID(max)}|$$

$$V_{SubLVDS(min)} = V_{CM(min)} – ½ \times |V_{ID(max)}|$$

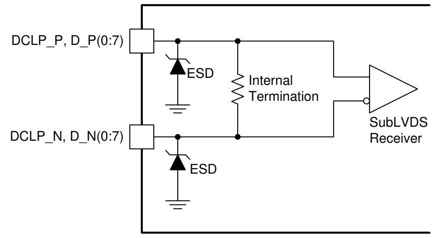


Figure 6-11. SubLVDS Equivalent Input Circuit

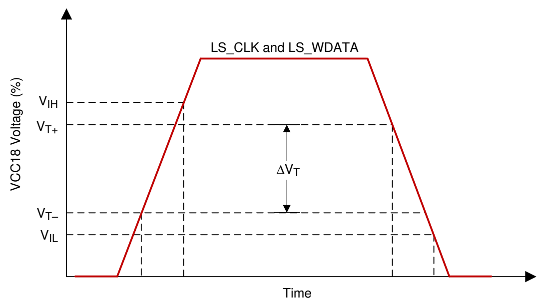


Figure 6-12. LPSDR Input Hysteresis

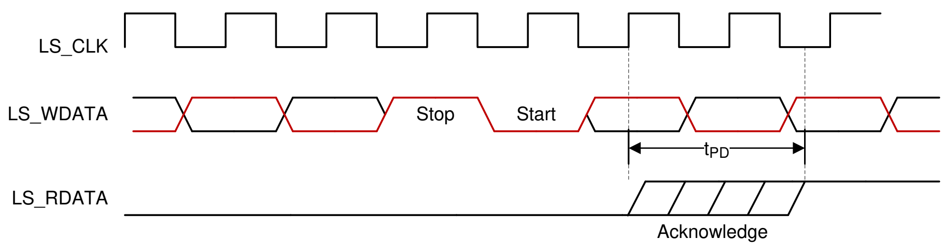
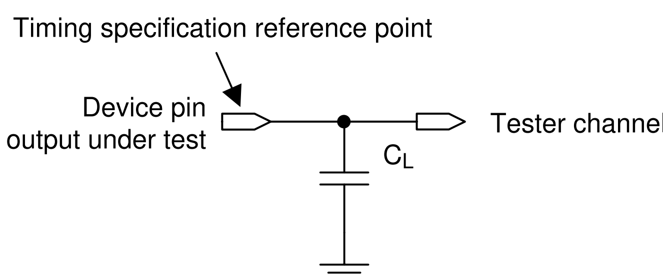


Figure 6-13. LPSDR Read Out



See Section 7.3.4 for more information.

Figure 6-14. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. Figure 6-13	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output duty cycle distortion, LS_RDATA		40%		60%	

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal Interface Area (see Figure 6-15)			60	N
	Clamping and Electrical Interface Area (see Figure 6-15)			110	N

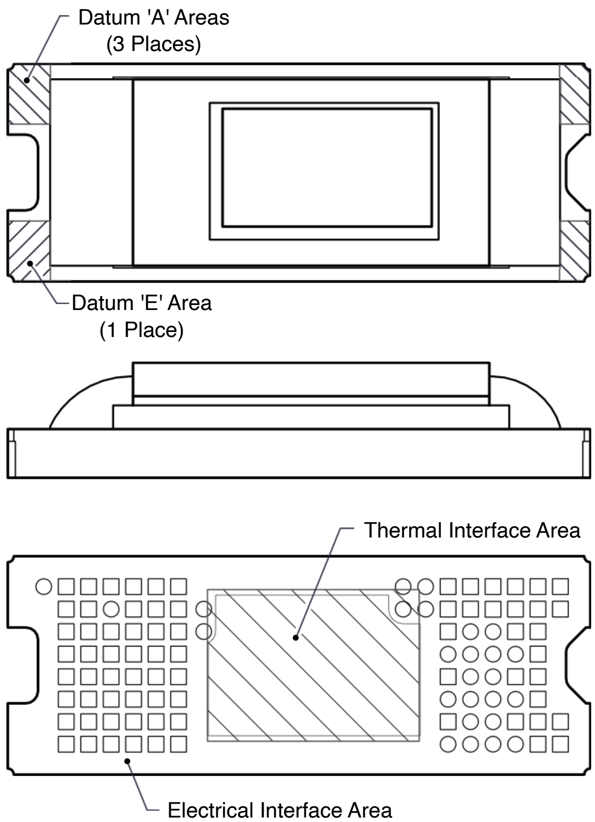


Figure 6-15. System Interface Loads

6.10 Micromirror Array Physical Characteristics

PARAMETER			VALUE	UNIT
	Number of active columns	See Figure 6-16	1280	micromirrors
	Number of active rows	See Figure 6-16	720	micromirrors
ε	Micromirror (pixel) pitch	See Figure 6-17	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 6-16	6.912	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 6-16	3.888	mm
	Micromirror active border	Pond of micromirror (POM)(1)	20	micromirrors/ side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

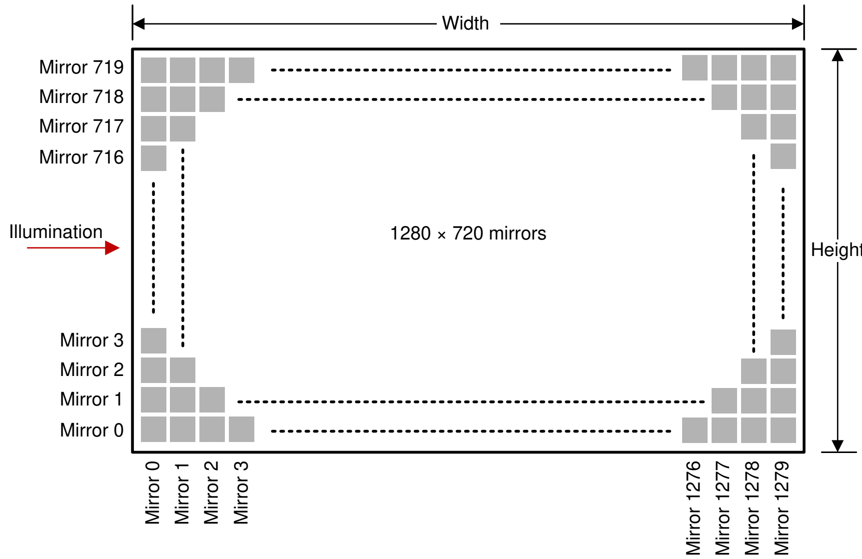


Figure 6-16. Micromirror Array Physical Characteristics

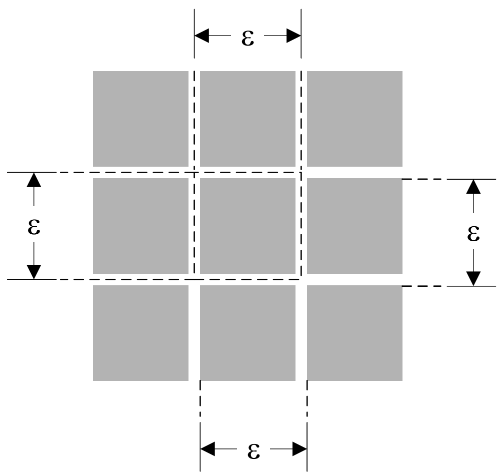


Figure 6-17. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state(1)		17		degree
Micromirror tilt angle tolerance(2) (3) (4) (5)			–1.4		1.4	degree
Micromirror tilt direction (6) (7)		Landed ON state		180		degree
		Landed OFF state		270		
Micromirror crossover time(8)		Typical performance		1	3	µs
Micromirror switching time(9)		Typical performance	10			
Image performance(10)	Bright pixel(s) in active area (11)	Gray 10 Screen (12)			0	micromirrors
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
	Dark pixel(s) in the active area (14)	White Screen			4	
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See Figure 6-18.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38 inch minimum viewing distance
The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

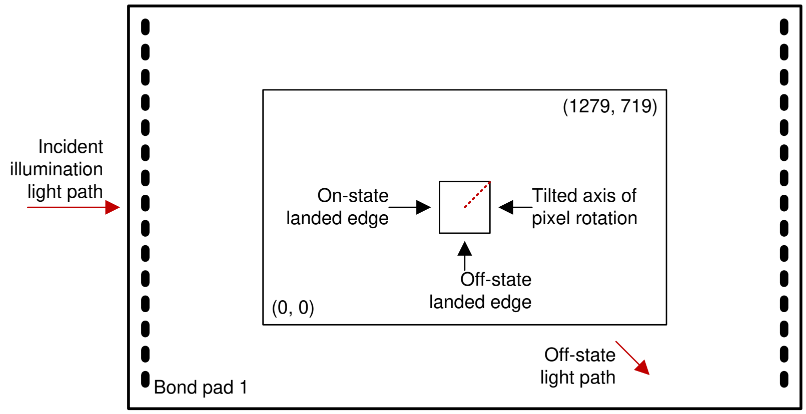


Figure 6-18. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER[3]		MIN	TYP	MAX	UNIT
Window material			Corning Eagle XG		
Window aperture[1]				See [1]	
Illumination overfill[2]				See [2]	
Window transmittance, single-pass through both surfaces and glass [4]	Minimum within the wavelength range 390 nm to 450 nm, 0-30° AOI.	93%	99%		
	Average within the wavelength range 390 nm to 450 nm, 0-30° AOI.	98%	99%		
	Minimum within the wavelength range 450 nm to 550 nm. 0-30° AOI.	75%	90%		

(1) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(2) The active area of the DLP301S device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.
(3) See Section 7.5 for more information.
(4) See the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP DMD Window*.

6.13 Chipset Component Usage Specification

The DLP301S is a component of one or more TI DLP® chipsets. Reliable function and operation of the DLP301S requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6.14 Software Requirements

CAUTION

The DLP301S DMD has mandatory software requirements. Refer to *Software Requirements for TI DLP®Pico® TRP Digital Micromirror Devices* application report for additional information. Failure to use the specified software will result in failure at power up.

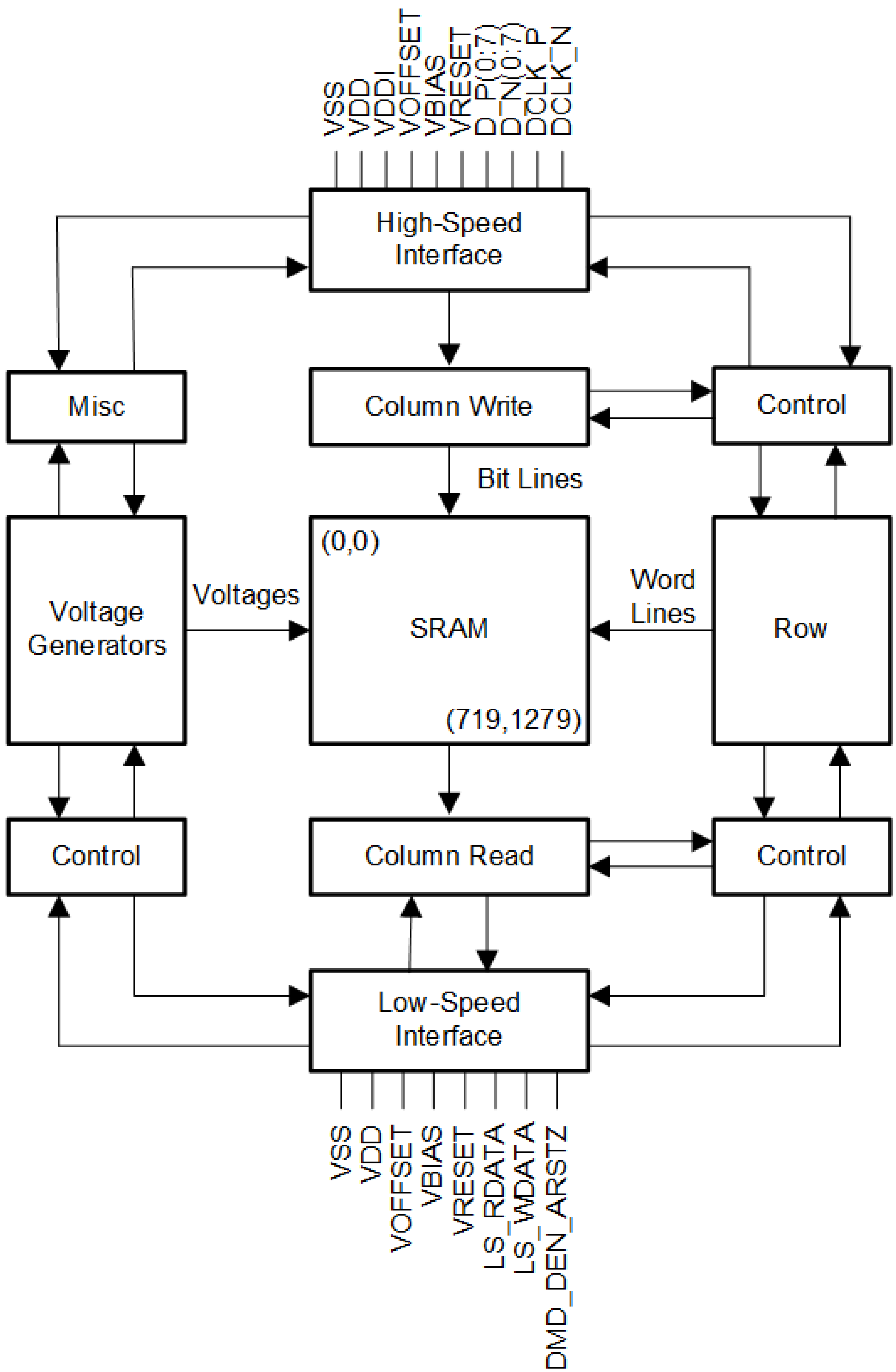
7 Detailed Description

7.1 Overview

The DLP301S DMD is a 0.3 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1280 columns by 720 rows in a square grid pixel arrangement. The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enable each micromirror to display 4 distinct pixels on the resin during every frame, resulting in a full 3.6MP image being projected upon the resin. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

This DMD is part of the chipset that includes the DLP301S DMD, DLPC1438 display and light controller and DLPA200x/DLPA300x PMIC/LED driver. To ensure reliable operation, this DMD must always be used with DLPC1438 display and light controller and DLPA200x/DLPA300x PMIC/LED driver.

7.2 Functional Block Diagram



A. Details are omitted for clarity.

B. Orientation is not representative of optical system.
C. Scale is not representative of layout.

7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA200x/DLPA300x, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC1438 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing test results at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Test Load Circuit for Output Propagation Measurement shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is intended for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC1438 controller. See the DLPC1438 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area is typically the same. Ensure this angle does not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border or active area may occur.

7.5.1.2 Pupil Match

The optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The window aperture is sized to anticipate several optical operating conditions. Overfill light directly illuminating the window aperture can create adverse imaging effects, and additional device heating leading to reduced device lifetime. Direct incident illumination should be prevented from striking the DMD window aperture.

7.6 Micromirror Array Temperature Calculation

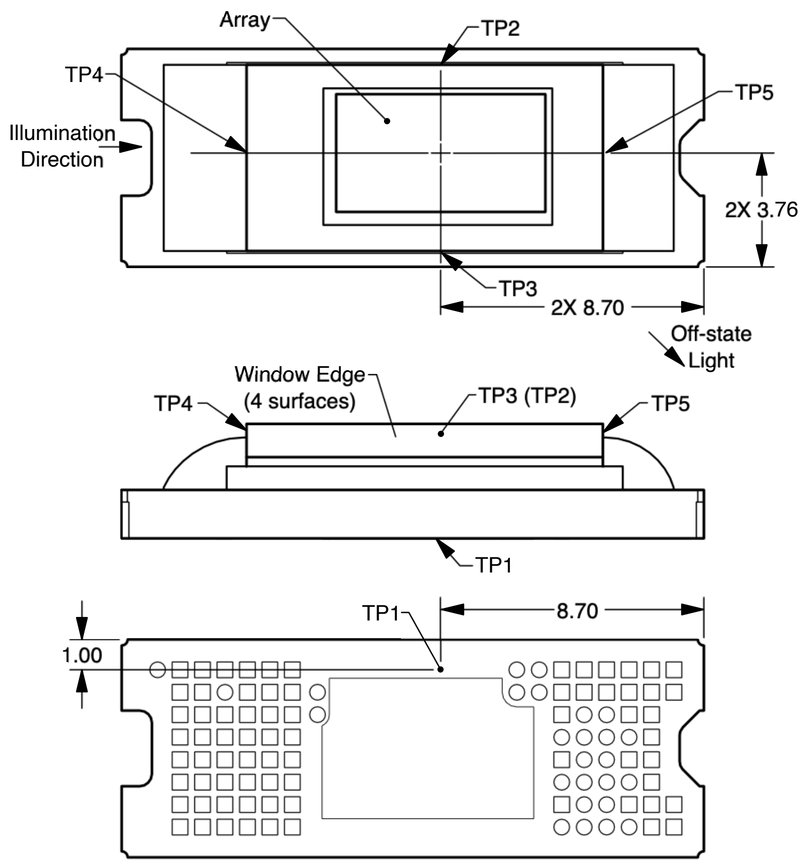


Figure 7-1. Thermal Test Point Location—FQS Package

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature shown as TP1 in Figure 7-1 is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = Computed micromirror array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in Section 6.5 from array to ceramic TP1 (°C/W)
- Q_{ARRAY} = Total DMD power on the array (electrical + absorbed) (W)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = measured total illumination optical power at DMD (W)
- $Q_{ILLUMINATION}$ = ($Q_{INCIDENT}$ × DMD average thermal absorptivity) (W)
- DMD average thermal absorptivity = 0.40

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.1 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for each DMD chip in a system. It assumes illumination distribution of 83.7% on the active array and 16.3% on the area outside the array.

$$Q_{ELECTRICAL} = 0.1\text{ W} \quad (3)$$

$$Q_{INCIDENT} = 0.9\text{ W (measured)} \quad (4)$$

$$T_{CERAMIC} = 35.0\text{ °C (measured)} \quad (5)$$

$$Q_{ARRAY} = 0.1\text{ W} + (0.9\text{ W x }0.40) = 0.46\text{ W} \quad (6)$$

$$T_{ARRAY} = 35.0\text{ °C} + (0.46\text{ W x }2.7\text{ °C /W}) = 36.2\text{°C} \quad (7)$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On and Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time), whereas 25/75 indicates that the pixel is in the OFF state 75% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

When assessing landed duty cycle, the time spent switching from the current state to the opposite state is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100. In practice, image processing algorithms in the DLP chipset can result a total of less that 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the usable life of the DMD.

The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD. This interaction can be used to reduce the impact that an asymmetrical landed duty cycle has on the useable life of the DMD.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel depends on the image content being displayed by that pixel. To enhance reliability, when coupled with the DLPC1438 controller, the DLP301S DMD operates at a maximum 78/22 duty cycle and a minimum of 22/78 duty cycle.

In the simplest case for example, when the system displays maximum full scale brightness on a given pixel for a given time period, that pixel operates very close to a 78/22 landed duty cycle during that time period. Likewise, when the system displays a pixel value of zero, the pixel operates very close to a 22/78 landed duty cycle.

The nominal landed duty cycle is additionally biased from the worst case above toward 50/50 during the time between print layers. The duty cycle approaches 50/50 when the illuminated print time is the same as the between layer time.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application depends primarily on the optical architecture of the system and format of the data coming into the DLPC1438 controller. Applications include:

- DLP 3D Printer
  - Additive manufacturing
  - Vat polymerization
  - Masked stereolithography (mSLA 3D printer)
- Light exposure: programmable spatial and temporal light exposure

DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA300x. Refer to Section 9 for power-up and power-down specifications. For reliable operation, the DLP301S DMD must be used with the DLPC1438 controller and DLPA200x/DLPA300x PMIC/LED driver.

8.2 Typical Application

Figure 8-1 and Figure 8-2 show typical DLP 3D printer system block diagrams using the DLP301S DMD, DLPC1438 controller, and DLPA200x PMIC/LED driver.

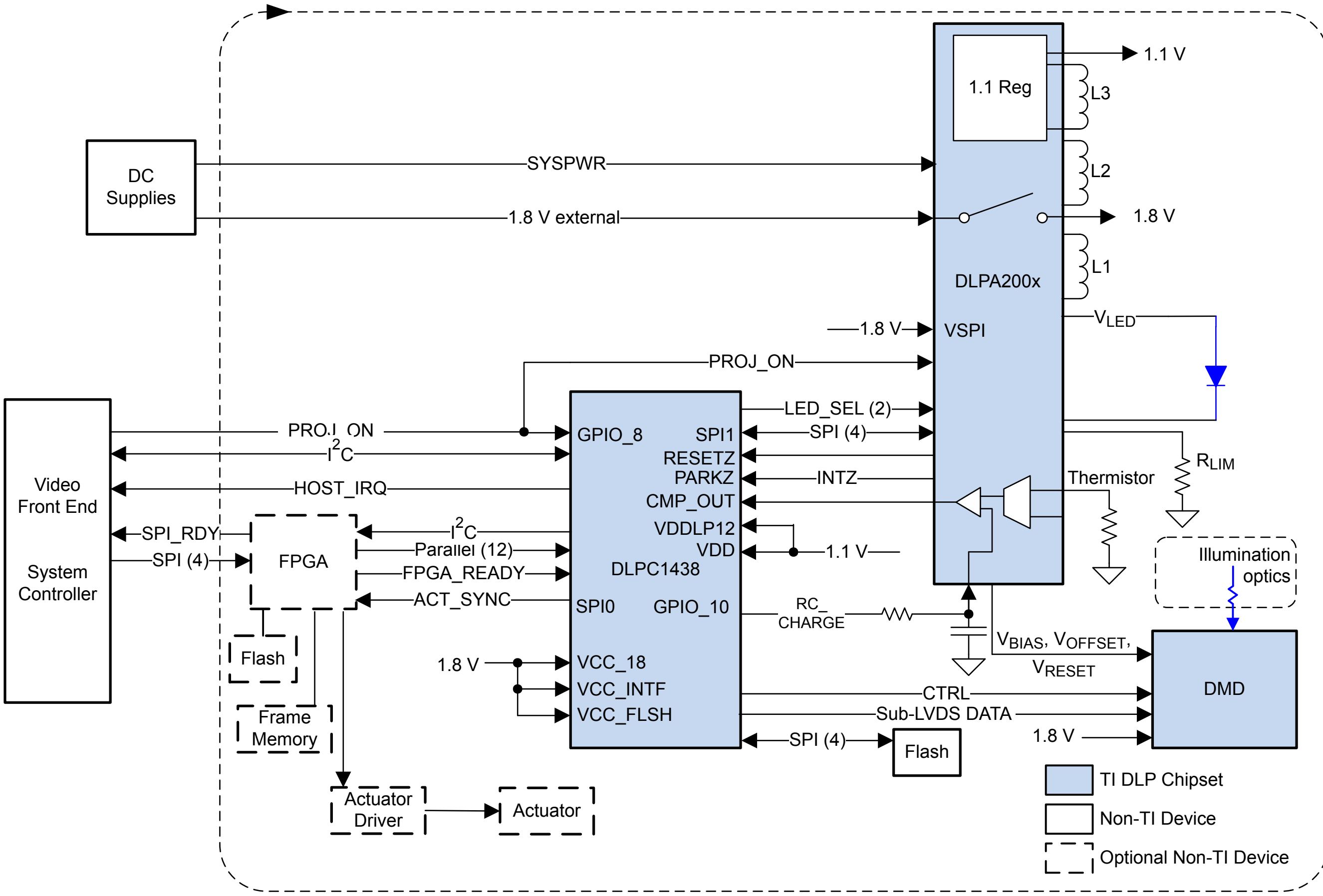


Figure 8-1. With FPGA

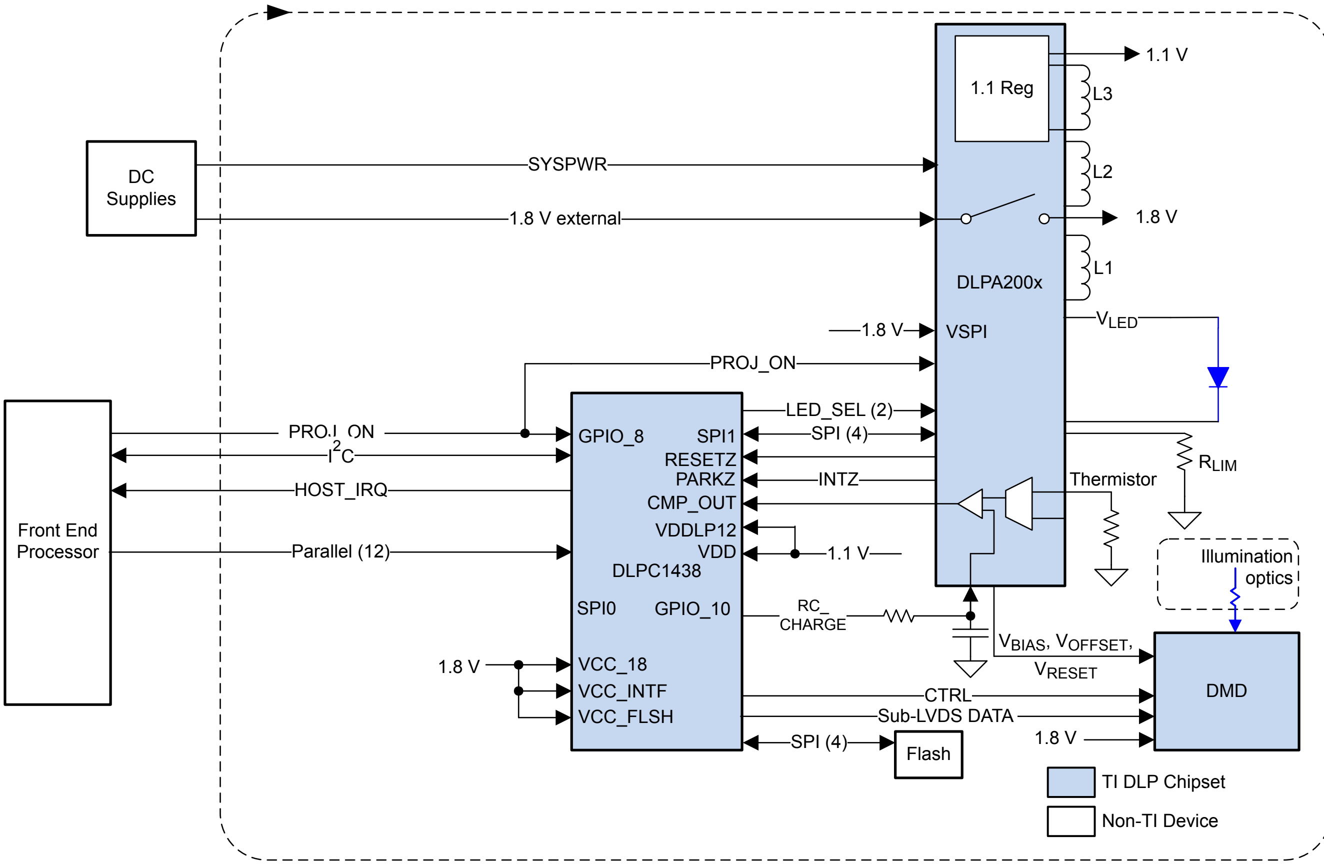


Figure 8-2. Without FPGA

8.2.1 Design Requirements

A DLP 3D printer can be created using the DLP301S, DLPC1438, and DLPA200x/DLPA300x PMIC/LED driver. In addition to the DLP chipset, other IC components may be needed including a flash device to store the software and firmware to control the DLPC1438.

A 405nm LED typically supplies the illumination for the DMD. In addition to LEDs, other light sources are supported.

8.2.2 Detailed Design Procedure

The optical engine, which includes the LED, DMD, and sometimes the electronics is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

This device drives current though the LED(s). As the LED current increases, the brightness of the optical engine increases. This increase is somewhat non-linear, and the curve for typical optical output power changes with LED currents as shown in Figure 8-3.

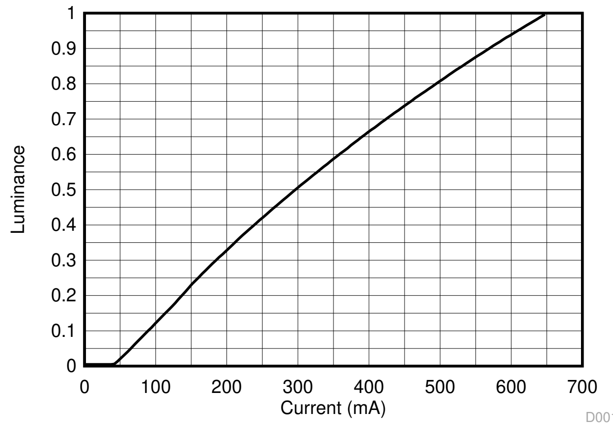


Figure 8-3. Optical Output vs LED Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDI}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLPAxxxx device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 9-1.

V_{BIAS}, V_{DD}, V_{DDI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

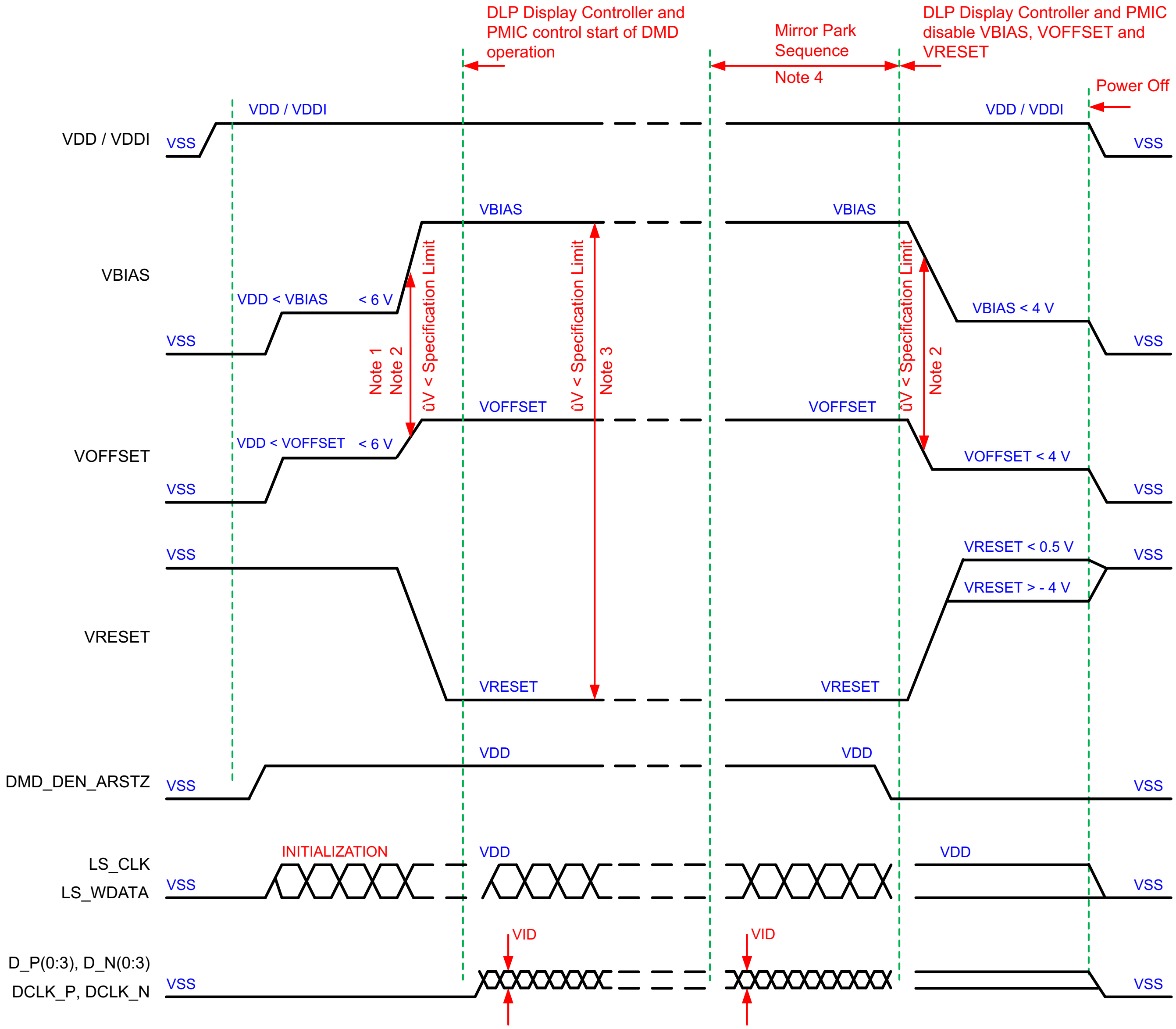
9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 6.4. Refer to Table 9-1 for power-up delay requirements.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} and V_{OFFSET}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Section 9.3.
- During power-up, LPSDR input pins must not be driven high until after V_{DD} /V_{DDI} have settled at operating voltages listed in Section 6.4.

9.2 DMD Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. During power-down, V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 6.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} and V_{OFFSET}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Section 9.3.
- During power-down, LPSDR input pins must be less than V_{DD} /V_{DDI} specified in Section 6.4.

9.3 Power Supply Sequencing Requirements



A. Refer to Table 9-1 and Figure 9-2 for critical power-up sequence delay requirements.

B. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in Section 6.4. OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down. Refer to Table 9-1 and Figure 9-2 for power-up delay requirements.

C. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than specified limit shown in Section 6.4.

D. When system power is interrupted, the ASIC driver initiates hardware power-down that disables V_{BIAS}, V_{RESET} and V_{OFFSET} after the Micromirror Park Sequence. Software power-down disables V_{BIAS}, V_{RESET}, and V_{OFFSET} after the Micromirror Park Sequence through software control.

E. Drawing is not to scale and details are omitted for clarity.

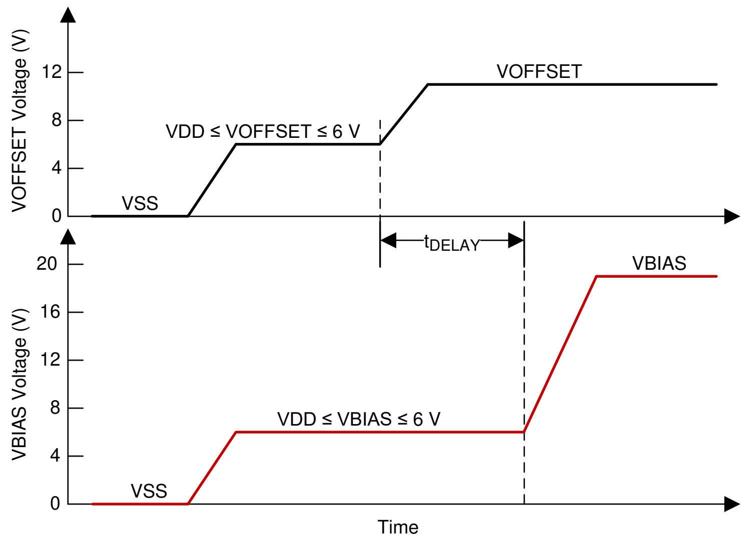
Figure 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

Table 9-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from V_{OFFSET} power up to V_{BIAS} power up	2		ms
V_{OFFSET}	Supply voltage level during power–up sequence delay (see Figure 9-2)		6	V

Table 9-1. Power-Up Sequence Delay Requirement (continued)

PARAMETER		MIN	MAX	UNIT
V_{BIAS}	Supply voltage level during power–up sequence delay (see Figure 9-2)		6	V



A. Refer to Table 9-1 for V_{OFFSET} and V_{BIAS} supply voltage levels during power-up sequence delay.

Figure 9-2. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and control signals between the DLPC1438 controller and the DLP301S DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Top Layer.
- Minimum of two 100-nF decoupling capacitor close to V_{BIAS}. Capacitor C6 and C7 in Top Layer.
- Minimum of two 100-nF decoupling capacitor close to V_{RESET}. Capacitor C9 and C8 in Top Layer.
- Minimum of two 220-nF decoupling capacitor close to V_{OFFSET}. Capacitor C5 and C4 in Top Layer.
- Minimum of four 100-nF decoupling capacitor close to V_{DDI} and V_{DD}. Capacitor C1, C2, C3 and C10 in Top Layer.

10.2 Layout Example

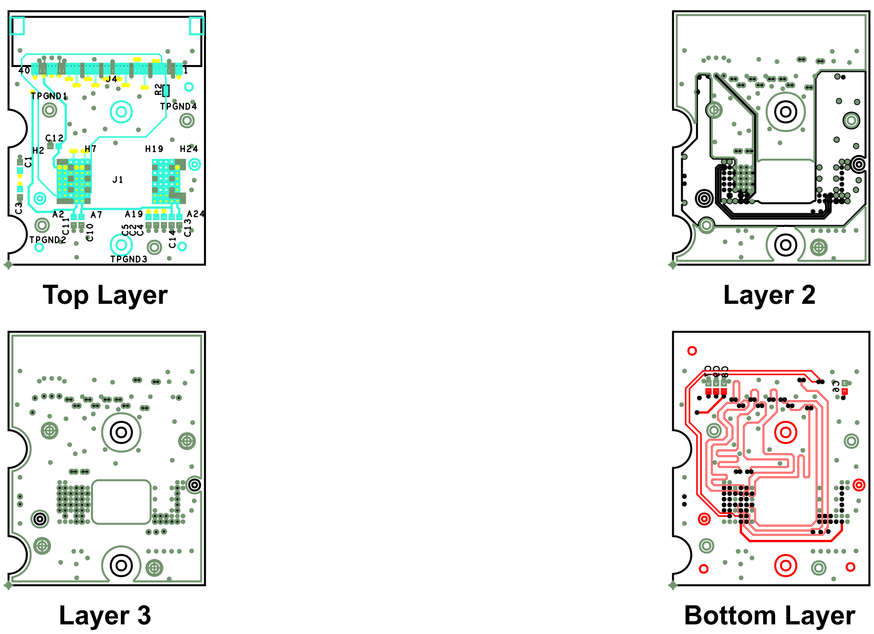


Figure 10-1. DMD Signal Routing

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

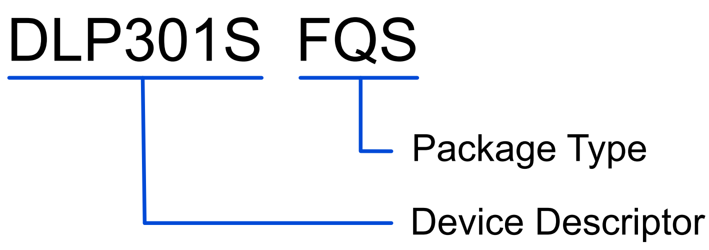

Figure 11-1. Part Number Description

11.1.3 Device Markings

The device marking includes the legible character string GHJJJJK DLP301SFQS. GHJJJJK is the lot trace code. DLP301SFQS is the orderable device number.

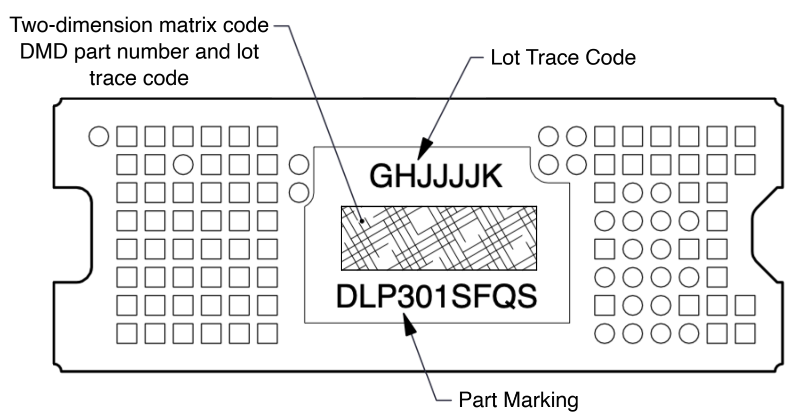

Figure 11-2. DMD Marking

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP301SFQS	Active	Production	CLGA (FQS) | 99	120 | JEDEC TRAY (5+1)	Yes	NI/AU	N/A for Pkg Type	0 to 40	
DLP301SFQS.B	Active	Production	CLGA (FQS) | 99	120 | JEDEC TRAY (5+1)	Yes	NI/AU	N/A for Pkg Type	0 to 40	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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