LM139-MIL Quad Differential Comparators

1 Features

- Wide Supply Ranges
  - Single Supply: 2 V to 36 V (Tested to 30 V)
  - Dual Supplies: ±1 V to ±18 V (Tested to ±15 V)
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA (Typical)
- Low Input Bias Current: 25 nA (Typical)
- Low Input Offset Current: 3 nA (Typical)
- Low Input Offset Voltage: 2 mV (Typical)
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Industrial
- Automotive
  - Infotainment and Clusters
  - Body Control Modules
- Power Supervision
- Oscillators
- Peak Detectors
- Logic Voltage Translation

3 Description

The LM139-MIL device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible, as long as the difference between the two supplies is 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

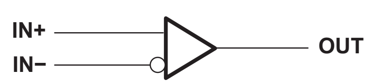
The LM139-MIL device is characterized for operation over the full military temperature range of –55°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM139-MIL	CDIP (14)	21.30 mm × 7.60 mm
	LCCC (20)	8.90 mm × 8.90 mm
	CFP (14)	9.20 mm × 6.29 mm
	SOIC (14)	8.70 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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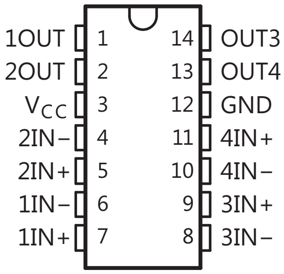
4 Revision History

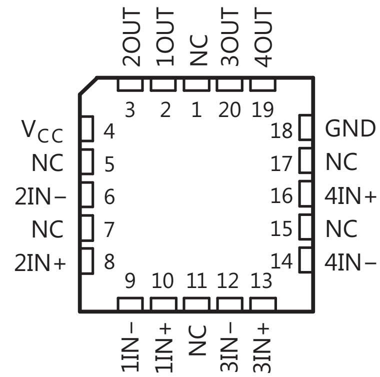
DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

D, J, or W Package
SOIC, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



NC = no internal connection.

Pin Functions

PIN			I/O (1)	DESCRIPTION
NAME	D, J, W	FK		
1IN+	7	10	I	Positive input pin of the comparator 1
1IN–	6	9	I	Negative input pin of the comparator 1
1OUT	1	2	O	Output pin of the comparator 1
2IN+	5	8	I	Positive input pin of the comparator 2
2IN–	4	6	I	Negative input pin of the comparator 2
2OUT	2	3	O	Output pin of the comparator 2
3IN+	9	13	I	Positive input pin of the comparator 3
3IN–	8	12	I	Negative input pin of the comparator 3
3OUT	14	20	O	Output pin of the comparator 3
4IN+	11	16	I	Positive input pin of the comparator 4
4IN–	10	14	I	Negative input pin of the comparator 4
4OUT	13	19	O	Output pin of the comparator 4
GND	12	18	—	Ground
V_{CC}	3	4	—	Supply pin
NC	—	1	—	No connect (no internal connection)
		5		
		7		
		11		
		15		
		17		

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			36	V
V_{ID}	Differential input voltage(3)			±36	V
V_I	Input voltage range (either input)		–0.3	36	V
I_K	Input current(4)			–50	mA
V_O	Output voltage			36	V
I_O	Output current			20	mA
	Duration of output short circuit to ground(5)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1.6 mm (1/16 in) from case for 60 s	J package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at xIN+ with respect to xIN–.
(4) Input current flows through parasitic diode to ground and will turn on parasitic transistors that will increase I_{CC} and may cause output to be incorrect. Normal operation resumes when input is removed.
(5) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	30	V
T_J	Junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM139-MIL				UNIT
		D (SOIC)	J (CDIP)	W (CFP)	FK (LCCC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.8	89.5	156.2	82.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	46.1	86.7	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.7	78.7	154.6	59.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.7	3	56.5	53	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.3	71.8	133.5	58.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	24.2	14.3	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[(1)]			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		T_A = 25°C		2	5	mV
				T_A = –55°C to +125°C			9	
I_{IO}	Input offset current	V_O = 1.4 V		T_A = 25°C		3	25	nA
				T_A = –55°C to +125°C			100	
I_{IB}	Input bias current	V_O = 1.4 V		T_A = 25°C		–25	–100	nA
				T_A = –55°C to +125°C			–300	
V_{ICR}	Common-mode input-voltage range[(2)]			T_A = 25°C	0 to V_{CC} – 1.5			V
				T_A = –55°C to +125°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC+} = ±7.5 V, V_O = –5 V to +5 V		T_A = 25°C		200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	T_A = 25°C		0.1		nA
			V_{OH} = 30 V	T_A = –55°C to +125°C			1	μA
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 4 mA	T_A = 25°C		150	400	mV
				T_A = –55°C to +125°C			700	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	T_A = 25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	T_A = 25°C		0.8	2	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V; however, one input can exceed V_{CC}, and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF[(1)(2)]	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.7 Typical Characteristics

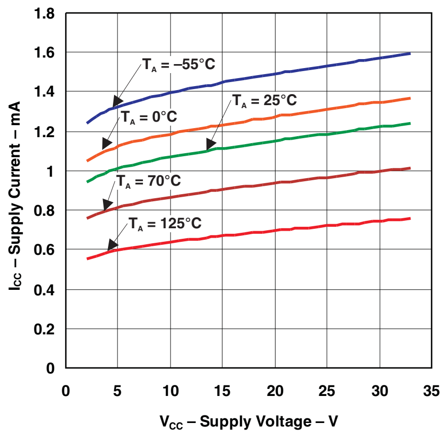


Figure 1. Supply Current vs Supply Voltage

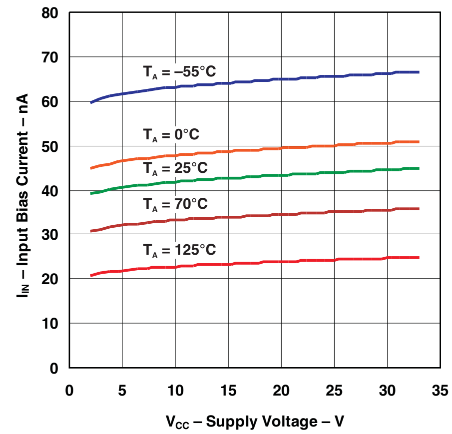


Figure 2. Input Bias Current vs Supply Voltage

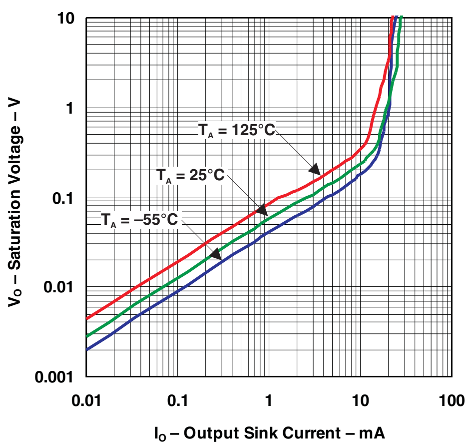


Figure 3. Output Saturation Voltage

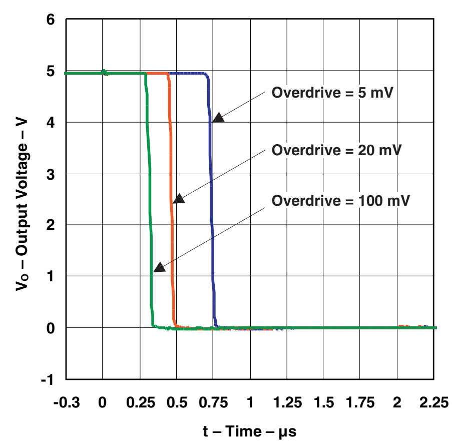


Figure 4. Response Time for Various Overdrives Negative Transition

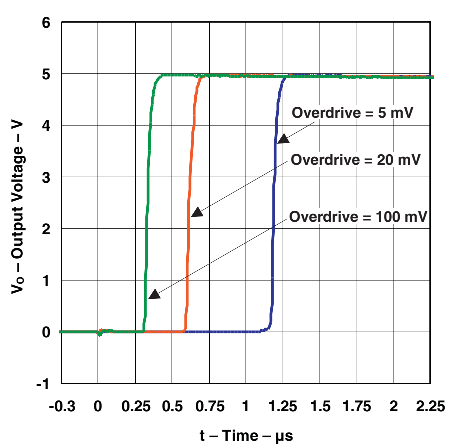


Figure 5. Response Time for Various Overdrives Positive Transition

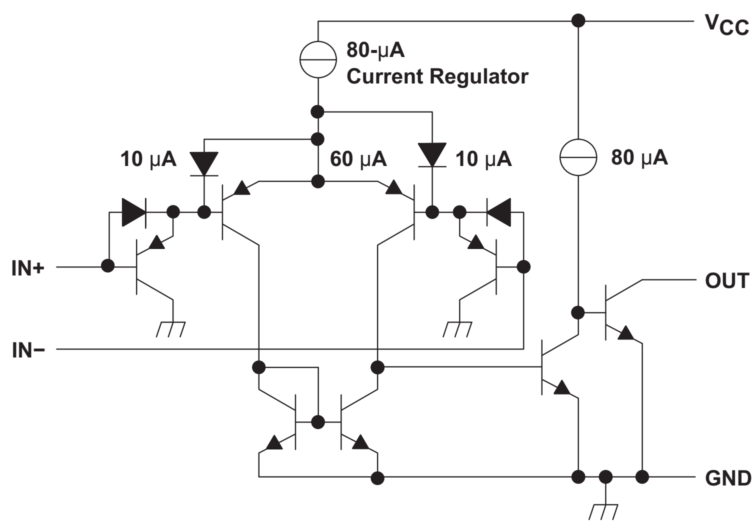
7 Detailed Description

7.1 Overview

The LM139-MIL is a quad comparators with the ability to operate up to an absolute maximum of 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V up to 32 V), low Iq, and fast response of the device.

The open-drain output allows the user to configure the output logic low voltage (V_{OL}) and allows the comparator to be used in AND functionality.

7.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

Figure 6. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage capability, allowing the comparator to accurately function from ground to (V_{CC} – 1.5 V) differential input. Allow for (V_{CC} – 2 V) at cold temperature.

The output consists of an open-collector NPN (pulldown or low-side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and scales with the output current. See the *Specifications* section for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

8.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two different signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes the LM139-MIL device optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

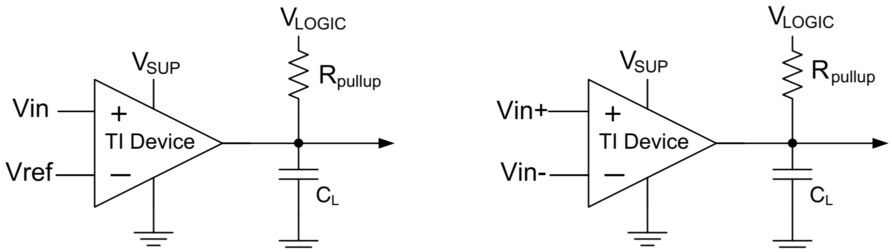


Figure 7. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 µA to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using the LM139-MIL in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common-mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2 V. This limits the input voltage range to as high as V_{CC}– 2 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
  - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
  - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 8 and Figure 9 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

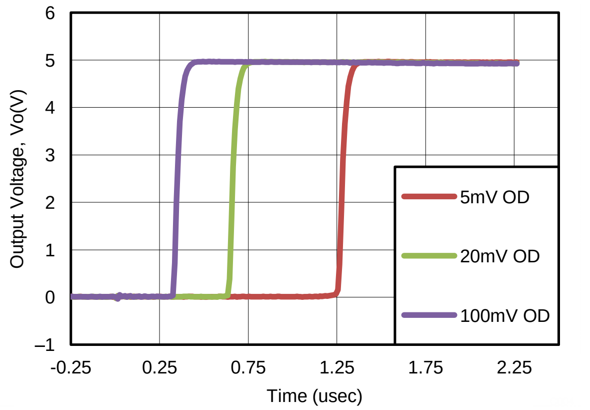
8.2.2.4 Response Time

Response time is a function of input over-drive. See the *Typical Characteristics* graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  - R_{CE} can be determined by taking the slope of Figure 3 in its linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

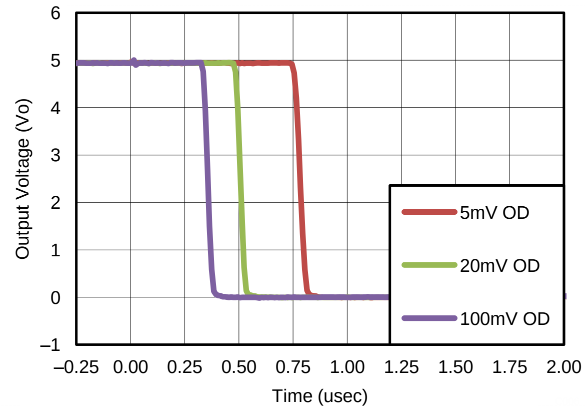
8.2.3 Application Curves

Figure 8 and Figure 9 were generated with scope probe parasitic capacitance of 50 pF.



V_{CC} = 5 V V_{Logic} = 5 V R_{PULLUP} = 5.1 kΩ

Figure 8. Response Time vs Output Voltage (Positive Transition)



V_{CC} = 5 V V_{Logic} = 5 V R_{PULLUP} = 5.1 kΩ

Figure 9. Response Time vs Output Voltage (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

NOTE

If a negative supply is not being used, do not place a capacitor between the GND pin of the device and system ground.

10.2 Layout Example

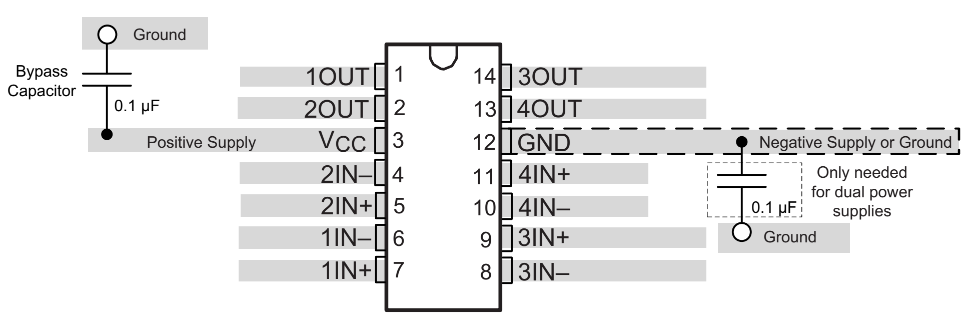


Figure 10. LM139-MIL Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
77008012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77008012A LM139FKB
7700801CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801CA LM139JB
7700801DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801DA LM139WB
JM38510/11201BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11201BCA
JM38510/11201BCA.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11201BCA
LM139FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139FK
LM139FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139FK
LM139FKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77008012A LM139FKB
LM139FKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	77008012A LM139FKB
LM139J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139J
LM139J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139J
LM139JB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801CA LM139JB
LM139JB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801CA LM139JB
LM139W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139W
LM139W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LM139W
LM139WB	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801DA LM139WB
LM139WB.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700801DA LM139WB
M38510/11201BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11201BCA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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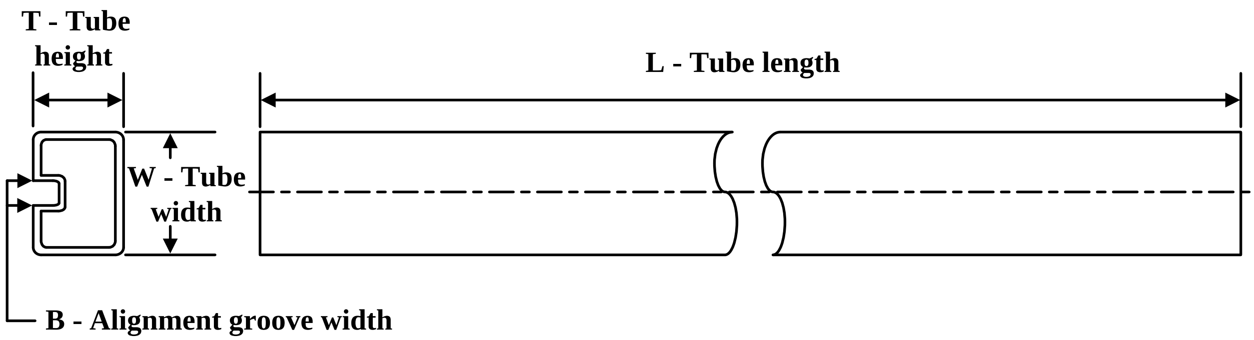
OTHER QUALIFIED VERSIONS OF LM139-MIL :

- Space : LM139-SP

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

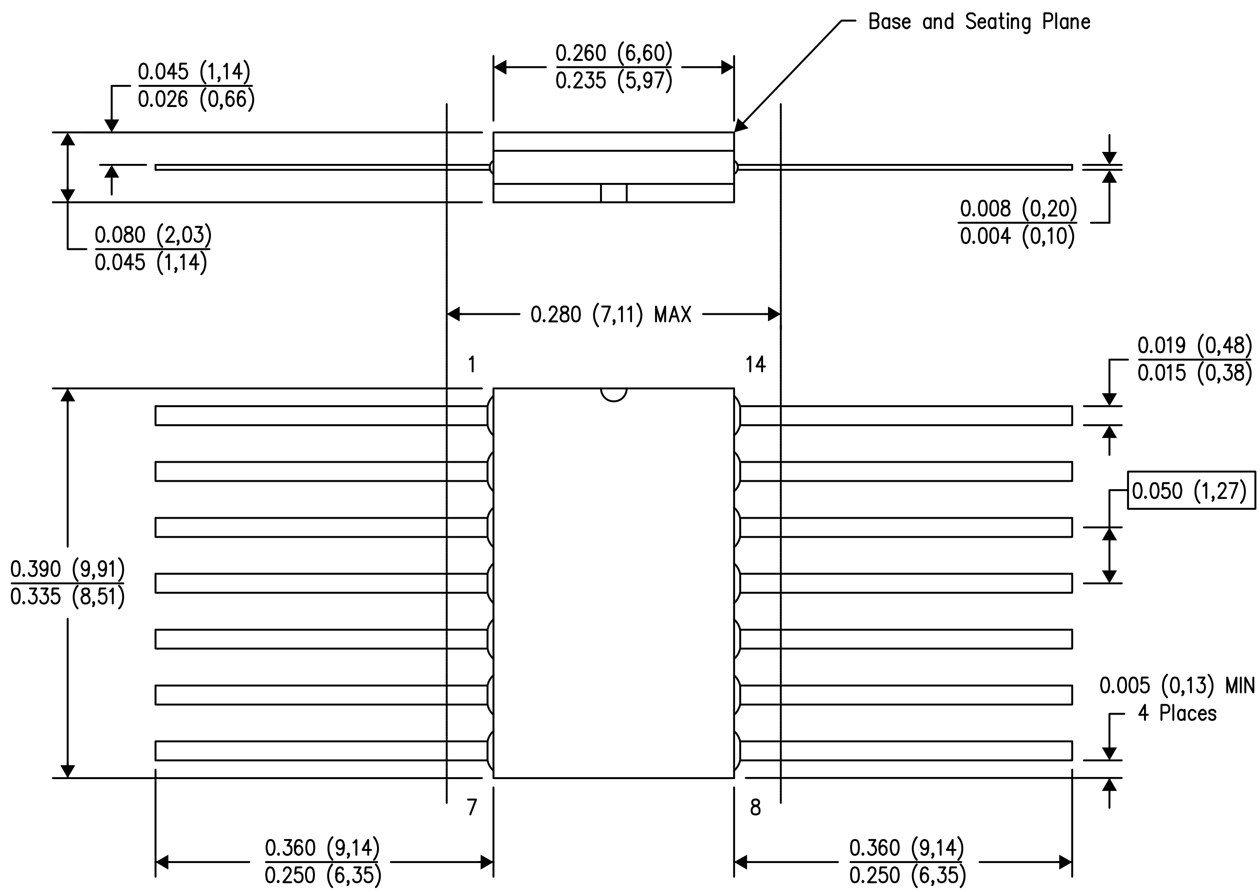
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
77008012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7700801DA	W	CFP	14	25	506.98	26.16	6220	NA
LM139FK	FK	LCCC	20	55	506.98	12.06	2030	NA
LM139FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
LM139FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM139FKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
LM139W	W	CFP	14	25	506.98	26.16	6220	NA
LM139W.A	W	CFP	14	25	506.98	26.16	6220	NA
LM139WB	W	CFP	14	25	506.98	26.16	6220	NA
LM139WB.A	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



4040180–2/F 04/14

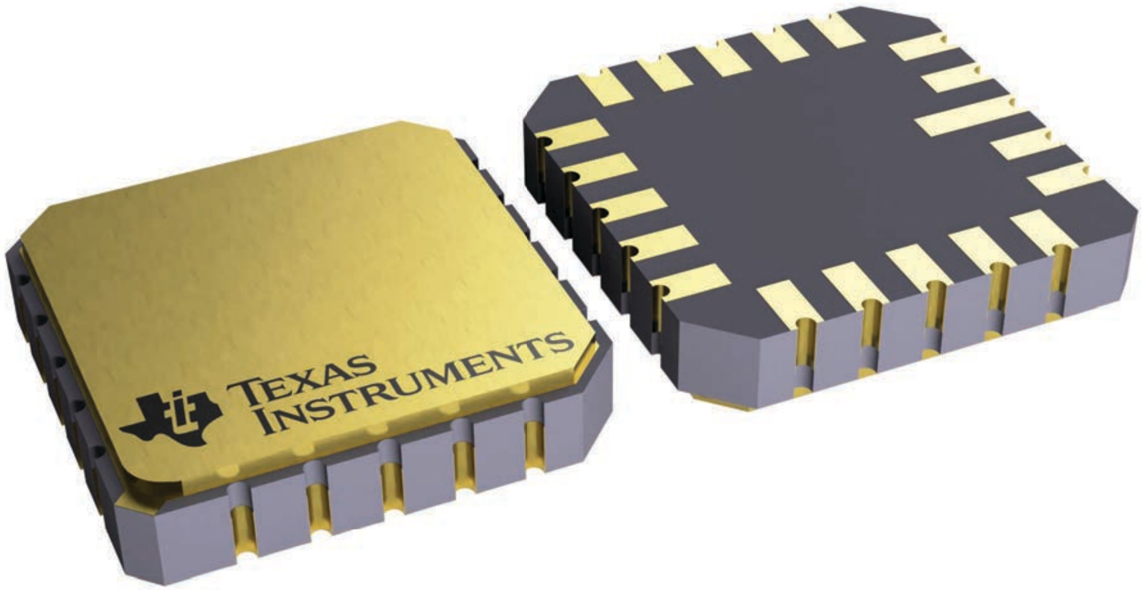
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

FK 20 **LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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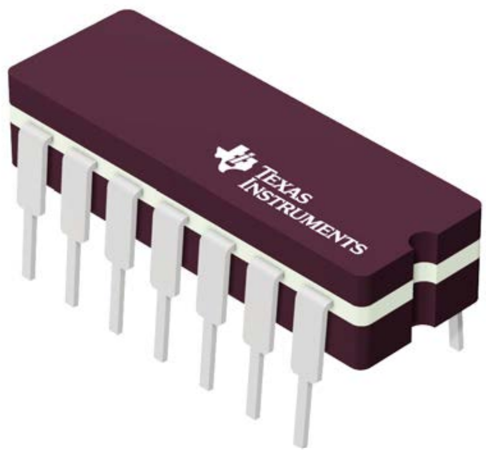
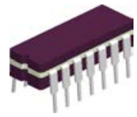
J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

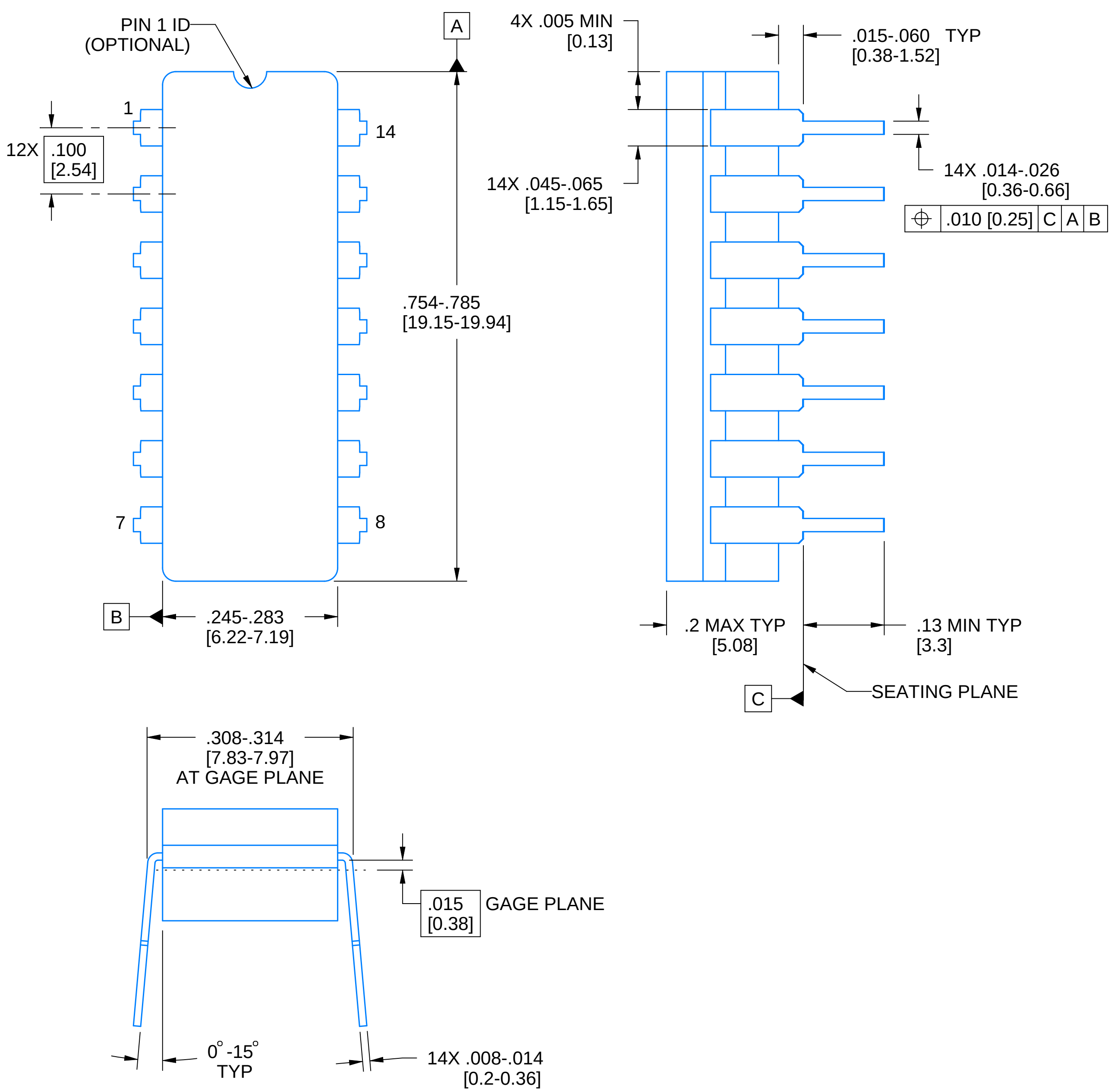


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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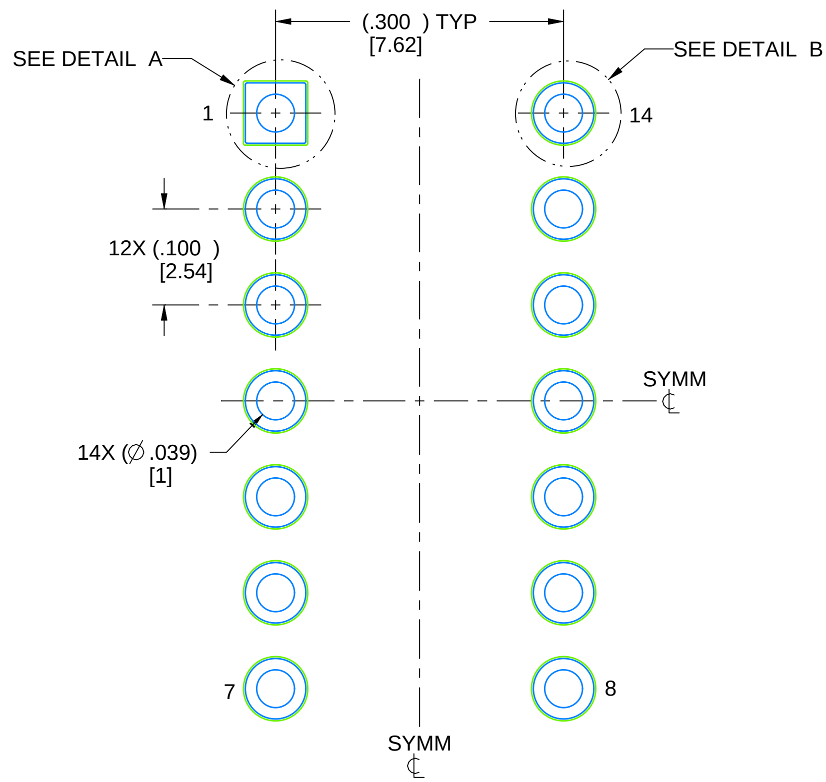
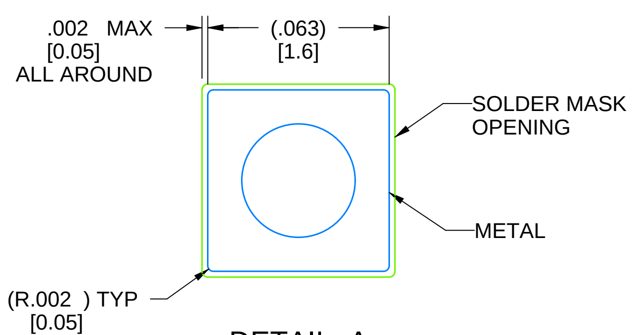
NOTES:

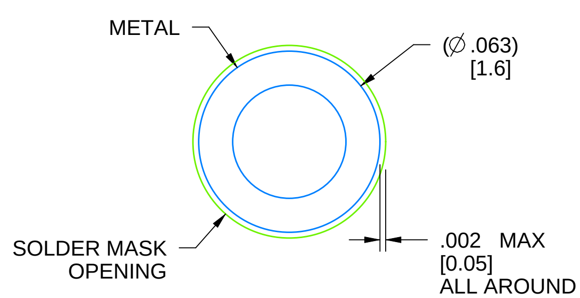
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

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