

Single, Dual, and Quad 40V Low Noise Precision Amplifiers

Check for Samples: [LMP8671](#), [LMP8672](#), [LMP8674](#)

FEATURES

- Output Short Circuit Protection
- PSRR and CMRR Exceed 110dB
- Best in Class Linearity (135dB)

APPLICATIONS

- Low Noise Industrial Applications Including Test, Measurement, and Ultrasound
- Precision Active Filters
- PLL Filters
- 4-20mA Current Loops
- Motor Control

KEY SPECIFICATIONS

- Input Offset Voltage 0.4mV
- TC V_{OS} 2 μ V/°C (max)
- Power Supply Voltage Range ± 2.5 V to ± 20 V
- Voltage Noise Density 2.5nV/ $\sqrt{\text{Hz}}$
- Slew Rate ± 20 V/ μ s
- Gain Bandwidth Product 55MHz
- Open Loop Gain 135dB
- Input Bias Current 10nA

Connection Diagrams

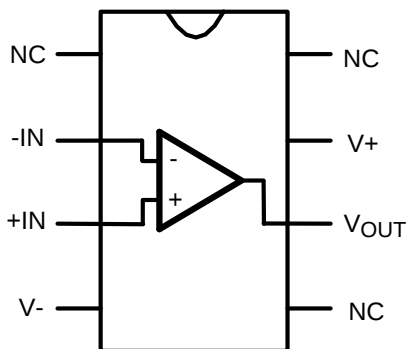


Figure 1. See Package Number — D0008A

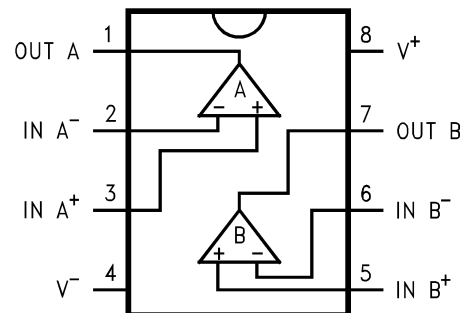


Figure 2. See Package Number — D0008A



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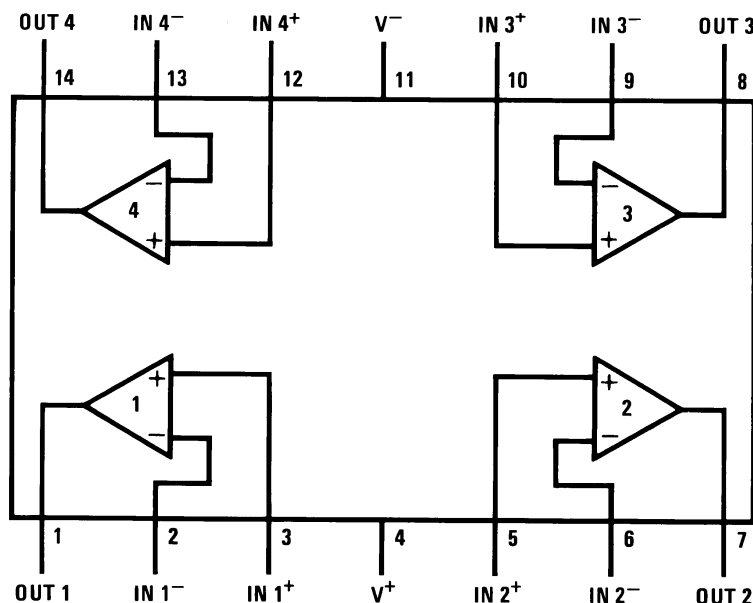


Figure 3. See Package Number — D0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Power Supply Voltage ($V_S = V^+ - V^-$)		46V
Storage Temperature		-65°C to 150°C
Input Voltage		(V^-) - 0.7V to (V^+) + 0.7V
Output Short Circuit ⁽⁴⁾		Continuous
Power Dissipation		Internally Limited
ESD Rating ⁽⁵⁾		2000V
ESD Rating ⁽⁶⁾	Pins 1, 4, 7 and 8	200V
	Pins 2, 3, 5 and 6	100V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (SO)	145°C/W
For soldering specifications, http://www.ti.com/lit/SNOA549		

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ 125°C
Supply Voltage Range LMP8671/2/4	$\pm 2.5V \leq V_S \leq \pm 22V$

Electrical Characteristics for the LMP8671/2/4⁽¹⁾

The following specifications apply for $V_S = \pm 20V$, $R_L = 2k\Omega$, $R_{SOURCE} = 10\Omega$, $f_{IN} = 1kHz$, $T_A = 25^\circ C$, unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LMP8671/2/4		Units (Limits)
			Typical ⁽²⁾	Limit ⁽³⁾	
V_{OS}	Offset Voltage		± 100	± 400 ± 750	μV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	$-40^\circ C \leq T_A \leq 125^\circ C$	0.1	2	$\mu V/^\circ C$ (max)
I_B	Input Bias Current	$V_{CM} = 0V$			
		LMP8671/4	10	± 75 ± 95	nA (max)
		$V_{CM} = 0V$			
		LMP8672	50	± 200 ± 250	nA (max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$			
		LMP8671/4	11	± 50 ± 95	nA (max)
		$V_{CM} = 0V$			
		LMP8672	25	± 100 ± 125	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	$-40^\circ C \leq T_A \leq 125^\circ C$	0.2		nA/ $^\circ C$
V_{IN-CM}	Common-Mode Input Voltage Range		+17.1 –16.9		V (min) V (min)
Z_{IN}	Differential Input Impedance		30		k Ω
	Common Mode Input Impedance	$-10V < V_{cm} < 10V$	1000		M Ω
e_n	Equivalent Input Noise Voltage	20Hz to 20kHz	0.34	0.65	μV_{RMS} (max)
	Equivalent Input Noise Density	$f = 1kHz$	2.5	4.7	nV/ $\sqrt{Hz}$ (max)
i_n	Current Noise Density	$f = 1kHz$	1.6		pA/ $\sqrt{Hz}$
		$f = 10Hz$	3.1		
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$, $V_{OUT} = 3V_{rms}$, $R_L = 600\Omega$	0.00003	0.00009	% (max)
t_S	Settling time	$A_V = -1$, 10V step, $C_L = 100pF$ 0.1% error range	1.2		μs
GBWP	Gain Bandwidth Product		55	45	MHz (min)
SR	Slew Rate		± 20	± 15	V/ μs (min)
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	See ⁽⁴⁾	125	110 100	dB (min)
CMRR	Common-Mode Rejection	$-15V \leq V_{cm} \leq 15V$	115	105 100	dB (min)
A_{VOL}	Open Loop Voltage Gain	$-15V \leq V_{out} \leq 15V$ $R_L = 2k\Omega$	135	125	dB (min)
V_{OUTMAX}	Maximum Output Voltage Swing	$R_L = 2k\Omega$	± 19.0	± 18.8 ± 18.6	V (min)
I_{OUT-CC}	Instantaneous Short Circuit Current		+53 –42		mA

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(3) Datasheet min/max specification limits are ensured by test or statistical analysis.

(4) PSRR is measured as follows: For V_S , V_{OS} is measured at two supply voltages, $\pm 5V$ and $\pm 20V$, $PSRR = |20\log(\Delta V_{OS}/\Delta V_S)|$.

Electrical Characteristics for the LMP8671/2/4⁽¹⁾ (continued)

The following specifications apply for $V_S = \pm 20V$, $R_L = 2k\Omega$, $R_{SOURCE} = 10\Omega$, $f_{IN} = 1kHz$, $T_A = 25^\circ C$, unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LMP8671/2/4		Units (Limits)
			Typical ⁽²⁾	Limit ⁽³⁾	
R_{OUT}	Output Impedance	$f_{IN} = 10kHz$ Closed-Loop Open-Loop	0.01 13		Ω
I_{OUT}	Output Current	$R_L = 2k\Omega$	9.5	9.3	mA (min)
I_S	Total Quiescent Current	$I_{OUT} = 0mA$			
		LMP8671	5	6 8	mA (max)
		LMP8672	12.5	16	mA (max)
		LMP8674	20	22	mA (max)

Typical Performance Characteristics

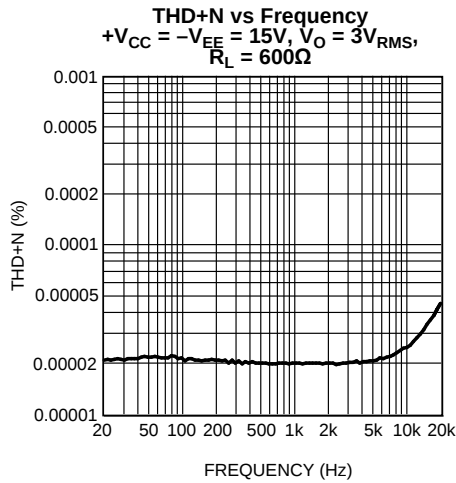


Figure 4.

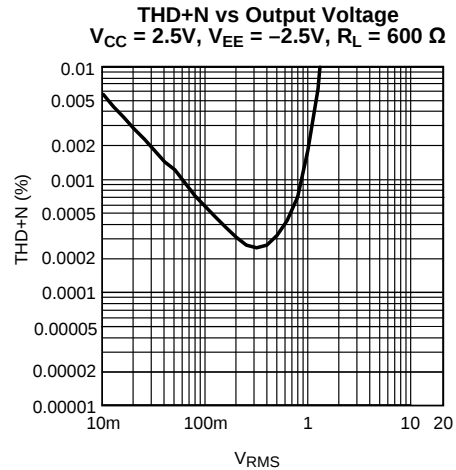


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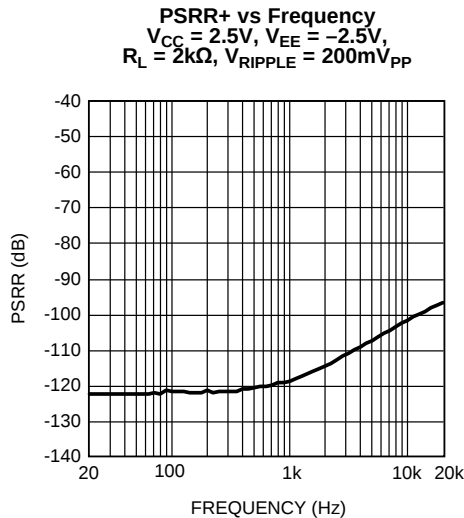


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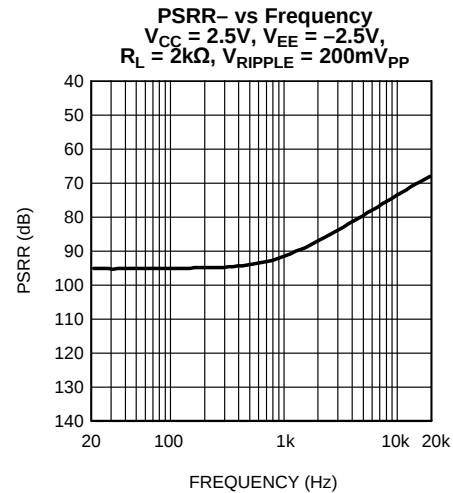


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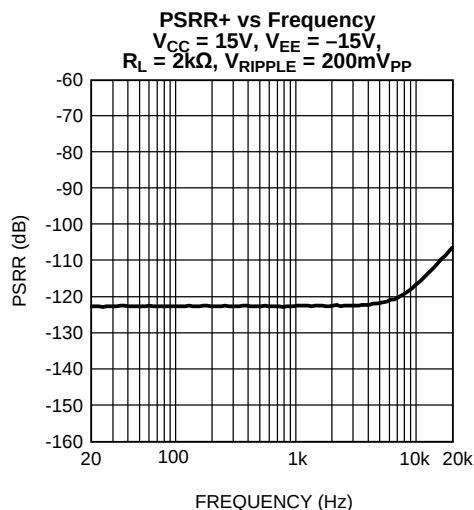


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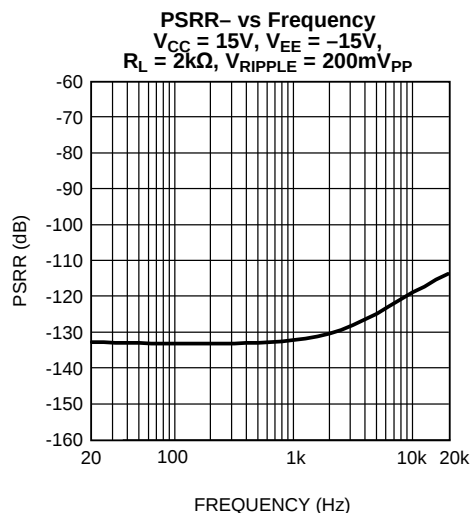


Figure 9.

Typical Performance Characteristics (continued)

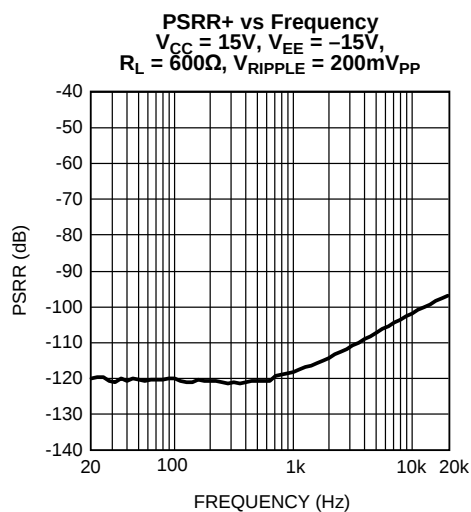


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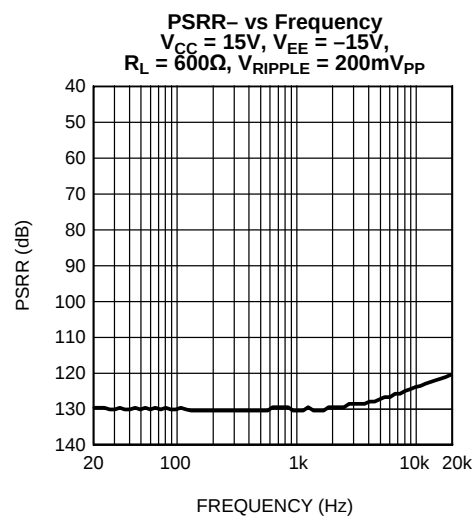


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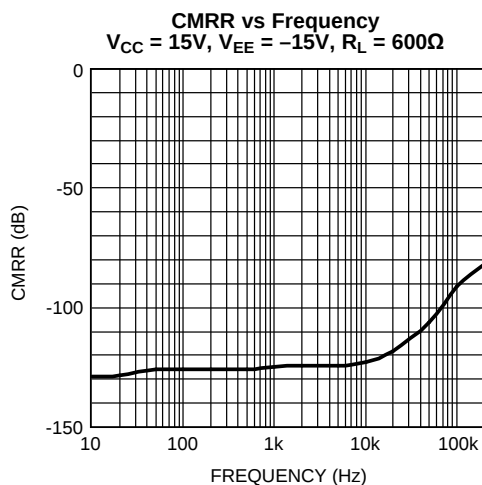


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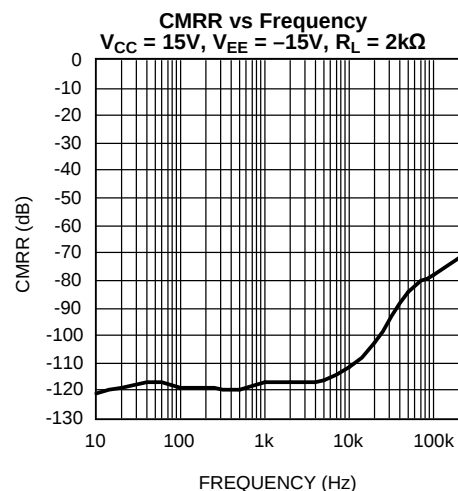


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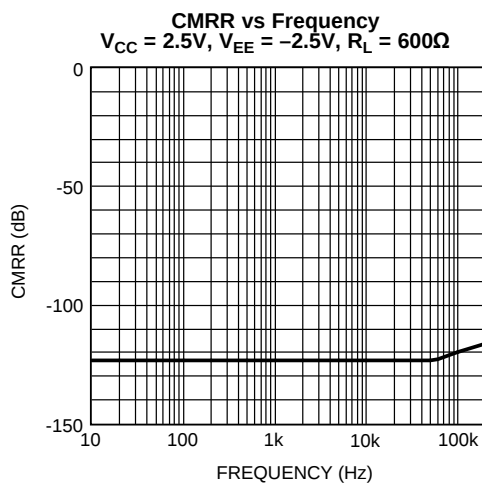


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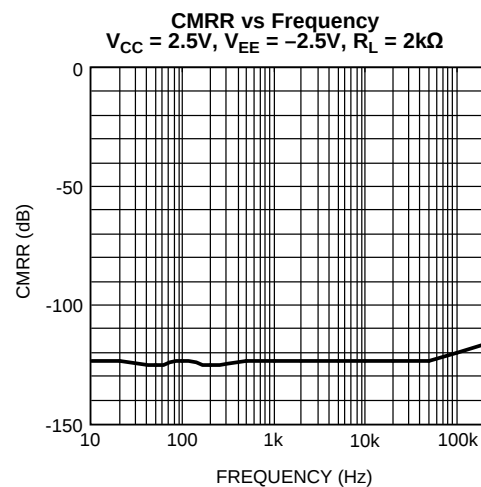


Figure 15.

Typical Performance Characteristics (continued)

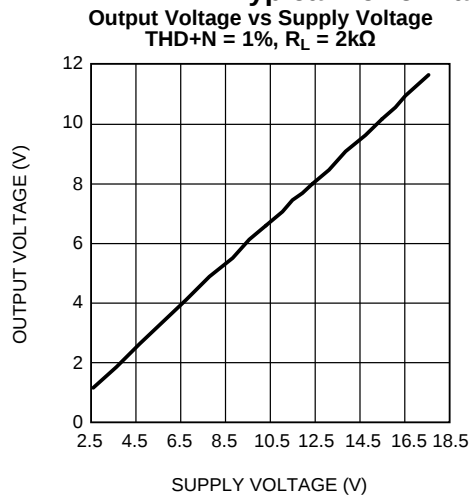


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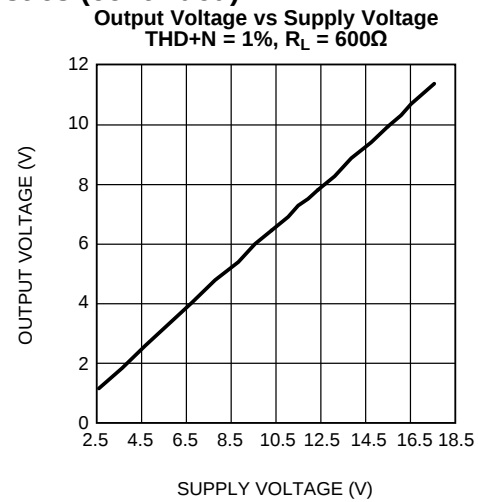


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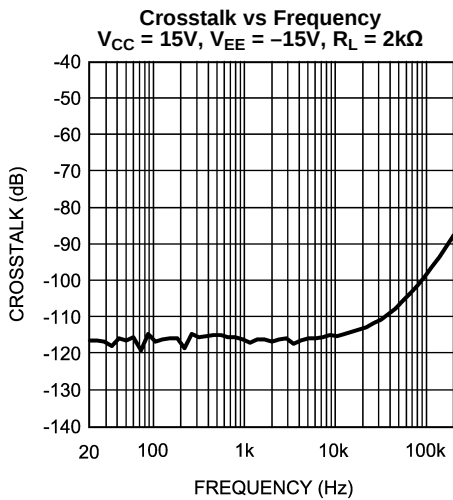


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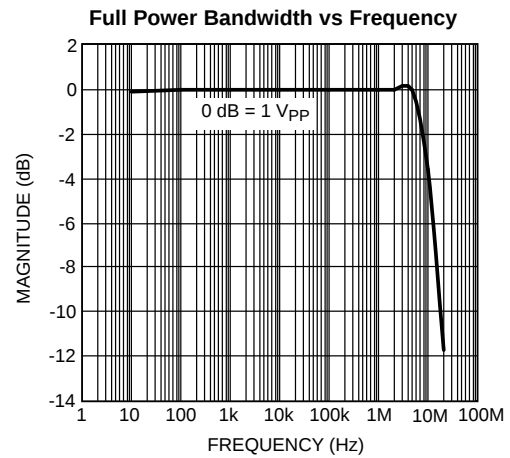


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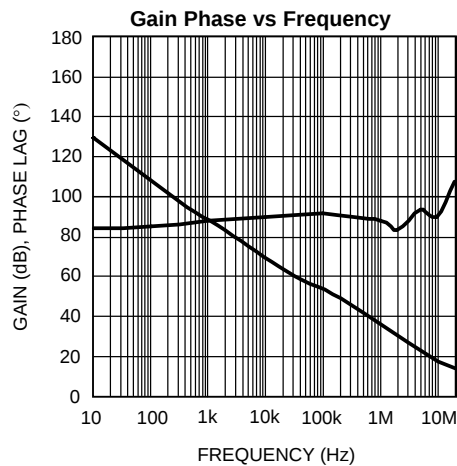


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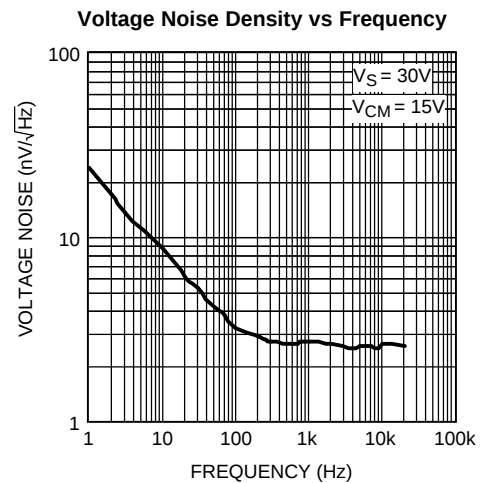


Figure 21.

Typical Performance Characteristics (continued)

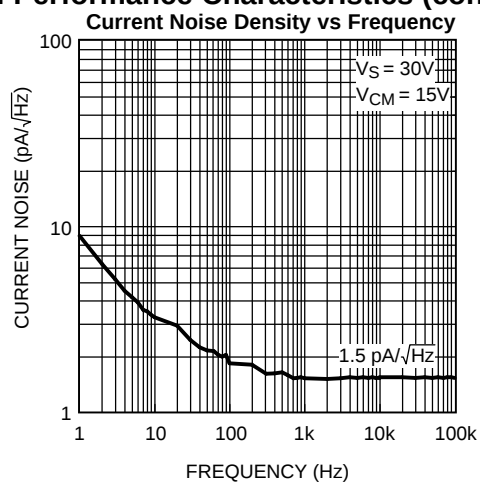


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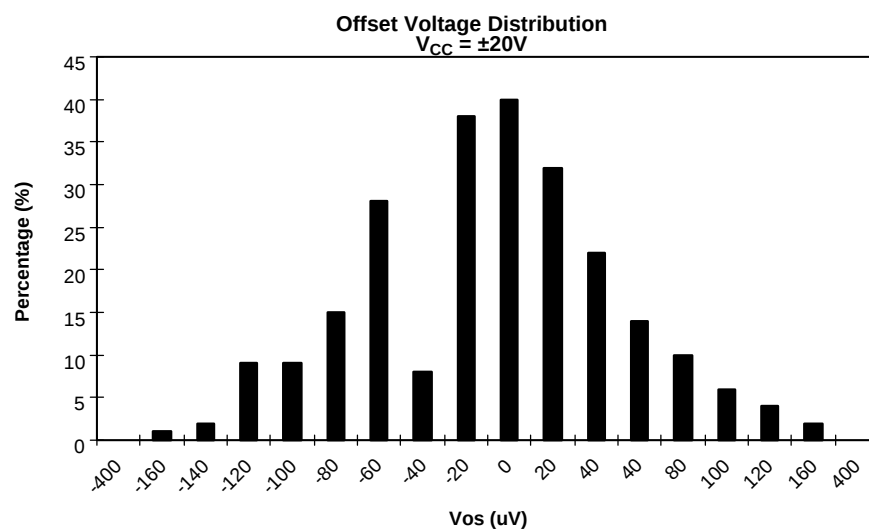


Figure 23.

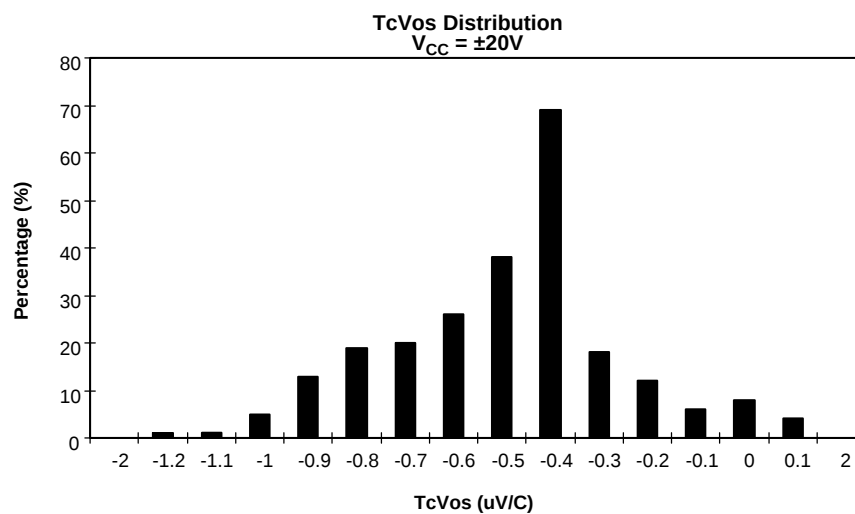


Figure 24.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B

Page

- Changed layout of National Data Sheet to TI format [8](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP8672MA/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA
LMP8672MA/NOPB.A	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA
LMP8672MA/NOPB.B	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA
LMP8672MAX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA
LMP8672MAX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA
LMP8672MAX/NOPB.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8672MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

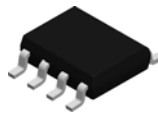
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8672MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMP8672MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP8672MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMP8672MA/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

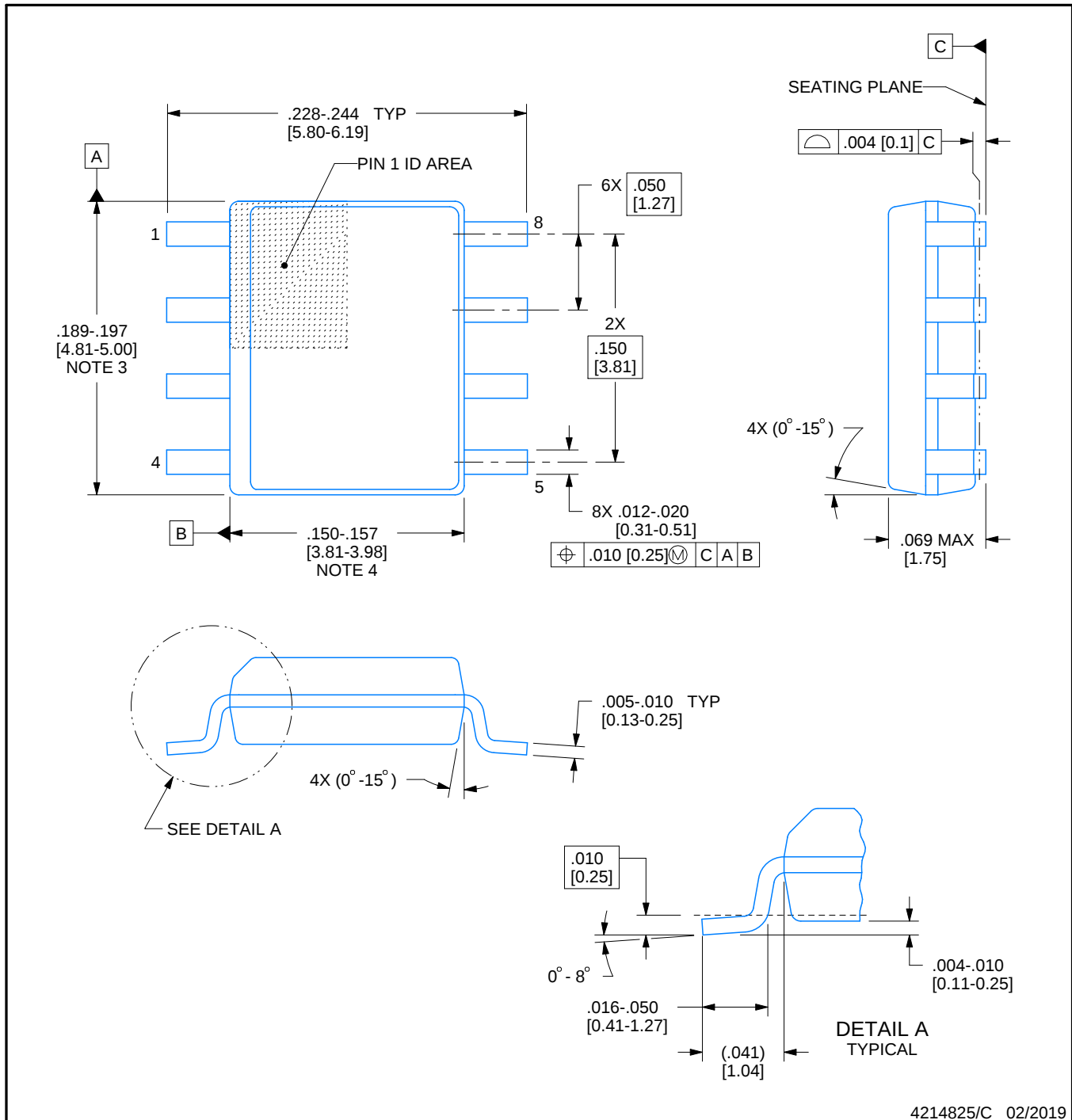


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

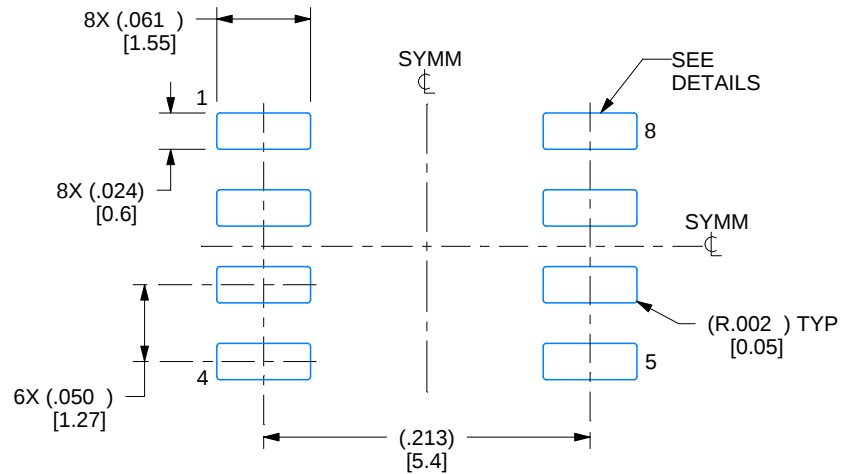
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

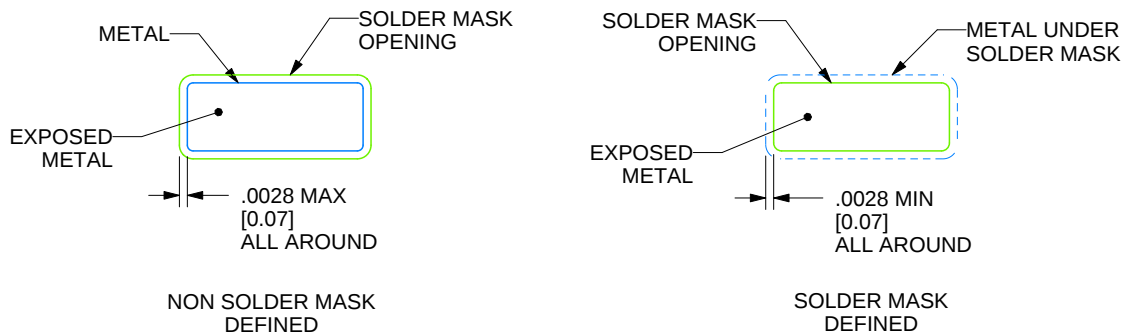
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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