

SNx4HC244 Octal Buffers and Line Drivers With 3-State Outputs

1 Features

- Wide operating voltage range of 2V to 6V
- High-current outputs drive up to 15 LSTTL loads
- 3-state outputs drive bus lines or buffer memory address registers
- Low power consumption: I_{CC} , 80 μ A (maximum)
- Typical t_{pd} = 11ns
- ± 6 mA output drive at 5V
- Low input current of 1 μ A (maximum)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

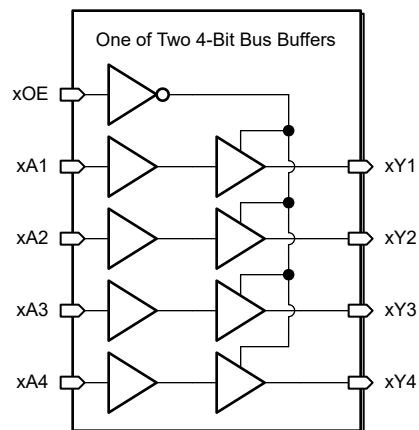
3 Description

The SNx4HC244 octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SNx4HC244 devices are organized as two 4-bit buffers and drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN54HC244	J (CDIP, 20)	24.38mm × 7.62mm	24.38mm × 6.92mm
	W (CFP, 20)	13.72mm × 8.13mm	13.72mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74HC244	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.3mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

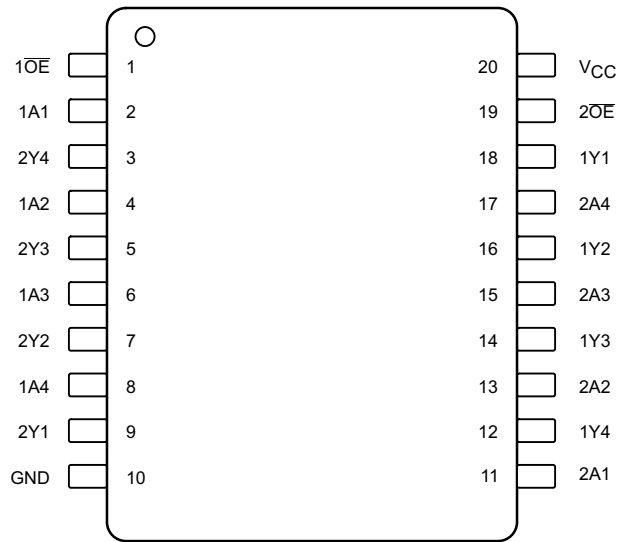


Figure 4-1. DB, DW, J, N, NS, PW, W Package 20-Pin SSOP, SOIC, CDIP, PDIP, SOP, TSSOP, or CFP Top View

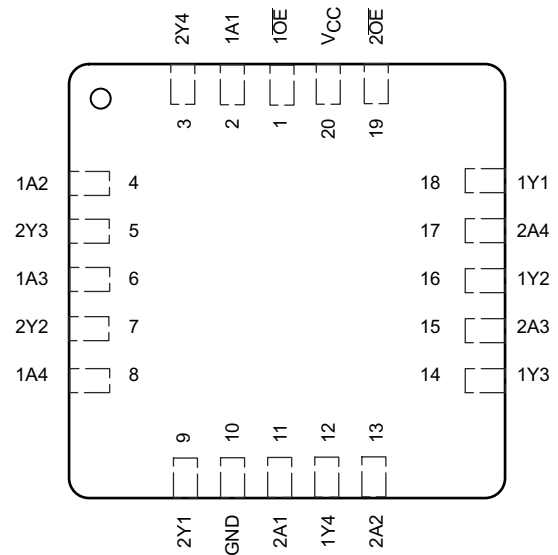


Figure 4-2. FK Package 20-Pin LCCC Top View

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable
2	1A1	I	Input
3	2Y4	O	Output
4	1A2	I	Input
5	2Y3	O	Output
6	1A3	I	Input
7	2Y2	O	Output
8	1A4	I	Input
9	2Y1	O	Output
10	GND	—	Ground
11	2A1	I	Input
12	1Y4	O	Output
13	2A2	I	Input
14	1Y3	O	Output
15	2A3	I	Input
16	1Y2	O	Output
17	2A4	I	Input
18	1Y1	O	Output
19	2 $\overline{OE}$	I	Output Enable
20	V _{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		−0.5	7	V
Input clamp current, I_{IK}	$V_I < 0$ or $V_I > V_{CC}$ ⁽²⁾		±20	mA
Output clamp current, I_{OK}	$V_O < 0$ or $V_O > V_{CC}$ ⁽²⁾		±20	mA
Continuous output current, I_O	$V_O = 0$ or V_{CC}		±35	mA
Continuous current through V_{CC} or GND			±70	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

SN74HC244		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 6\text{ V}$	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 6\text{ V}$		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	$V_{CC} = 2\text{ V}$		1000	ns/V
		$V_{CC} = 4.5\text{ V}$		500	
		$V_{CC} = 6\text{ V}$		400	
C_{pd}	Power dissipation capacitance per buffer or driver (no load)		35		pF
T_A	Operating free-air temperature	SN54HC244	−55	125	°C
		SN74HC244	−40	85	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the Texas Instruments application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC		SN74HC244					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	109.1	122.7	84.6	113.4	131.8	°C/W
$R_{\theta JC (top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = −20 μA	V _{CC} = 2 V	1.9	1.998	V	
			V _{CC} = 4.5 V	4.4	4.499		
			V _{CC} = 6 V	5.9	5.999		
		I _{OH} = −6 mA, V _{CC} = 4.5 V		3.98	4.3		
		I _{OH} = −7.8 mA, V _{CC} = 6 V		5.48	5.8		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V		0.002	0.1	V
			V _{CC} = 4.5 V		0.001	0.1	
			V _{CC} = 6 V		0.001	0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V			0.17	0.26	
		I _{OL} = 7.8 mA, V _{CC} = 6 V			0.15	0.26	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V				±0.1	±100	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V				±0.01	±0.5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					8	μA
C _i	V _{CC} = 2 V to 6 V				3	10	pF

5.6 Electrical Characteristics – SN54HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} = 2 \text{ V}$	1.9			V
			$V_{CC} = 4.5 \text{ V}$	4.4			
			$V_{CC} = 6 \text{ V}$	5.9			
		$I_{OH} = -6 \text{ mA}, V_{CC} = 4.5 \text{ V}$		3.7			
		$I_{OH} = -7.8 \text{ mA}, V_{CC} = 6 \text{ V}$		5.2			

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V			0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 6 V			0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V				0.4	
		I _{OL} = 7.8 mA, V _{CC} = 6 V				0.4	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V					±1000	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V					±10	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					160	μA
C _i	V _{CC} = 2 V to 6 V					10	pF

5.7 Electrical Characteristics – SN74HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = −20 μA	V _{CC} = 2 V	1.9			V
			V _{CC} = 4.5 V	4.4			
			V _{CC} = 6 V	5.9			
		I _{OH} = −6 mA, V _{CC} = 4.5 V		3.7			
		I _{OH} = −7.8 mA, V _{CC} = 6 V		5.2			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	V _{CC} = 2 V			0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 6 V			0.1	
		I _{OL} = 6 mA, V _{CC} = 4.5 V				0.4	
		I _{OL} = 7.8 mA, V _{CC} = 6 V				0.4	
I _I	V _I = V _{CC} or 0, V _{CC} = 6 V					±1000	nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL} , V _{CC} = 6 V					±10	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V					160	μA
C _i	V _{CC} = 2 V to 6 V					10	pF

5.8 Switching Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted; see [Figure 6-1](#))

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	$C_L = 50 \text{ pF}$		40	115	ns
			$C_L = 150 \text{ pF}$		56	165	
		$V_{CC} = 4.5 \text{ V}$	$C_L = 50 \text{ pF}$		13	23	
			$C_L = 150 \text{ pF}$		18	33	
		$V_{CC} = 6 \text{ V}$	$C_L = 50 \text{ pF}$		11	20	
			$C_L = 150 \text{ pF}$		15	28	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	$C_L = 50 \text{ pF}$		75	150	ns
			$C_L = 150 \text{ pF}$		100	200	
		$V_{CC} = 4.5 \text{ V}$	$C_L = 50 \text{ pF}$		15	30	
			$C_L = 150 \text{ pF}$		20	40	
		$V_{CC} = 6 \text{ V}$	$C_L = 50 \text{ pF}$		13	26	
			$C_L = 150 \text{ pF}$		17	34	

$T_A = 25^\circ\text{C}$ (unless otherwise noted; see [Figure 6-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dis}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2\text{ V}$ $C_L = 50\text{ pF}$		75	150	ns
		$V_{CC} = 4.5\text{ V}$ $C_L = 50\text{ pF}$		15	30	
		$V_{CC} = 6\text{ V}$ $C_L = 50\text{ pF}$		13	26	
t_t	To Y (output)	$V_{CC} = 2\text{ V}$	$C_L = 50\text{ pF}$	28	60	ns
			$C_L = 150\text{ pF}$	45	210	
		$V_{CC} = 4.5\text{ V}$	$C_L = 50\text{ pF}$	8	12	
			$C_L = 150\text{ pF}$	17	42	
		$V_{CC} = 6\text{ V}$	$C_L = 50\text{ pF}$	6	10	
			$C_L = 150\text{ pF}$	13	36	

5.9 Switching Characteristics – $C_L = 50\text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see [Figure 6-1](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2\text{ V}$	SN54HC244		170	ns
			SN74HC244		170	
		$V_{CC} = 4.5\text{ V}$	SN54HC244		34	
			SN74HC244		34	
		$V_{CC} = 6\text{ V}$	SN54HC244		29	
			SN74HC244		29	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2\text{ V}$	SN54HC244		225	ns
			SN74HC244		225	
		$V_{CC} = 4.5\text{ V}$	SN54HC244		45	
			SN74HC244		45	
		$V_{CC} = 6\text{ V}$	SN54HC244		38	
			SN74HC244		38	
t_{dis}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2\text{ V}$	SN54HC244		225	ns
			SN74HC244		225	
		$V_{CC} = 4.5\text{ V}$	SN54HC244		45	
			SN74HC244		45	
		$V_{CC} = 6\text{ V}$	SN54HC244		38	
			SN74HC244		38	
t_t	To Y (output)	$V_{CC} = 2\text{ V}$	SN54HC244		90	ns
			SN74HC244		90	
		$V_{CC} = 4.5\text{ V}$	SN54HC244		18	
			SN74HC244		18	
		$V_{CC} = 6\text{ V}$	SN54HC244		15	
			SN74HC244		15	

5.10 Switching Characteristics – $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		245	ns
			SN74HC244		245	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		49	
			SN74HC244		49	
		$V_{CC} = 6 \text{ V}$	SN54HC244		42	
			SN74HC244		42	
t_{en}	From $\overline{OE}$ (input) to Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		300	ns
			SN74HC244		300	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		60	
			SN74HC244		60	
		$V_{CC} = 6 \text{ V}$	SN54HC244		51	
			SN74HC244		51	
t_t	To Y (output)	$V_{CC} = 2 \text{ V}$	SN54HC244		315	ns
			SN74HC244		315	
		$V_{CC} = 4.5 \text{ V}$	SN54HC244		63	
			SN74HC244		63	
		$V_{CC} = 6 \text{ V}$	SN54HC244		53	
			SN74HC244		53	

5.11 Typical Characteristic

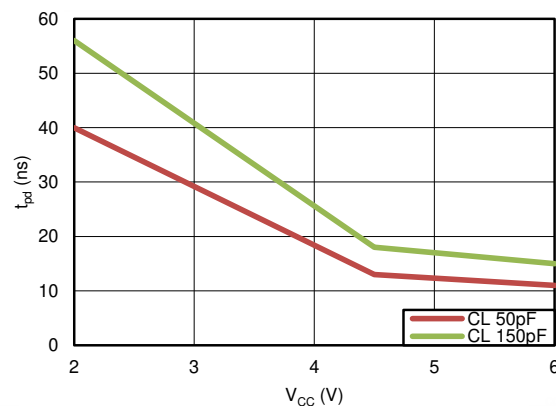


Figure 5-1. Propagation Delay

6 Parameter Measurement Information

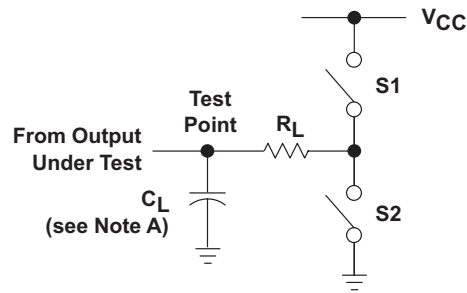


Figure 6-1. Load Circuit

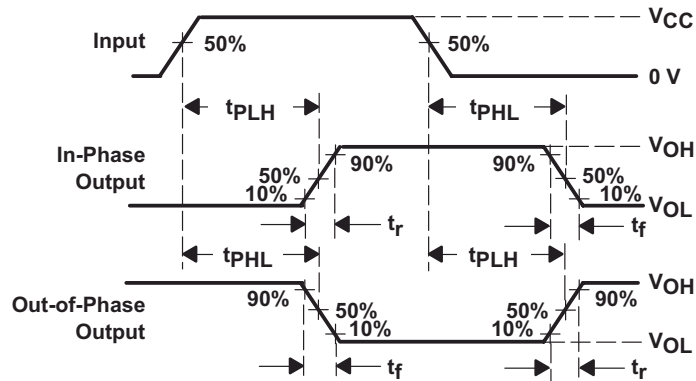


Figure 6-2. Propagation Delay and Output Transition Times

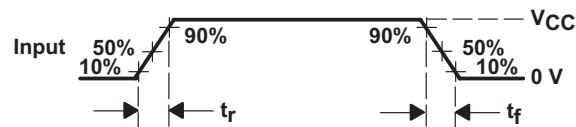


Figure 6-3. Input Rise and Fall Times

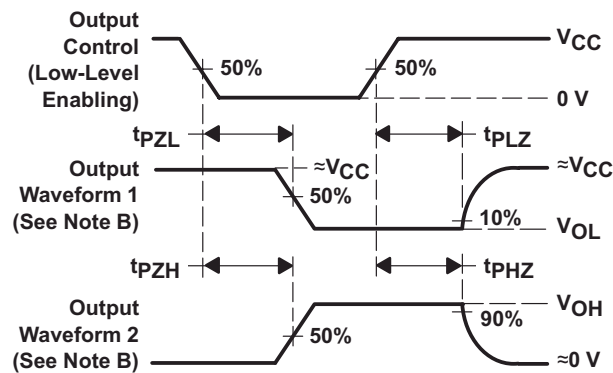


Figure 6-4. Enable and Disable Times for 3-State Outputs

Note**NOTE:**

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Table 6-1. Switching Information Table

PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}	1 k Ω	50 pF or 150 pF	Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}	1 k Ω	50 pF	Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open

7 Detailed Description

7.1 Overview

The SNx4HC244 contains 8 individual high speed CMOS buffers with Schmitt-trigger inputs and 3-state outputs.

Each buffer performs the boolean logic function $xY_n = xA_n$, with x being the bank number and n being the channel number.

Each output enable ($x\overline{OE}$) controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

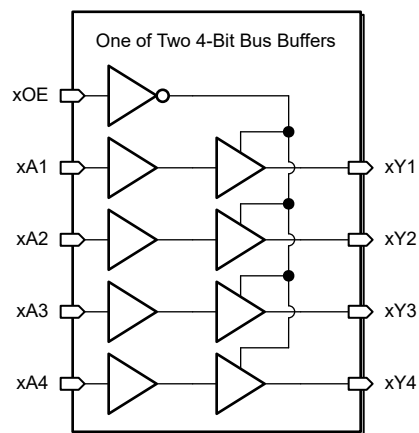


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4HC244.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application and Implementation

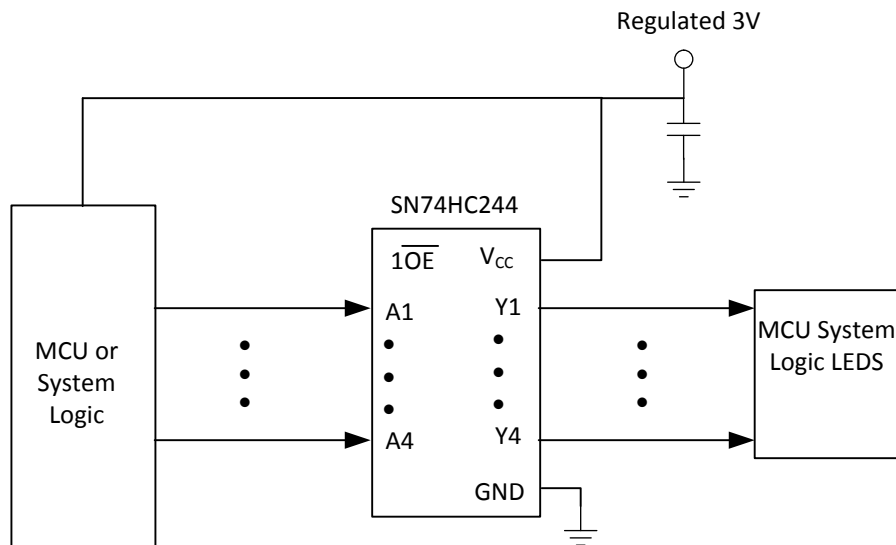
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application



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Figure 8-1. SN74HC244 Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in [Section 5.3](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Section 5.3](#).
2. Recommend output conditions:
 - Load currents should not exceed I_O max per output and should not exceed the continuous current through V_{CC} or GND total current for the part. These limits are located in [Section 5.1](#).
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curve

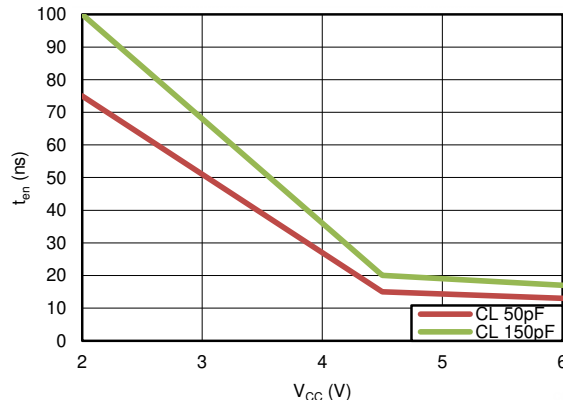


Figure 8-2. Enable Time

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer signals that must branch separately

8.4.1 Layout Example

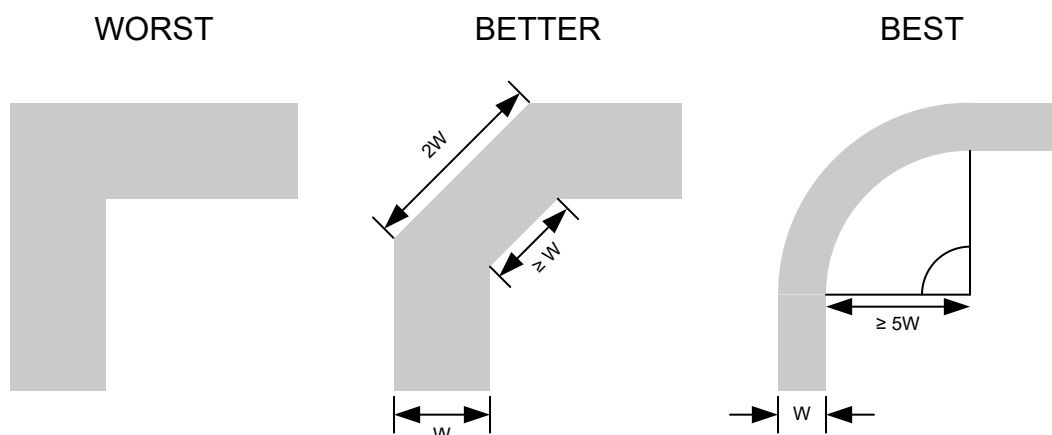


Figure 8-3. Example Trace Corners for Improved Signal Integrity

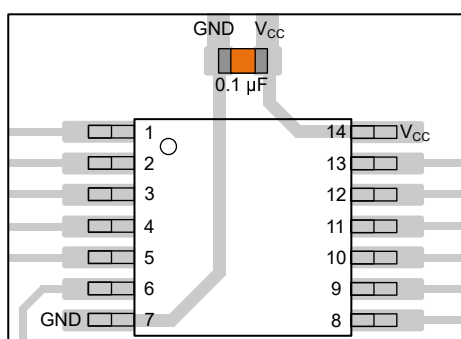


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

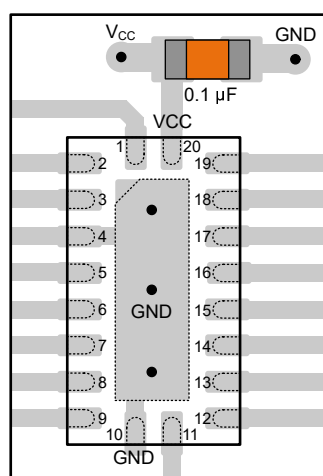


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

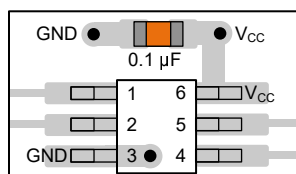


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

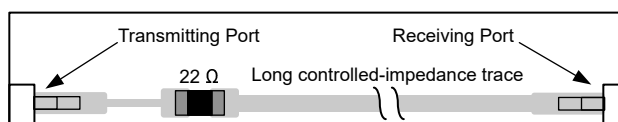


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

Table 9-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC244	Click here	Click here	Click here	Click here	Click here
SN74HC244	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2025) to Revision H (February 2025) Page

- Updated SN74HC244 operating temperature to 125°C and respective values in *Electrical Characteristics* table, *Recommended Operating Conditions* table, and *Switching Characteristics* tables..... **1**

Changes from Revision F (May 2022) to Revision G (January 2025) Page

- Added package size to *Device Information* table and updated structural layout of data sheet to current standards..... **1**
- Updated *Features Description* and corrected *Functional Block Diagram* image and *Device Functional Modes* table **11**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8409601VRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8409601VR A SNV54HC244J
5962-8409601VRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8409601VR A SNV54HC244J
5962-8409601VSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8409601VS A SNV54HC244W
5962-8409601VSA.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8409601VS A SNV54HC244W
84096012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK
8409601RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J
8409601SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W
JM38510/65705B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705B2A
JM38510/65705B2A.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705B2A
JM38510/65705BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BRA
JM38510/65705BRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BRA
JM38510/65705BSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BSA
JM38510/65705BSA.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BSA
M38510/65705B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705B2A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M38510/65705BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BRA
M38510/65705BSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65705BSA
SN54HC244J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC244J
SN54HC244J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC244J
SN74HC244APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244A
SN74HC244APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244A
SN74HC244DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244DWRG4.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC244N
SN74HC244N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC244N
SN74HC244NE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC244N
SN74HC244NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244NSRG4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HC244
SN74HC244PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244
SN74HC244PWT	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HC244
SN74HC244QDWRG4Q1	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	HC244Q
SN74HC244QDWRG4Q1.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC244Q
SNJ54HC244FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54HC244FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84096012A SNJ54HC 244FK
SNJ54HC244J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J
SNJ54HC244J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601RA SNJ54HC244J
SNJ54HC244W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W
SNJ54HC244W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409601SA SNJ54HC244W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC244, SN54HC244-SP, SN74HC244 :

- Catalog : [SN74HC244](#), [SN54HC244](#)
- Automotive : [SN74HC244-Q1](#), [SN74HC244-Q1](#)
- Enhanced Product : [SN74HC244-EP](#), [SN74HC244-EP](#)
- Military : [SN54HC244](#)
- Space : [SN54HC244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC244NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC244APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244DWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244DWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC244NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74HC244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC244QDWRG4Q1	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8409601VSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8409601VSA.A	W	CFP	20	25	506.98	26.16	6220	NA
84096012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8409601SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65705B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65705B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65705BSA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65705BSA.A	W	CFP	20	25	506.98	26.16	6220	NA
M38510/65705B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65705BSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74HC244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC244N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC244FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC244FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC244W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54HC244W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

NOTES:

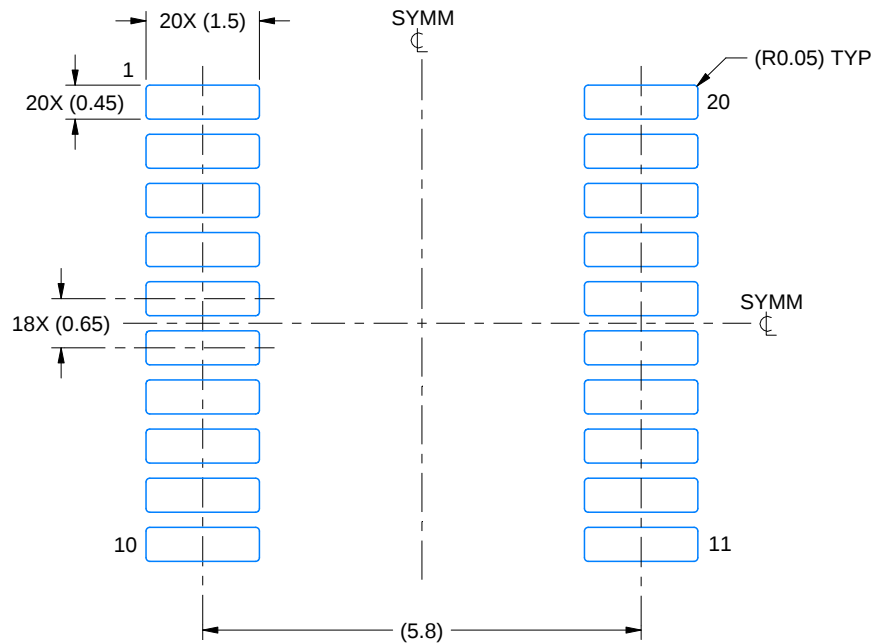
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

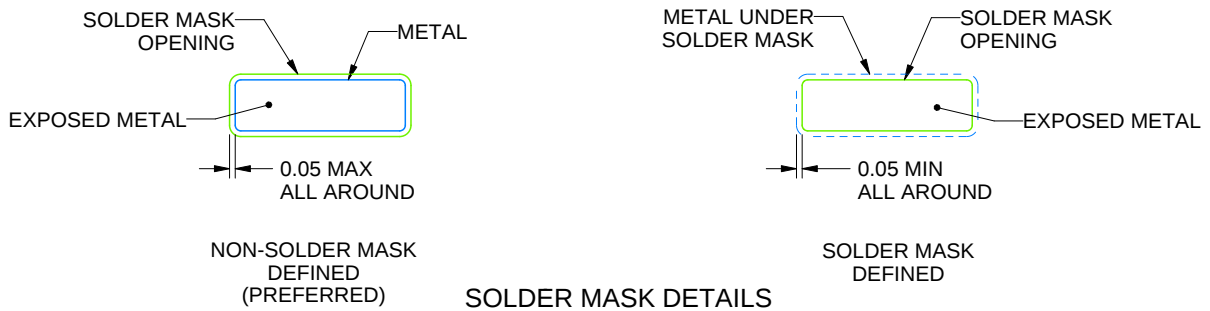
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

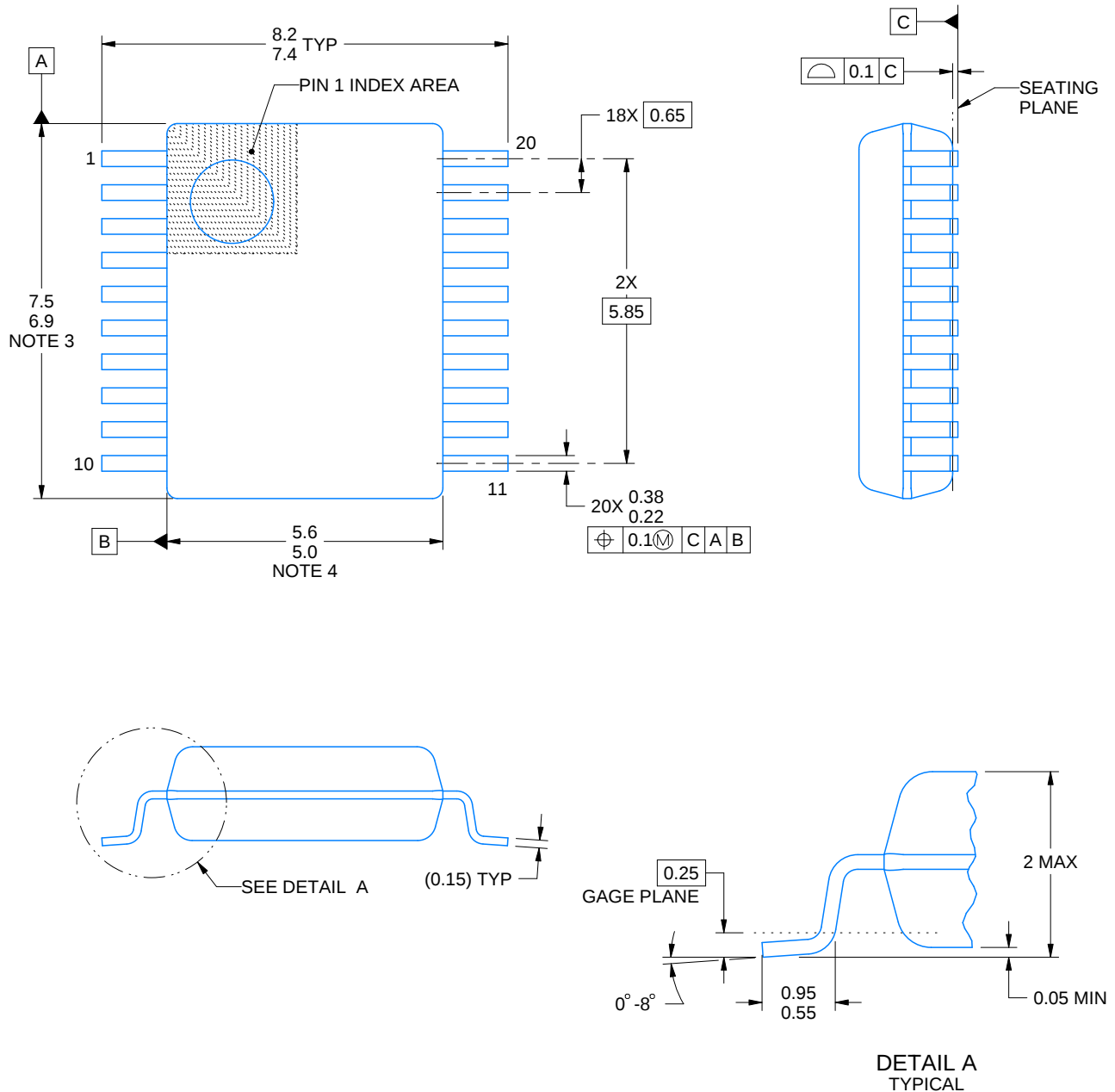
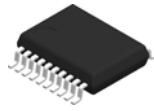


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

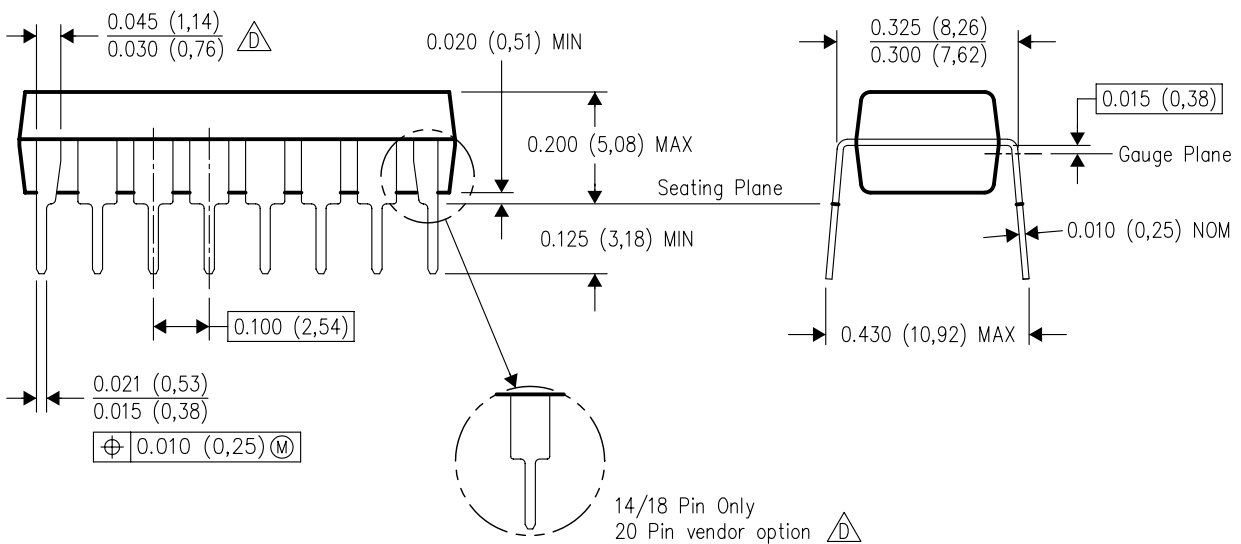
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



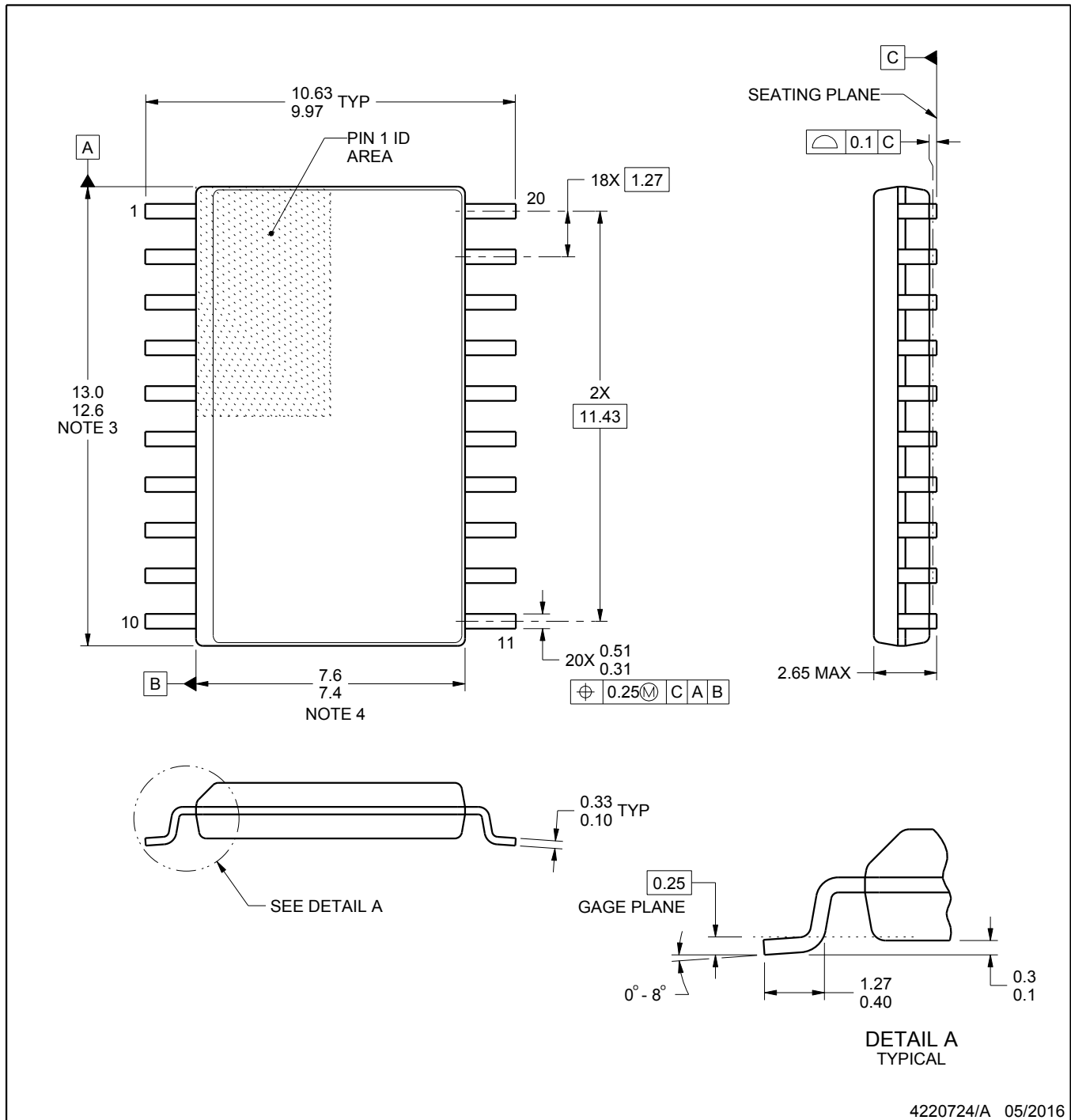
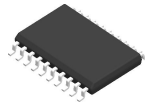
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



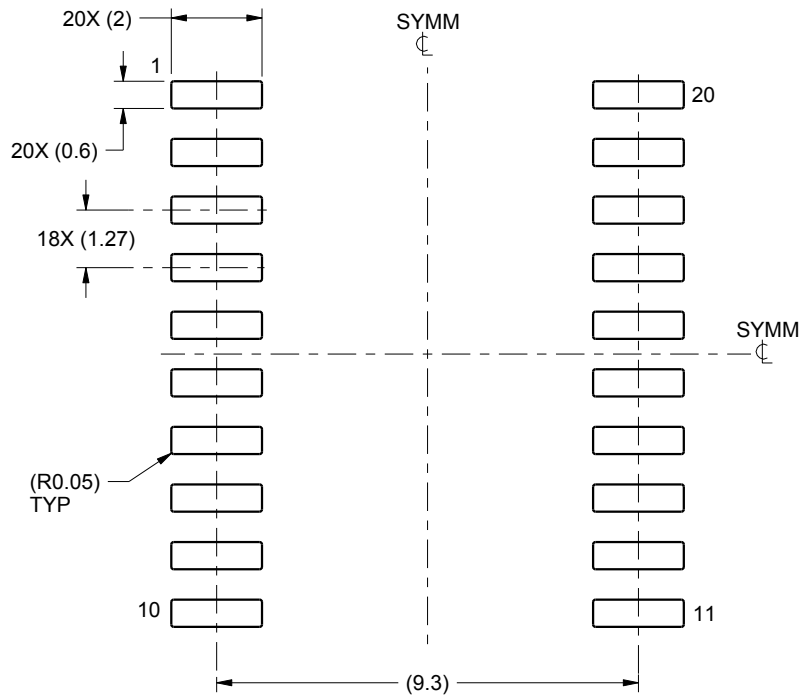
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

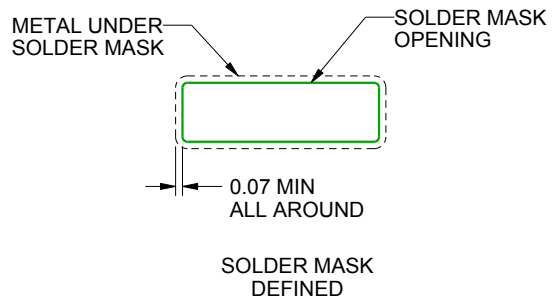
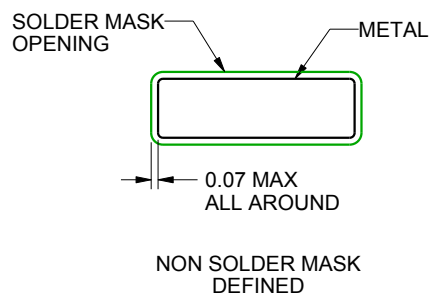
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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