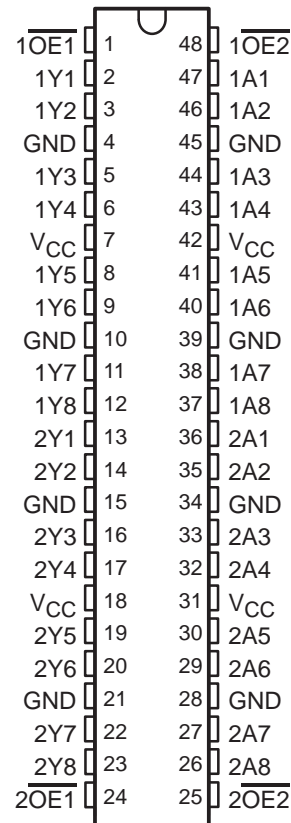


SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS331F – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16540 . . . WD PACKAGE
SN74AHC16540 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16540 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z



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 **TEXAS
INSTRUMENTS**

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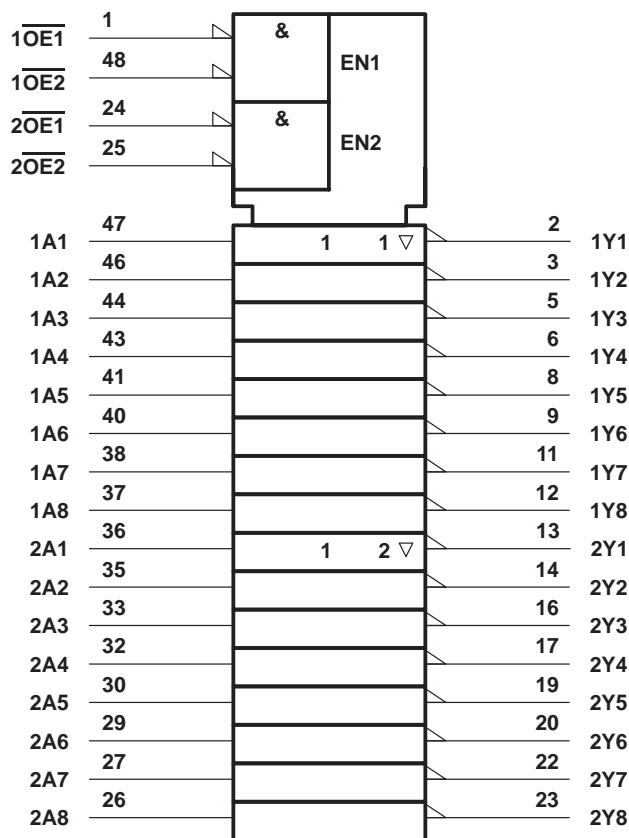
SN54AHC16540, SN74AHC16540

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

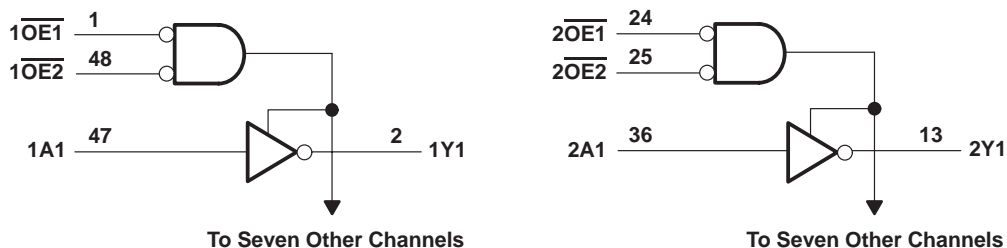
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54AHC16540, SN74AHC16540
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCLS331F – MARCH 1996 – REVISED JANUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through each V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHC16540		SN74AHC16540		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5		V
		$V_{CC} = 3$ V		2.1		
		$V_{CC} = 5.5$ V		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		V
		$V_{CC} = 3$ V		0.9		
		$V_{CC} = 5.5$ V		1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		–4		mA
		$V_{CC} = 5$ V ± 0.5 V		–8		
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		4		mA
		$V_{CC} = 5$ V ± 0.5 V		8		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHC16540, SN74AHC16540

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCLS331F – MARCH 1996 – REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		V	
		3 V			0.1		0.1			
		4.5 V			0.1		0.1			
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		μA	
I _{OZ}	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		4.8**	8.4**	1**	10**	1	10	ns
t _{PHL}											
t _{PZH}	\overline{OE}	Y	C _L = 15 pF		6.8**	10.6**	1**	12.5**	1	12.5	ns
t _{PZL}											
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF		6.8**	11.5**	1**	12.5**	1	12.5	ns
t _{PLZ}											
t _{PLH}	A	Y	C _L = 50 pF		7.7	11	1	12.5	1	12.5	ns
t _{PHL}											
t _{PZH}	\overline{OE}	Y	C _L = 50 pF		9.7	14.1	1	16	1	16	ns
t _{PZL}											
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF		9.4	14	1	16	1	16	ns
t _{PLZ}											
t _{sk(o)}			C _L = 50 pF			1.5***				1.5	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

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SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	3.7*	6*	1*	7*	1	7	ns	
t _{PHL}				3.7*	6*	1*	7*	1	7		
t _{PZH}	\overline{OE}	Y	C _L = 15 pF	4.7*	7.3*	1*	8.5*	1	8.5	ns	
t _{PZL}				4.7*	7.3*	1*	8.5*	1	8.5		
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF	4.5*	7.2*	1*	8.5*	1	8.5	ns	
t _{PLZ}				4.5*	7.2*	1*	8.5*	1	8.5		
t _{PLH}	A	Y	C _L = 50 pF	5.2	8	1	9	1	8.5	ns	
t _{PHL}				5.2	8	1	9	1	8.5		
t _{PZH}	\overline{OE}	Y	C _L = 50 pF	6.2	9.3	1	10.5	1	10.5	ns	
t _{PZL}				6.2	9.3	1	10.5	1	10.5		
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF	6	9.2	1	10.5	1	10.5	ns	
t _{PLZ}				6	9.2	1	10.5	1	10.5		
t _{sk(o)}			C _L = 50 pF		1**				1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC16540			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.6		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.3		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.7		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load, f = 1 MHz	13	pF

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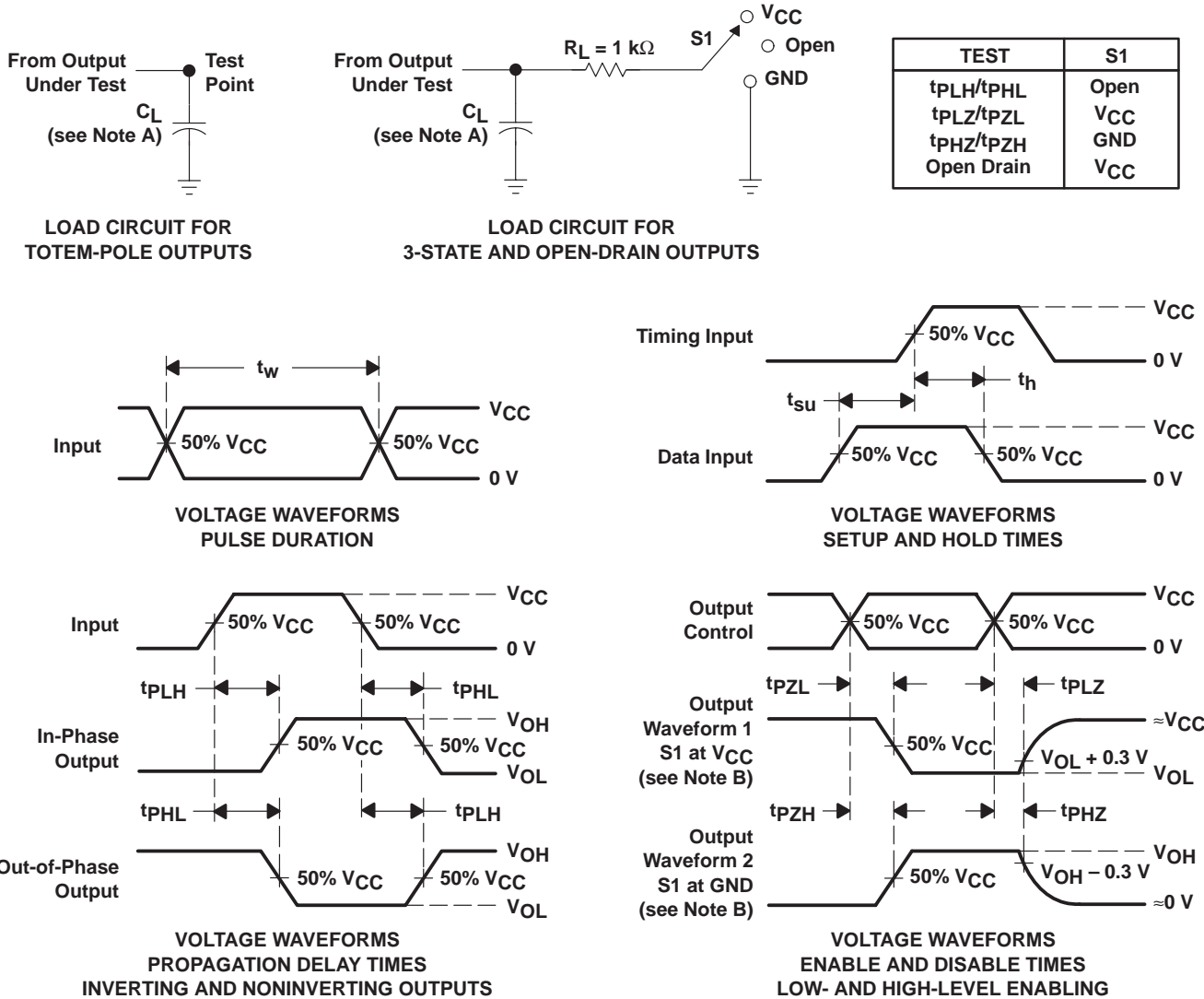


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SN54AHC16540, SN74AHC16540
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC16540DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16540
SN74AHC16540DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16540
SN74AHC16540DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16540
SN74AHC16540DL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16540

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

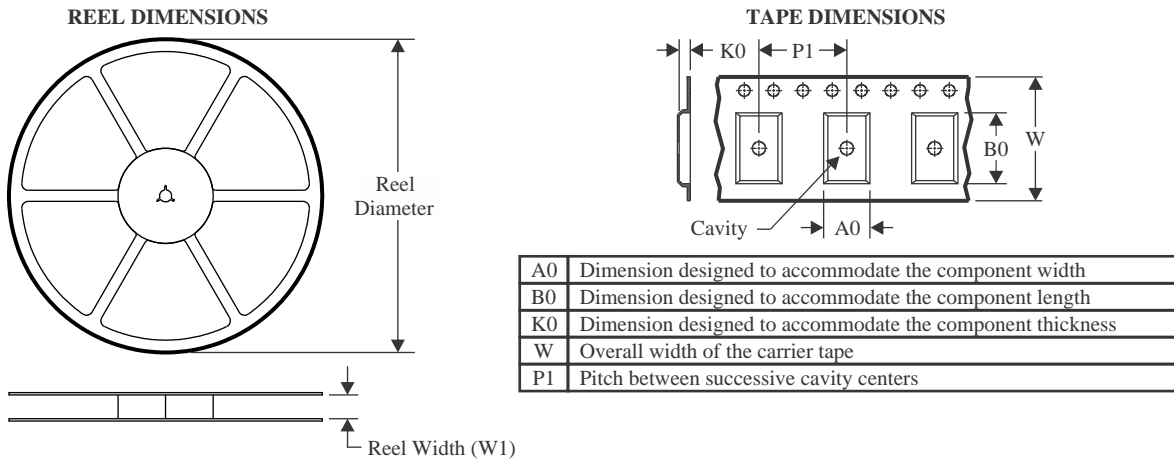
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

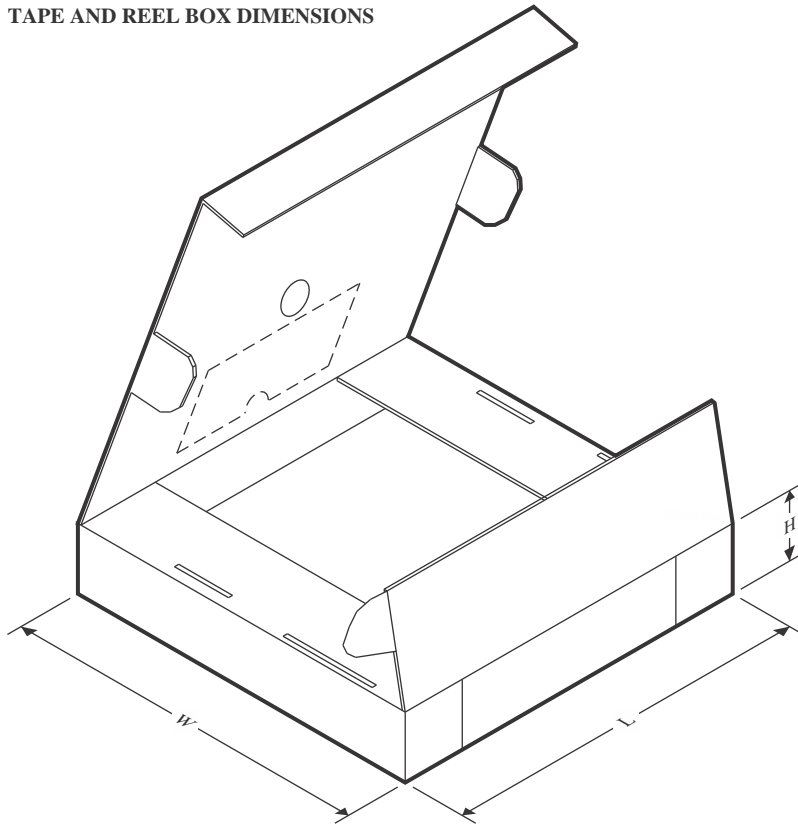
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16540DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16540DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

TUBE

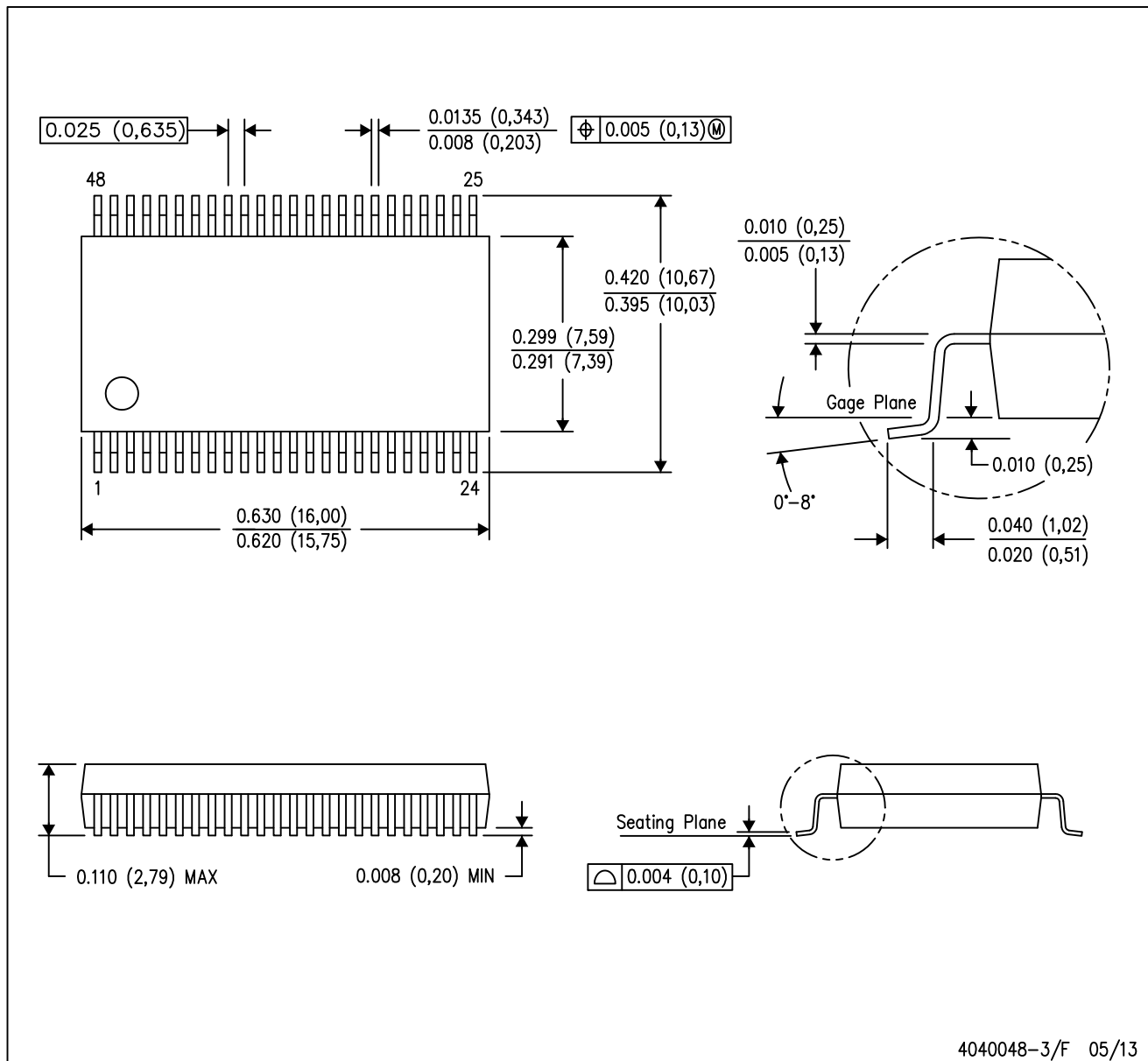

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC16540DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74AHC16540DL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

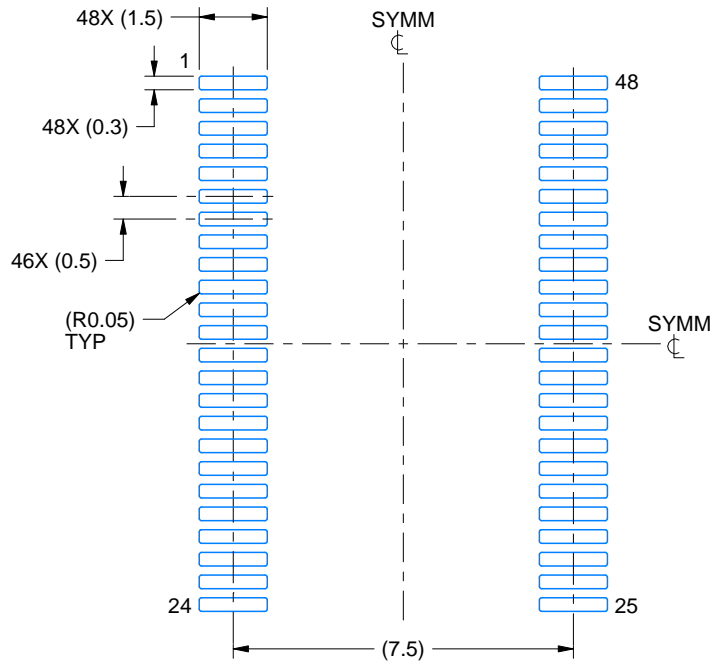
PowerPAD is a trademark of Texas Instruments.

EXAMPLE BOARD LAYOUT

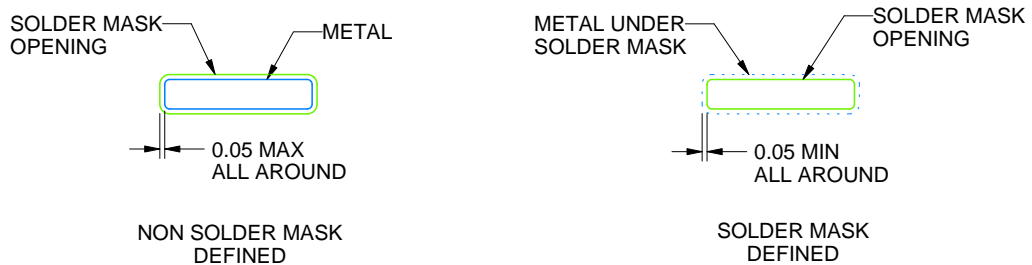
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

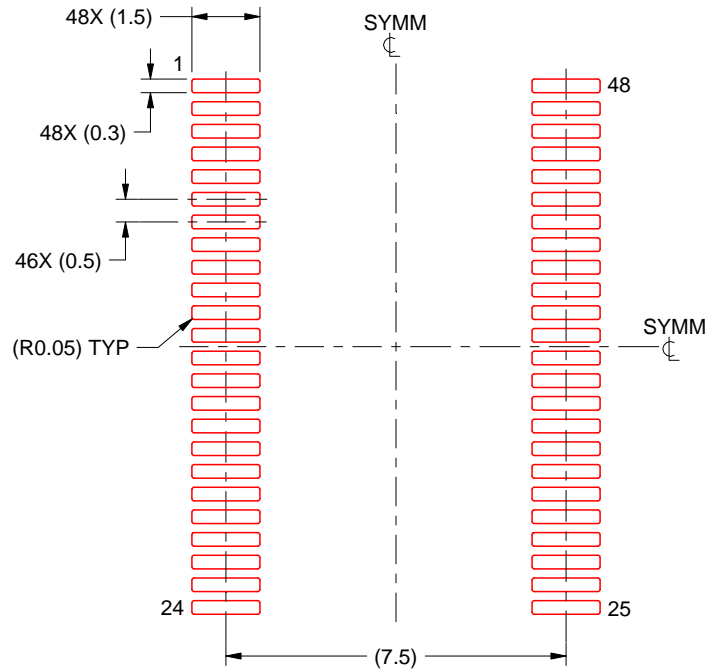
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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