

SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (-32 -mA I_{OH} , 64 -mA I_{OL})**
- **Parity-Error Flag With Parity Generator/Checker**
- **Register for Storage of Parity-Error Flag**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

description

The 'ABT16833 consist of two noninverting 8-bit to 9-bit parity bus transceivers and are designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error ($\overline{1ERR}$ or $\overline{2ERR}$) output is configured as an open-collector output. The B-to-A parity-error flag is clocked into $\overline{1ERR}$ (or $\overline{2ERR}$) on the low-to-high transition of the clock ($\overline{1CLK}$ or $\overline{2CLK}$) input. $\overline{1ERR}$ (or $\overline{2ERR}$) is cleared (set high) by taking the clear ($\overline{1CLR}$ or $\overline{2CLR}$) input low.

The output-enable ($\overline{OE_A}$ and $\overline{OE_B}$) inputs can be used to disable the device so that the buses are effectively isolated. When both $\overline{OE_A}$ and $\overline{OE_B}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16833 . . . WD PACKAGE
SN74ABT16833 . . . DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OE_B}$	1	56	$\overline{1OE_A}$
$\overline{1CLK}$	2	55	$\overline{1CLR}$
$\overline{1ERR}$	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2ERR}$	26	31	2PARITY
$\overline{2CLK}$	27	30	$\overline{2CLR}$
$\overline{2OE_B}$	28	29	$\overline{2OE_A}$



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**TEXAS
INSTRUMENTS**

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SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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description (continued)

The SN54ABT16833 is characterized for operation over the full military temperature range of –55°C to 125°C.
The SN74ABT16833 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	CLK	Ai $\Sigma \text{ OF H}$	$\text{Bi}^\dagger$ $\Sigma \text{ OF H}$	A	B	PARITY	$\overline{\text{ERR}}^\ddagger$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	$\uparrow$	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error-flag register
H	H	H	No $\uparrow$	X	X	Z	Z	Z	NC	Isolation §
		L	No $\uparrow$	X					H	
		H	$\uparrow$	Odd					H	
		H	$\uparrow$	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

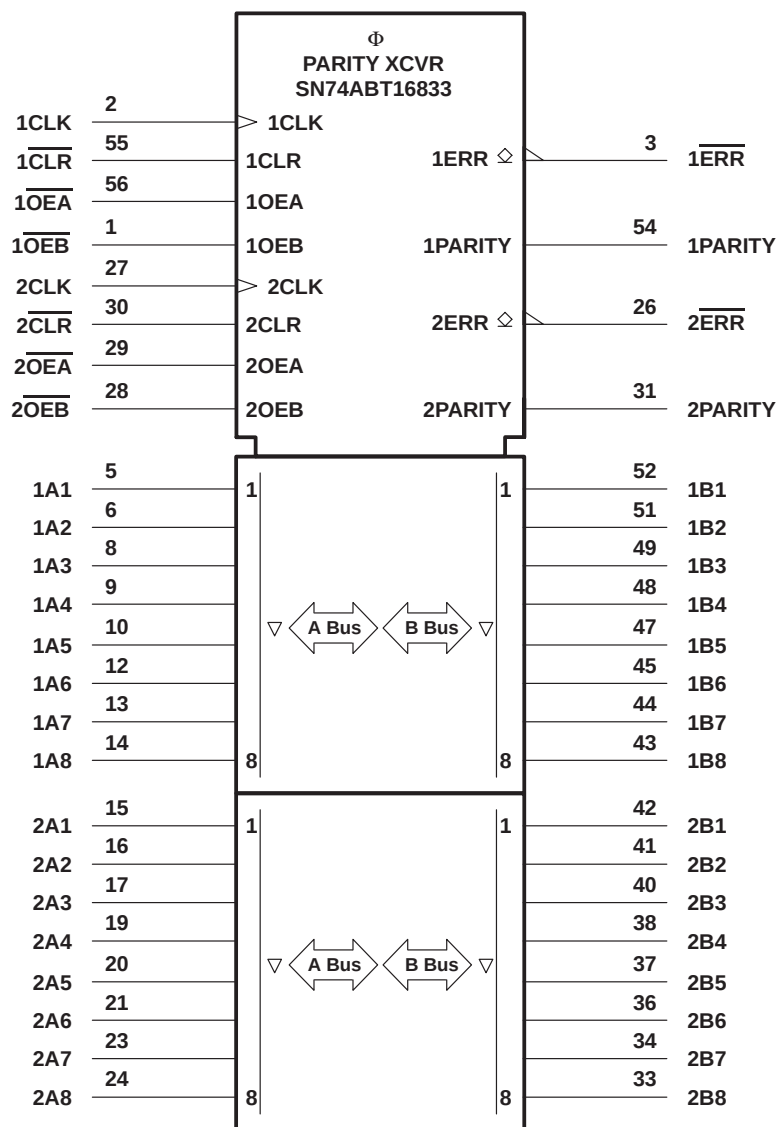
‡ Output states shown assume $\overline{\text{ERR}}$ was previously high.

§ In this mode, $\overline{\text{ERR}}$ (when clocked) shows inverted parity of the A bus.

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logic symbol[†]

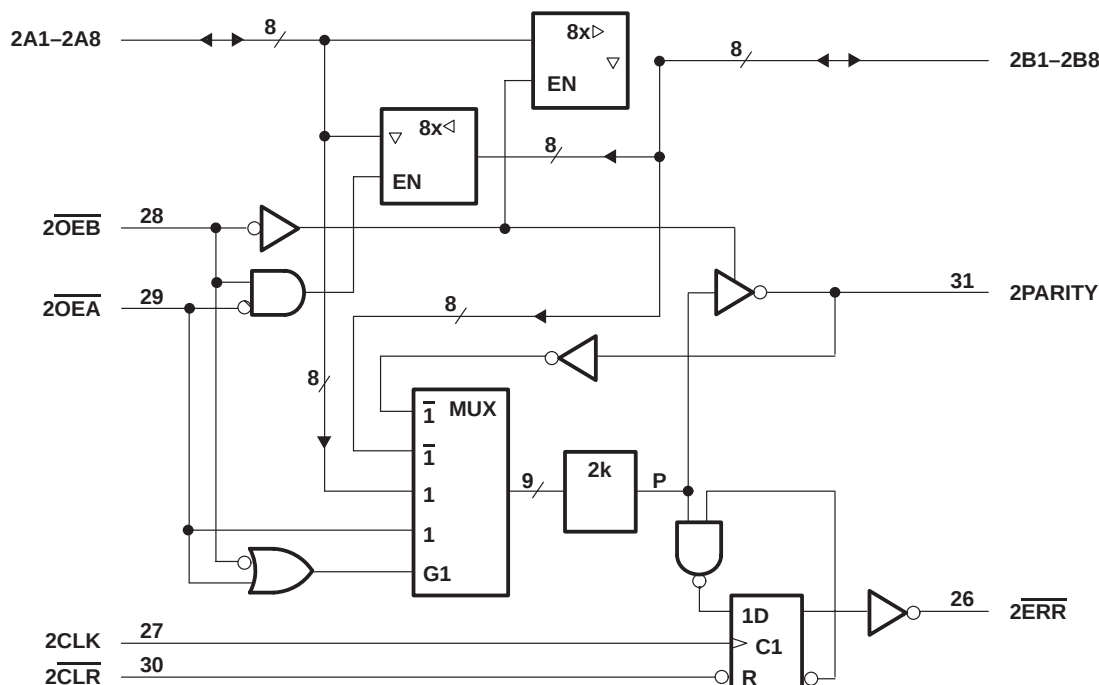
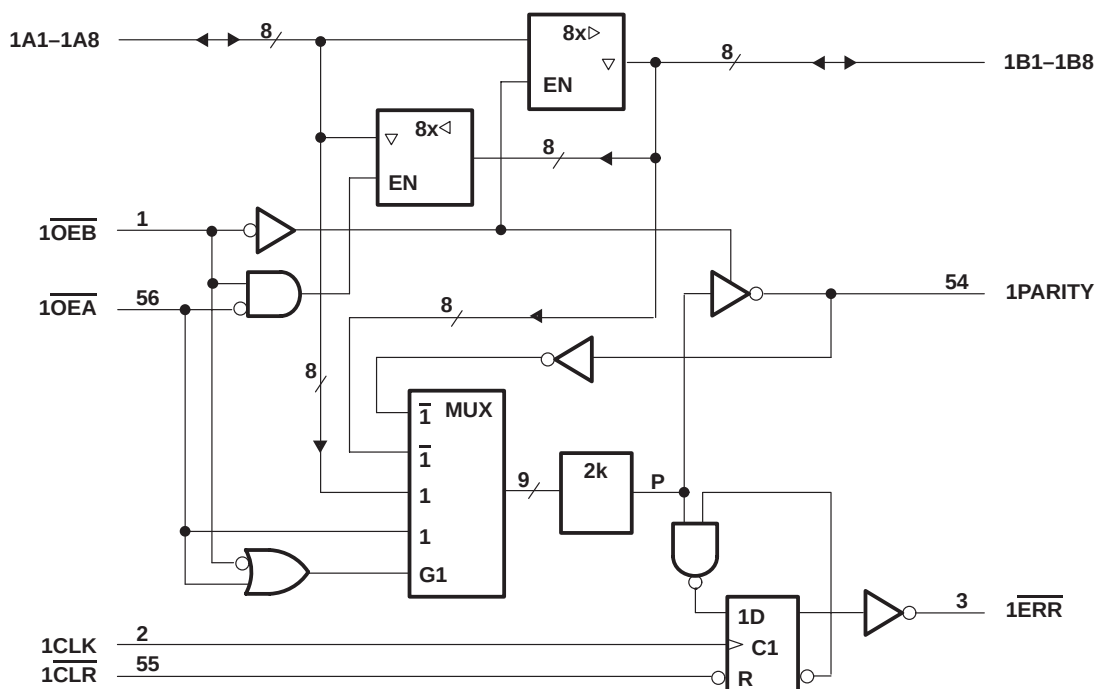


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

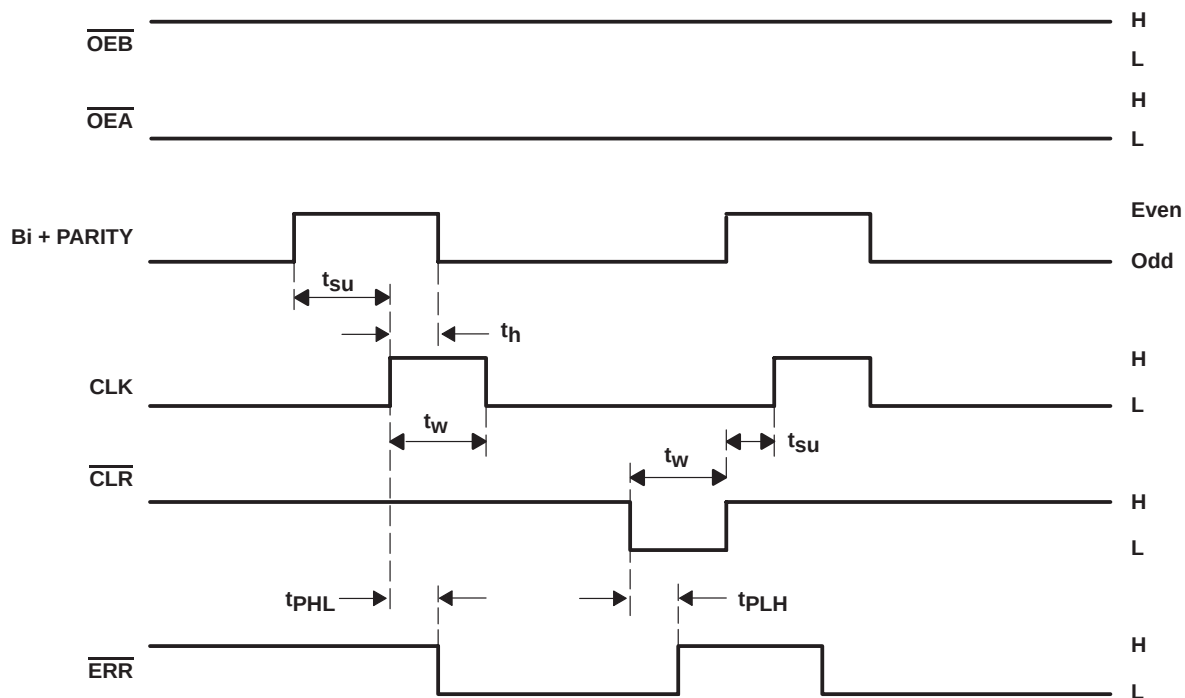
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ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	$\overline{\text{ERR}}_{n-1}^{\dagger}$		
H	$\uparrow$	H	H	H	Sample
H	$\uparrow$	X	L	L	
H	$\uparrow$	L	X	L	
L	X	X	X	H	Clear

$\dagger$ State of $\overline{\text{ERR}}$ before changes at CLR, CLK, or point P

error-flag waveforms



SN54ABT16833, SN74ABT16833

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16833	96 mA
SN74ABT16833	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16833		SN74ABT16833		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_{OH}	High-level output voltage	ERR		5.5		V
I_{OH}	High-level output current	Except ERR		–32		mA
I_{OL}	Low-level output current			64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16833		SN74ABT16833		UNIT
				MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V
V _{OH}	All outputs except $\overline{\text{ERR}}$	V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5	3		2.5				V
		V _{CC} = 5 V, I _{OH} = –3 mA		3	3.4		3		3		
		V _{CC} = 4.5 V	I _{OH} = –24 mA					2			
			I _{OH} = –32 mA		2*	2.7				2	
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 24 mA		0.25	0.55	0.55				V
			I _{OL} = 64 mA		0.3	0.55*			0.55		
V _{hys}				100							mV
I _{OH}	$\overline{\text{ERR}}$	V _{CC} = 4.5 V, V _{OH} = 5.5 V		20			20		20		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V		50			50		50		μA
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports			±100			±100		±100		
I _{IL}	A or B ports	V _{CC} = 0, V _I = GND		–50			–50		–50		μA
I _O [‡]		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I _{OZH} [§]		V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA
I _{OZL} [§]		V _{CC} = 5.5 V, V _O = 0.5 V		–50			–50		–50		μA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1.5	2	2		2		mA
			Outputs low		28	36	36		36		
			Outputs disabled		1	2	2		2		
ΔI _{CC} [¶]		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		50			50		50		μA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3							pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		9							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT16833		SN74ABT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, CLK high or low		3		3		3		ns
t _{SU}	Setup time before CLK↑	A port	4.5		4.5		4.5		ns
		$\overline{\text{CLR}}$	1		1		1		
		$\overline{\text{OEA}}$	5		5		5		
t _H	Hold time after CLK↑	A port or $\overline{\text{OEA}}$	0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

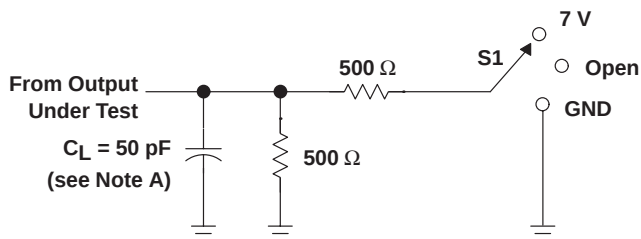
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT16833		SN74ABT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PZH}	$\overline{\text{OE}}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	$\overline{\text{OE}}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PLH}	A or $\overline{\text{OE}}$	PARITY	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PZH}	$\overline{\text{OE}}$	PARITY	2	3.6	5	2	5.8	2	5.7	ns
t_{PZL}			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
t_{PHZ}	$\overline{\text{OE}}$	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t_{PLZ}			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
t_{PLH}	CLK, $\overline{\text{CLR}}$	$\overline{\text{ERR}}$	2	3.4	4.2	2	4.8	2	4.6	ns
t_{PHL}	CLK		2	2.8	3.6	2	4.1	2	3.9	

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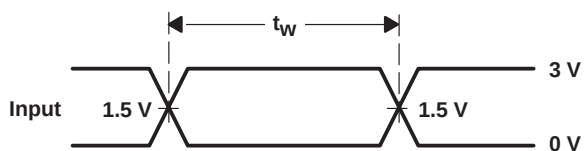
PARAMETER MEASUREMENT INFORMATION



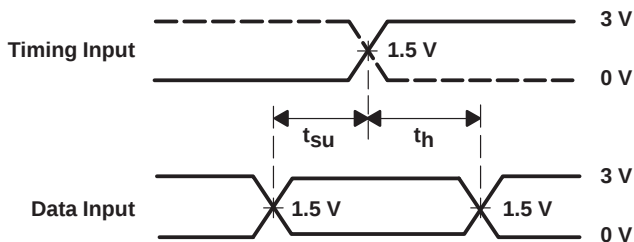
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

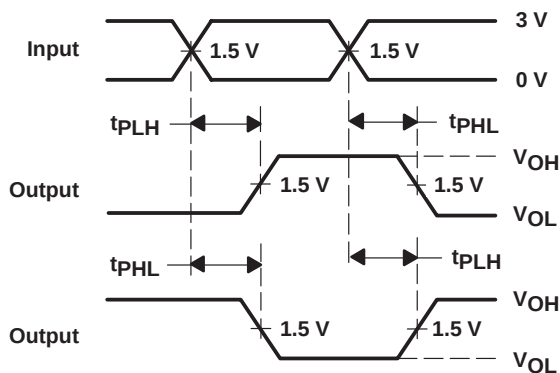
$\overline{\text{ERR}}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V



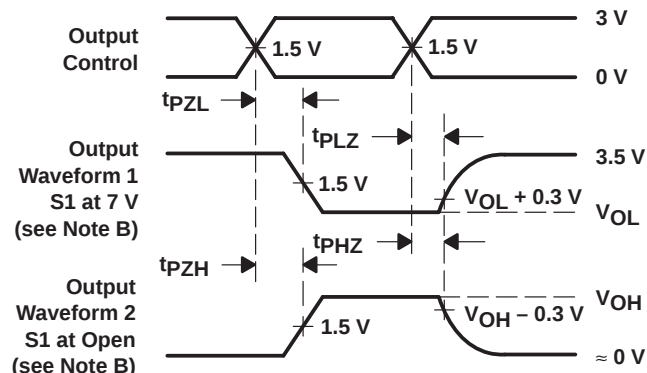
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PHL} is measured at 1.5 V.
- F. t_{PLH} is measured at $V_{OL} + 0.3 \text{ V}$.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT16833DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16833
SN74ABT16833DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16833
SN74ABT16833DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16833
SN74ABT16833DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16833

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16833DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16833DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16833DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16833DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

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