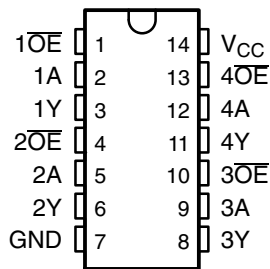


SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

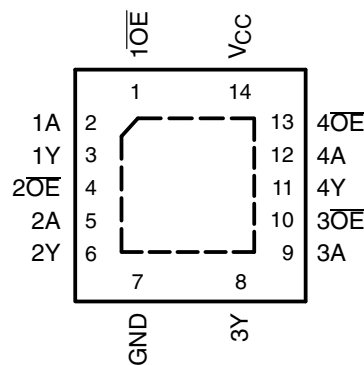
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- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

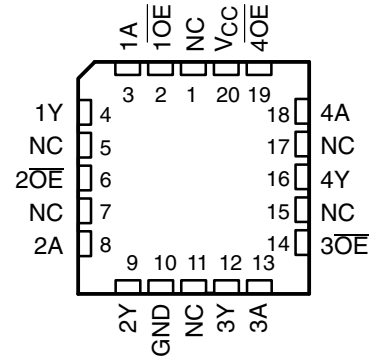
SN54ABT125 . . . J OR W PACKAGE
SN74ABT125 . . . D, DB, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74ABT125 . . . RGY PACKAGE
(TOP VIEW)



SN54ABT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'ABT125 quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ABT125N	SN74ABT125N
	QFN – RGY	Tape and reel	SN74ABT125RGYR	AB125
	SOIC – D	Tube	SN74ABT125D	ABT125
		Tape and reel	SN74ABT125DR	
	SOP – NS	Tape and reel	SN74ABT125NSR	ABT125
	SSOP – DB	Tape and reel	SN74ABT125DBR	AB125
TSSOP – PW	Tape and reel	SN74ABT125PWR	AB125	
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT125J	SNJ54ABT125J
	CFP – W	Tube	SNJ54ABT125W	SNJ54ABT125W
	LCCC – FK	Tube	SNJ54ABT125FK	SNJ54ABT125FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

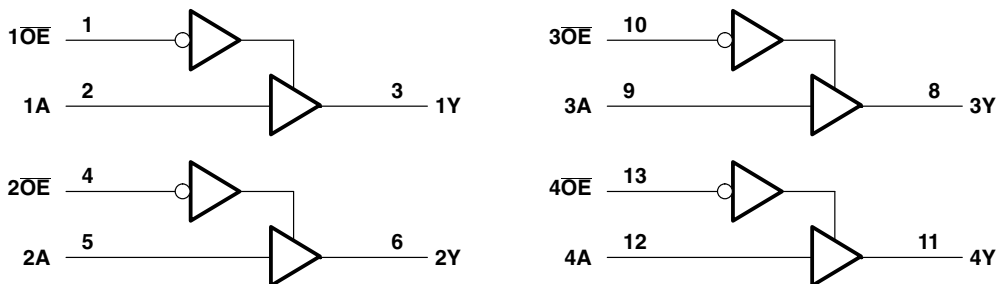
SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS182I – FEBRUARY 1997 – REVISED NOVEMBER 2002

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT125	96 mA
SN74ABT125	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS182I – FEBRUARY 1997 – REVISED NOVEMBER 2002

recommended operating conditions (see Note 4)

		SN54ABT125		SN74ABT125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS1821 – FEBRUARY 1997 – REVISED NOVEMBER 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT125		SN74ABT125		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$				2			2	
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55			V
		$I_{OL} = 64\text{ mA}$		0.55*			0.55		
V_{hys}			100						mV
I_I	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1		± 1		± 1	μA
I_{OZPU}	$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA
I_{OZPD}	$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50		± 50		± 50	μA
I_{OZH}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 2.7\text{ V}$, $\overline{OE} \geq 2\text{ V}$			10		10		10	μA
I_{OZL}	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V}$, $\overline{OE} \geq 2\text{ V}$			-10		-10		-10	μA
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$			± 100				± 100	μA
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$			50		50		50	μA
I_O^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-200§	-50	-200§	-50	-200§	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		1	250	250		250	μA
		Outputs low		24	30	30		30	mA
		Outputs disabled		0.5	250	250		250	μA
ΔI_{CC}^\parallel	Data inputs $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		0.05		0.05		0.05	
	Control inputs $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1.5		1.5		1.5	
C_i	$V_I = 2.5\text{ V or }0.5\text{ V}$			3					pF
C_o	$V_O = 2.5\text{ V or }0.5\text{ V}$			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This limit may vary among suppliers.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS182I – FEBRUARY 1997 – REVISED NOVEMBER 2002

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

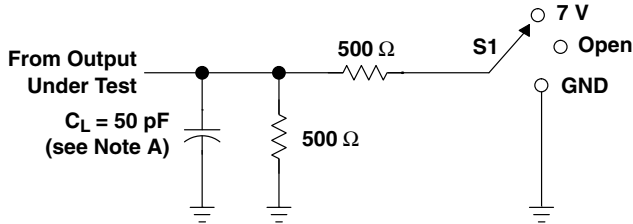
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			SN54ABT125		SN74ABT125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}^\dagger	A	Y	1	3.2	4.6	1	6	1	4.9	ns
t_{PHL}^\dagger			1	2.5	4.6	1	6.2	1	4.9	
t_{PZH}^\dagger	\overline{OE}	Y	1	3.6	5	1	6	1	5.9	ns
t_{PZL}^\dagger			1	2.5	6.2	1	7.5	1	6.8	
t_{PHZ}	\overline{OE}	Y	1	3.8	5.4	1	6.3	1	6.2	ns
t_{PLZ}^\dagger			1	3.3	5.3	1	6.5	1	6.2	

[†] This limit may vary among suppliers.

SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

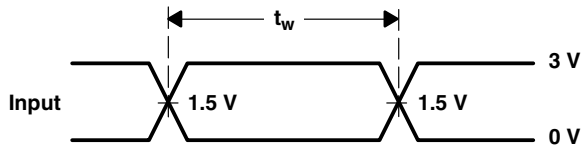
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PARAMETER MEASUREMENT INFORMATION

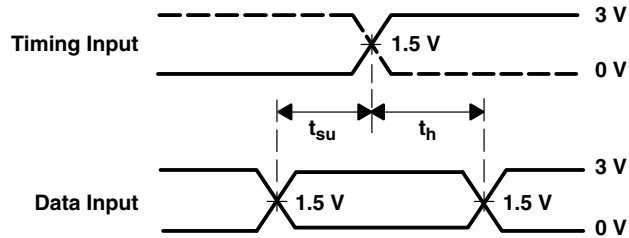


LOAD CIRCUIT

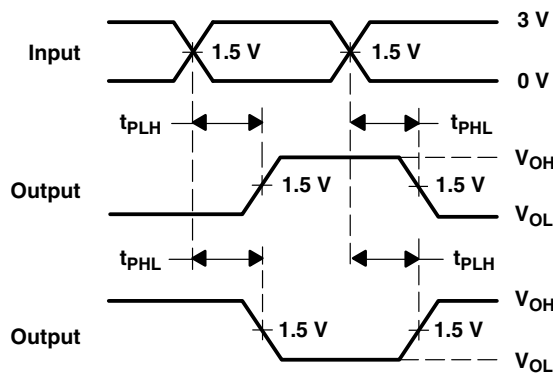
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



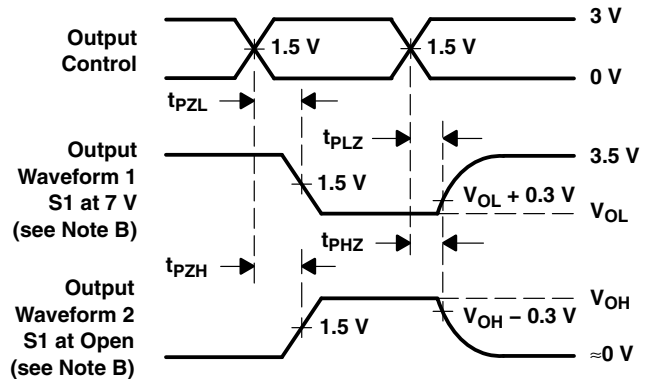
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9676801Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9676801Q2A SNJ54ABT 125FK
5962-9676801QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676801QC A SNJ54ABT125J
5962-9676801QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676801QD A SNJ54ABT125W
SN74ABT125D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125D.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125DBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125DBRG4.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125DE4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DRE4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT125N
SN74ABT125N.B	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT125N
SN74ABT125NS.B	Active	Production	SOP (NS) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125NSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT125
SN74ABT125PW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125PW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125PWG4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT125PWRE4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB125
SN74ABT125RGRY	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB125
SN74ABT125RGRY.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB125
SN74ABT125RGRYR4.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB125
SNJ54ABT125FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676801Q2A SNJ54ABT125FK
SNJ54ABT125J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676801QC A SNJ54ABT125J
SNJ54ABT125W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9676801QD A SNJ54ABT125W

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABT125, SN74ABT125 :

- Catalog : [SN74ABT125](#)
- Military : [SN54ABT125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

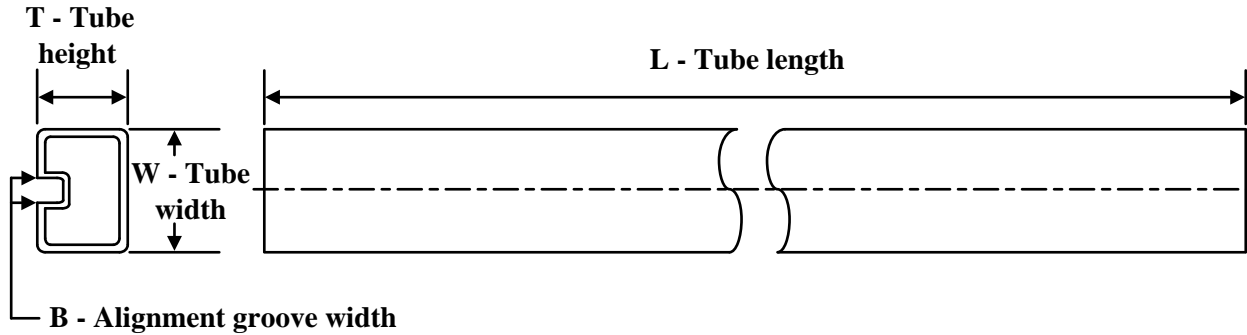

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ABT125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ABT125NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ABT125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ABT125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT125DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ABT125DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74ABT125NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74ABT125PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ABT125RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9676801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9676801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ABT125D	D	SOIC	14	50	506.6	8	3940	4.32
SN74ABT125D	D	SOIC	14	50	507	8	3940	4.32
SN74ABT125D.B	D	SOIC	14	50	507	8	3940	4.32
SN74ABT125D.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74ABT125DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74ABT125DE4	D	SOIC	14	50	507	8	3940	4.32
SN74ABT125DG4	D	SOIC	14	50	507	8	3940	4.32
SN74ABT125DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74ABT125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT125N.B	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT125N.B	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT125NS.B	NS	SOP	14	50	530	10.5	4000	4.1
SN74ABT125PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74ABT125PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74ABT125PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54ABT125FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT125W	W	CFP	14	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

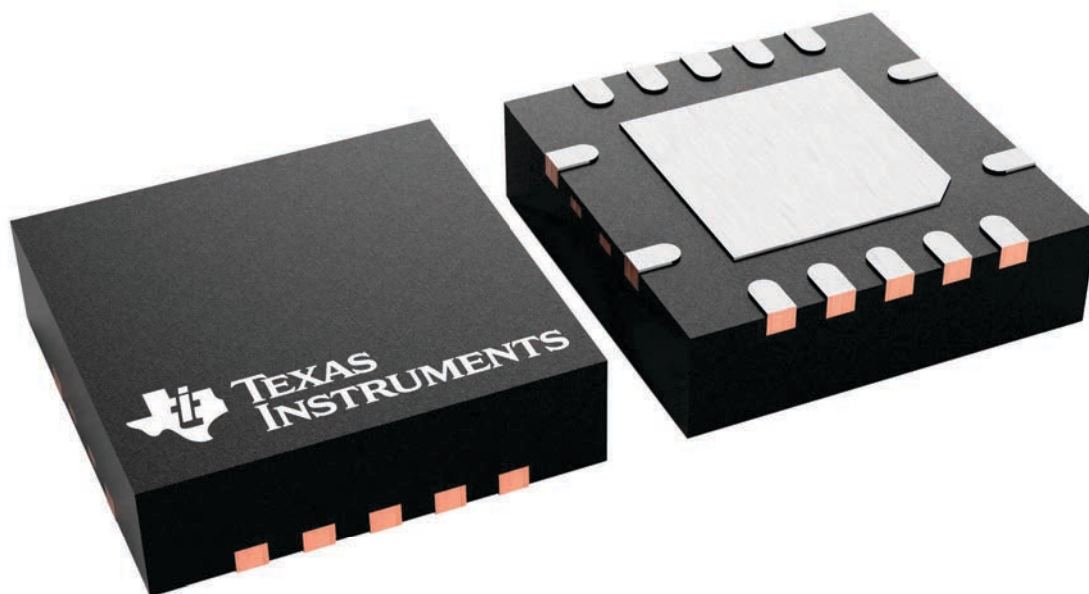
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

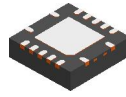
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

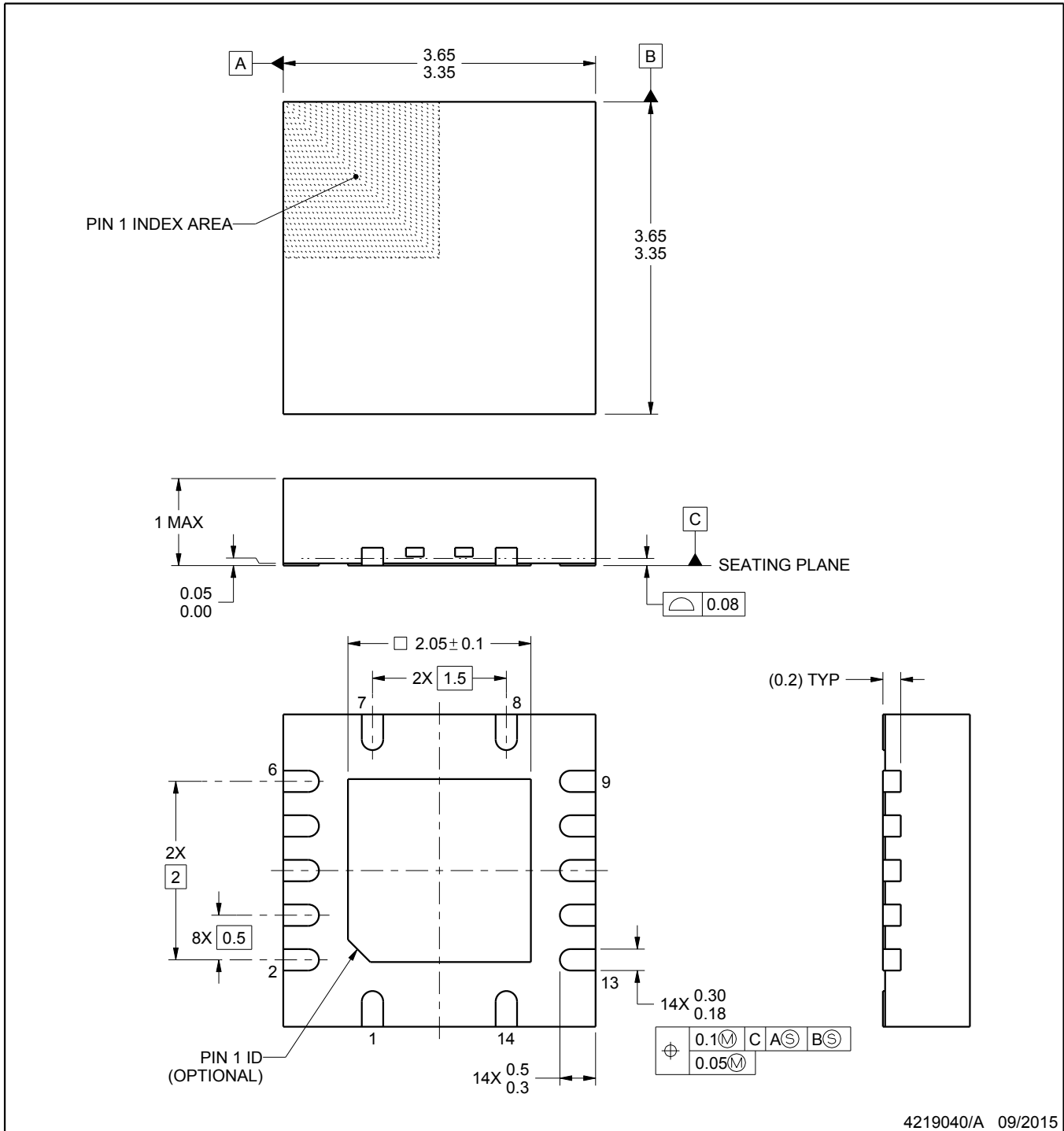
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

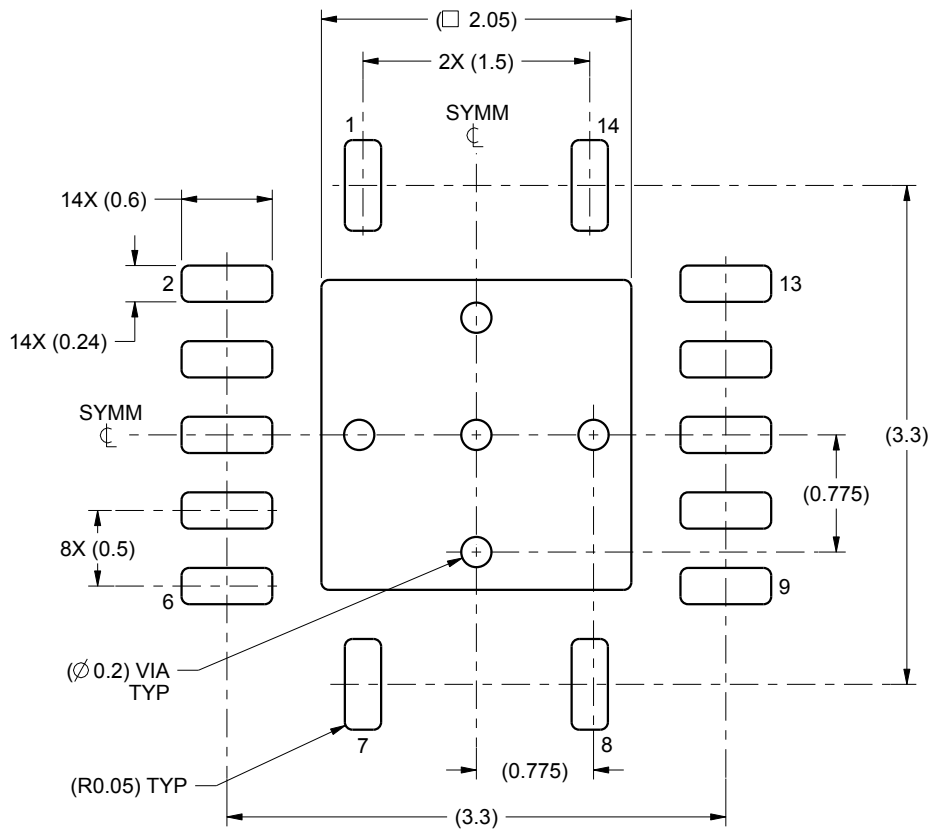
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

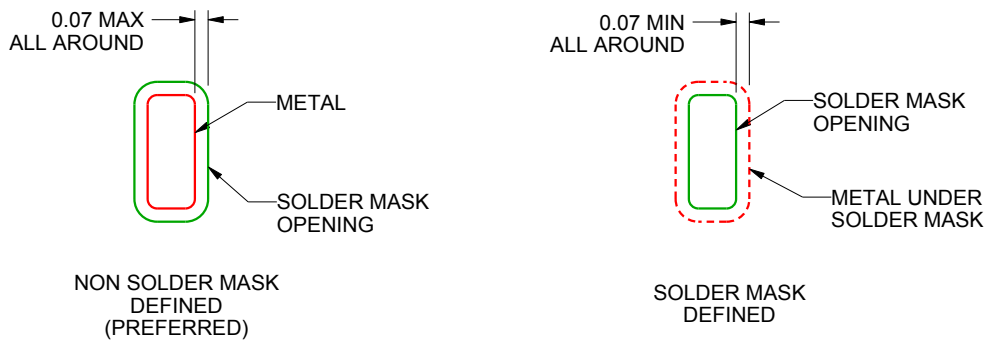
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

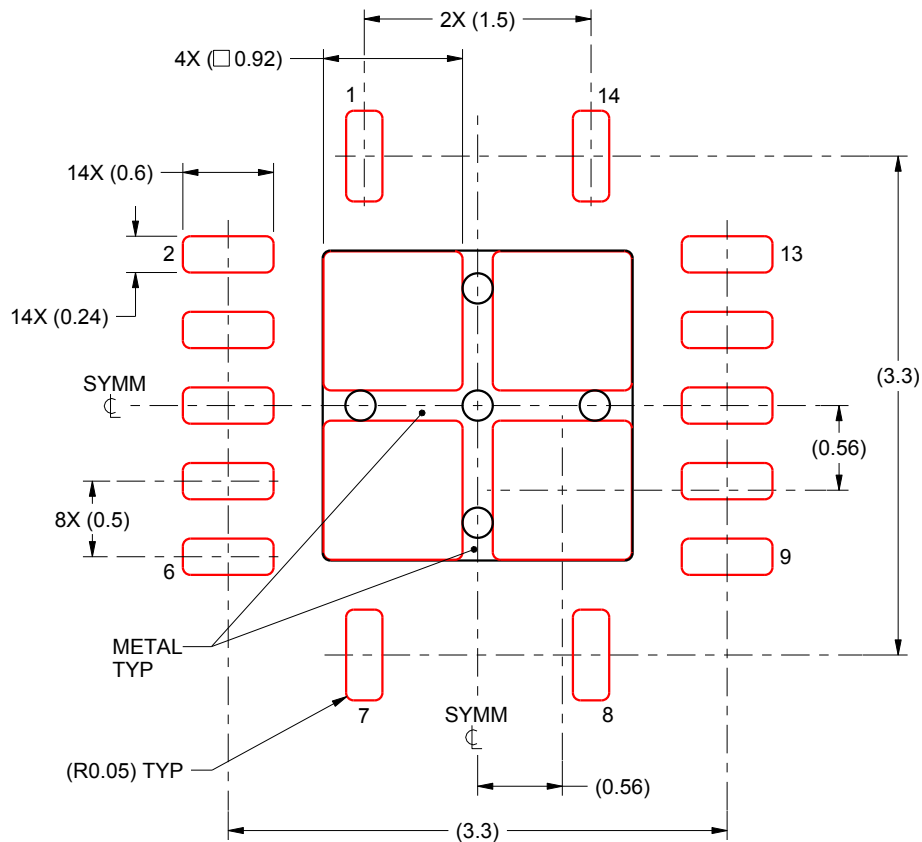
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

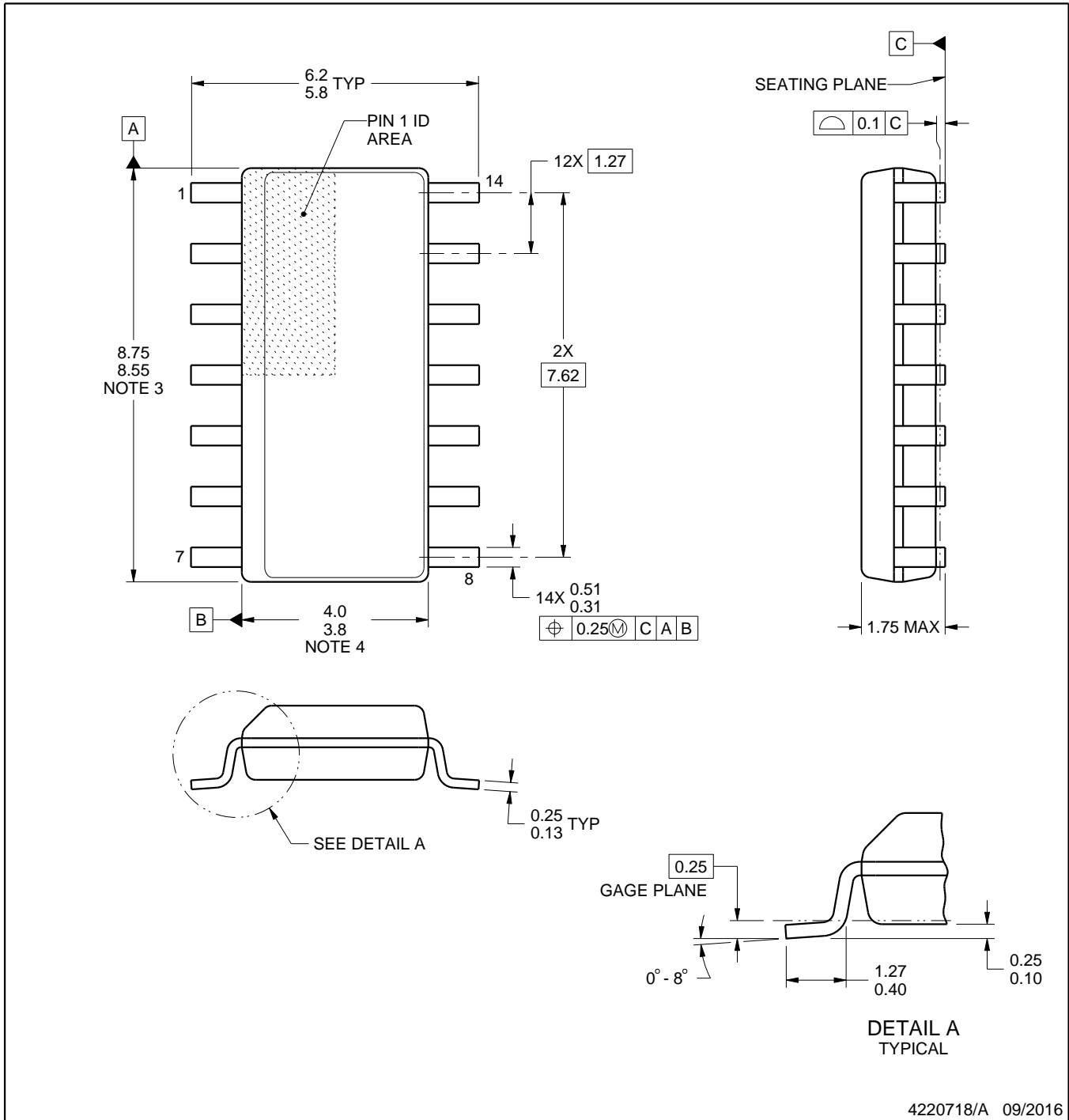
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

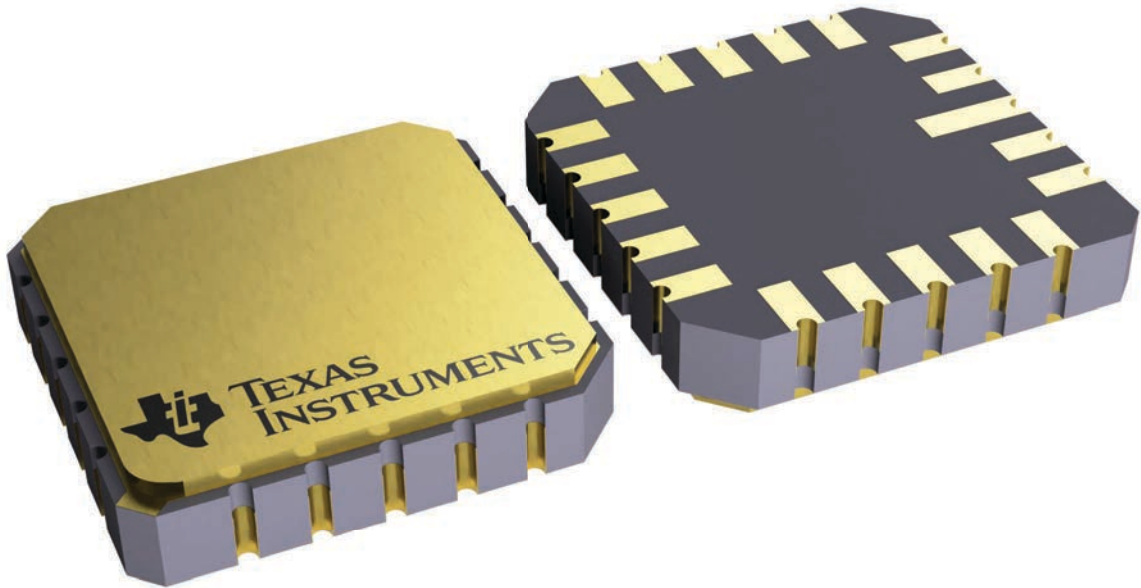
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

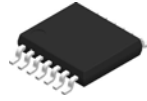
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

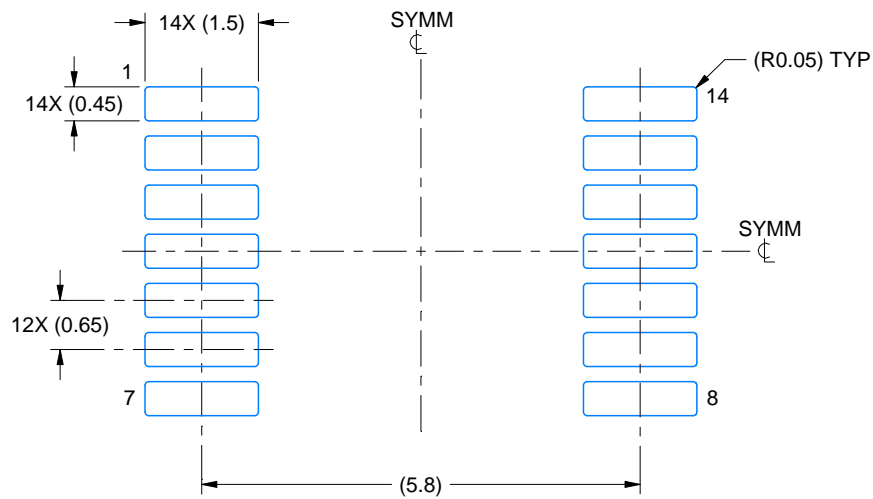
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

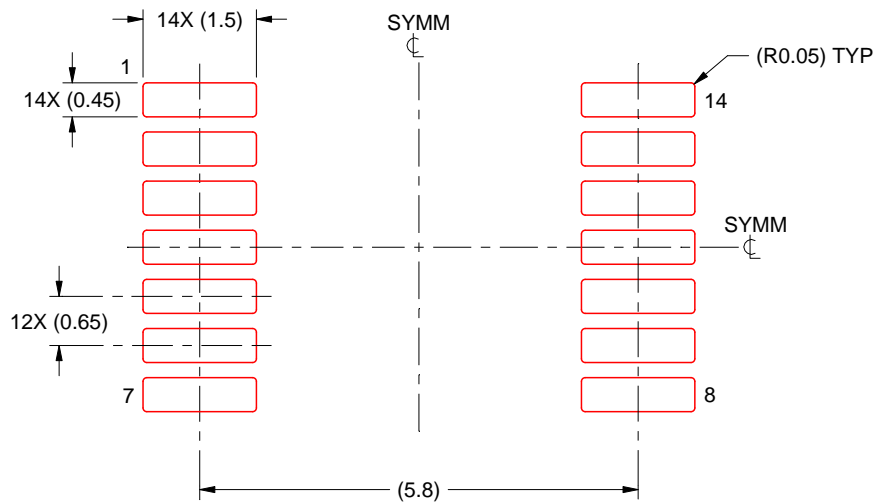
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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