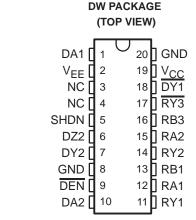
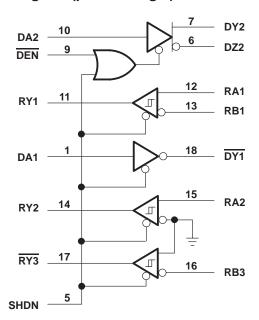
- Supports a 9-Pin GeoPort™ Host Interface Standard for the Intelligent Network Port
- Designed to Operate up to 4-Mbit/s Full **Duplex**
- ±5 V Supply Operation
- **Provides 6 kV ESD Protection**
- **Has Driver Short-Circuit Protection**
- Includes Failsafe Mechanism for Open Inputs
- Is Backward Compatible with AppleTalk™ and LocalTalk™
- **Combines Multiple Components into a** Single Chip Solution
- Complements the SN75LBC772 9-Pin **GeoPort Peripheral (DCE) Interface Device**
- Uses LinBiCMOS™ Process Technology

## description

The SN75LBC771 is a low-power LinBiCMOS™ device that incorporates the drivers and receivers for a 9-pin GeoPort host interface. GeoPort combines hybrid EIA/TIA-422-B and EIA/ TIA-423-B drivers and receivers to transmit data up to four-Mbit/s full duplex. GeoPort is a serial communications standard that is intended to replace the RS-232, AppleTalk, and printer ports all in one connector in addition to providing real-time data transfer capability. SN75LBC771 provides point-to-point connections between GeoPort-compatible devices with data transmission rates up to 4-Mbit/s full duplex featuring a hot-plug capability. Applications include connection to telephone, ISDN, digital sound and imaging, fax-data modems, and other traditional serial and parallel connections. The GeoPort is backwardly compatible to both LocalTalk and AppleTalk.



#### logic diagram (positive logic)



While the SN75LBC771 is powered off ( $V_{CC}$  and  $V_{EE} = 0$ ), the outputs are in a high-impedance state. Also, when the shutdown (SHDN) terminal is high, all outputs go into a high-impedance state. A logic high on the driver enable (DEN) terminal places the outputs of the differential driver into a high-impedance state. All drivers and receivers have fail-safe mechanisms that ensure a high output state when the inputs are left open.

The SN75LBC771 is characterized for operation over the 0°C to 70°C temperature range.



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#### **FUNCTION TABLES**†

	SINGLE-ENDED DRIVER									
INPUT (DA1)	ENABLE (SHDN)	OUTPUT (DY1)								
H L OPEN X X	L L H OPEN	L H L Z Z								

	DIFFERENTIAL DRIVER										
INPUT (DA2)	ENA (SHDN)	BLE (DEN)	OUT	PUT (DZ2)							
H	(OTIDIT)	(DEIV)	H	(DZZ)							
':'	L	L	L	Н							
OPEN	L	L	Н	L							
X	Н	Χ	Z	Z							
X	OPEN	Χ	Z	Z							
X	Х	Н	Z	Z							
Х	Х	OPEN	Z	Z							

SINGLED-ENDED RECEIVER									
INPUT (RA2, RA3)	ENABLE (SHDN)	OUTPUT (RY2) (RY3)							
Н	L	Н	L						
L	L	L	Н						
OPEN	L	Н	Н						
SHORT‡	L	?	?						
X	Н	Z	Z						
Х	OPEN	Z	Z						

	DIFFERENTIAL RECEIVER								
	INPUT ENABLE RA1) (RB1) (SHDN)		OUTPUT (RY1)						
Н	L	L	Н						
L	Н	L	L						
OP	EN	L	Н						
SHC	RT‡	L	?						
Х	Χ	Н	Z						
Х	Χ	OPEN	Z						

<sup>†</sup> H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Positive supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 to 7 V
Negative supply voltage range, VEE (see Note 1)	–7 to 0.5 V
Receiver input voltage range (RA, RB)	
· · · · · · · · · · · · · · · · · · ·	
Receiver differential input voltage range, V <sub>ID</sub>	
Receiver output voltage range (RY)	
Driver output voltage range (Power Off) (DY1, DY2, DZ2)	–15 V to 15 V
Driver output voltage range (Power On) (DY1, DY2, DZ2)	
Driver input voltage range (DA, SHDN, DEN)	
Electrostatic Discharge (see Note 2)	00
(All pins) Class 3, A	6 kV
(All pins) Class 3, B	
Continuous total power dissipation	
Operating free-air temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Lead temperature 1,0 min (1/10 men) nom case for 10 seconds	

<sup>§</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal unless otherwise noted.
  - 2. This rating is per MIL-STD-883C, Method 3015.7.



 $<sup>^{\</sup>ddagger}$ -0.2 V < V<sub>ID</sub> < 0.2 V

#### DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V <sub>CC</sub>	4.75	5	5.25	V
Negative supply voltage, VEE	-5.25	-5	-4.75	V
High-level input voltage, VIH (DA, SHDN, DEN)	2			V
Low-level input voltage, V <sub>IL</sub> (DA, SHDN, DEN)			0.8	V
Receiver common-mode input voltage, V <sub>IC</sub>	-7		7	V
Receiver differential input voltage, V <sub>ID</sub>	-12		12	V
Operating free-air temperature, T <sub>A</sub>	0		70	°C

# driver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V	High lovel output voltage		R <sub>L</sub> = 12 kΩ		3.6	4.5		V
Vон	High-level output voltage	Single-ended,	R <sub>L</sub> = 120 Ω		2	3.6		V
\/a.	Low lovel output voltage	See Figure 1	R <sub>L</sub> = 12 kΩ			-4.5	-3.6	V
VOL	Low-level output voltage		R <sub>L</sub> = 120 Ω			-3.6	-2	V
IVODI	Magnitude of differential output	t voltage	R <sub>L</sub> = 120 Ω,	See Figure 2	4			V
$\Delta  V_{OD} $	Change in differential voltage	magnitude					250	mV
Voc	Common-mode output voltage	;			-2		2	V
l∆Voc(ss)l	Magnitude of change, common steady-state output voltage	n-mode	See Figure 3				200	mV
ΔVOC(PP)	Magnitude of change, common peak-to-peak output voltage	n-mode		Ĭ		700		mV
Icc	Positive supply current			Noteed		4	10	mA
I <sub>EE</sub>	Negative supply current		$SHDN = \overline{DEN} = 0 \text{ V},$	No Load		-2	-5	mA
Icc	Positive supply current		OURN BEN SV	Noload			100	μΑ
IEE	Negative supply current		SHDN = DEN = 5 V,	No Load			-100	μΑ
loz	High-impedance output curren	t	$V_{CC} = 0 \text{ or } 5 \text{ V},$	-10 ≤ V <sub>O</sub> ≤ 10 V			±100	μΑ
los	Short-circuit output current		V <sub>CC</sub> = 5.25 V, See Note 3	$-5 \text{ V} \le \text{V}_{\text{O}} \le 5 \text{ V},$		±170	±450	mA

NOTE 3: Not more than one output should be shorted at one time.

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## driver switching characteristics over operating free-air temperature range

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPHL	Propagation delay time, high-to-low level output				42	75	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high level output				41	75	ns
tPZL	Driver output enable time to low-level output				25	100	μs
<sup>t</sup> PZH	Driver output enable time to high-level output	SHDN	Single ended,		25	100	μs
tPLZ	Driver output disable time from low-level output	SUDIN	See Figure 4		28	100	ns
tPHZ	Driver output disable time from high-level output	7			37	100	ns
t <sub>r</sub>	Rise time		1	10	25	75	ns
t <sub>f</sub>	Fall time		1	10	23	75	ns
tPHL	Propagation delay time, high-to-low level output				40	75	ns
tPLH	Propagation delay time, low-to-high level output		1		42	75	ns
4	Driver cutout enable time to level evel cutout	SHDN			25	100	μs
tPZL	Driver output enable time to low-level output	DEN	]		29	150	ns
4	Driver cutout enable time to high level cutout	SHDN			25	100	μs
<sup>t</sup> PZH	Driver output enable time to high-level output	DEN	Differential,		35	150	ns
4	Driver cutout disable time from level cutout	SHDN	See Figure 5		28	100	ns
<sup>t</sup> PLZ	Driver output disable time from low-level output	DEN	]		34	100	ns
4	Driver cuteut dischie time from high level cuteut	SHDN	1		37	100	ns
tPHZ	Driver output disable time from high-level output	DEN			34	100	ns
t <sub>r</sub>	Rise time		]	10	27	75	ns
t <sub>f</sub>	Fall time		<u> </u>	10	26	75	ns
tSK(p)	Pulse skew,  tpLH - tpHL					22	ns

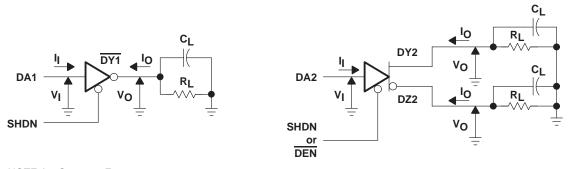
# receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>IT+</sub>	Positive-going input threshold voltage					200	mV
V <sub>IT</sub> _	Negative-going input threshold voltage	See Figure 6		-200			mV
V <sub>hys</sub>	Differential input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> )				50		mV
VOH	High-level output voltage (see Note 4)	V <sub>IC</sub> = 0, I <sub>OH</sub> = -	-2 mA,	2	4.5		V
VOL	Low-level output voltage	$V_{IC} = 0$ , $I_{OL} = 2$ See Figure 6	mA,		0.4	0.8	V
la a	Chart aire it autout aurent	V <sub>O</sub> = 0			-45	-85	mA
los	Short-circuit output current	V <sub>O</sub> = 5.25 V			45	85	mA
R <sub>IN</sub>	Input resistance	$V_{CC} = 0 \text{ or } 5.25 \text{ V}, -12 \text{ V} \le$	. V <sub>I</sub> ≤ 12 V	6	30		kΩ

NOTE 4: If the inputs are left unconnected, receivers one and two interpret this as a high-level input and receiver three interprets this as a low-level input so that all outputs are at the high level.

## receiver switching characteristics over recommended conditions (unless otherwise noted)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
tPHL	Propagation delay time, high-to-low level output					30	75	ns
tPLH	Propagation delay time, low-to-high level output		]			30	75	ns
t <sub>r</sub>	Rise time		$R_L = 2 kΩ$ , See Figure 6	$C_L = 15 pF,$		15	30	ns
t <sub>f</sub>	Fall time		Occ riguic o			15	30	ns
tSK(P)	Pulse skew  tpLH-tpHL		]				20	ns
tPZL	Receiver output enable time to low-level output					35	100	ns
tPZH	Receiver output enable time to high-level output					35	100	ns
tPLZ	Receiver output disable time from low-level output	Differential				20	100	ns
<sup>t</sup> PHZ	Receiver output disable time from high-level output	]		Caa Firuma 7		20	100	ns
tPZL	Receiver output enable time to low-level output		$C_L = 50 \text{ pF},$	See Figure 7		12	25	ns
<sup>t</sup> PZH	Receiver output enable time to high-level output	1				12	25	μs
t <sub>PLZ</sub>	Receiver output disable time from low-level output	Single-ended				25	100	μs
<sup>t</sup> PHZ	Receiver output disable time from high-level output					125	400	ns



NOTE A: C<sub>L</sub> = 50 pF

Figure 1. Single-Ended Driver DC Parameter Test Circuits

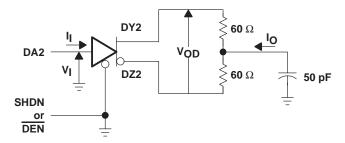
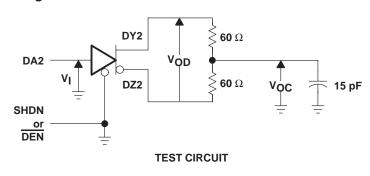
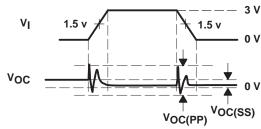


Figure 2. Differential Driver DC Parameter Test Circuit



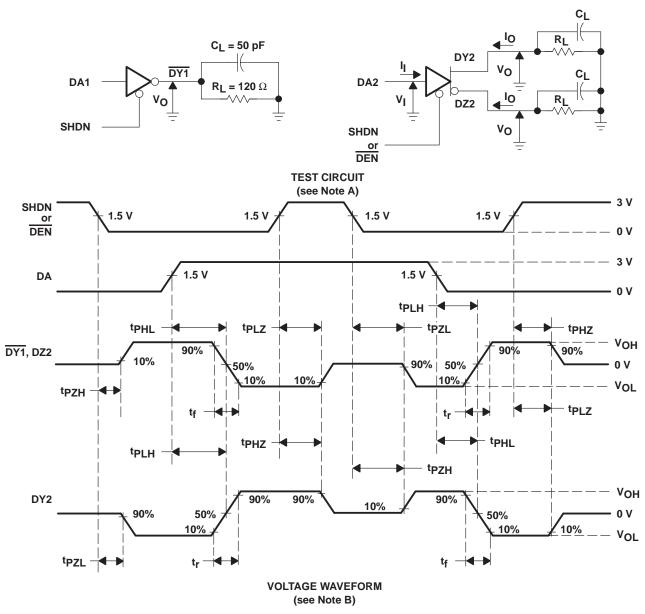


**VOLTAGE WAVEFORM** 

NOTE A: Measured 3dB Bandwidth = 300 MHz

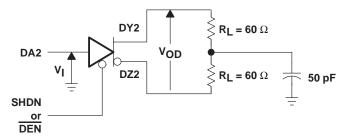
Figure 3. Differential Driver Common-Mode Output Voltage Test Circuit



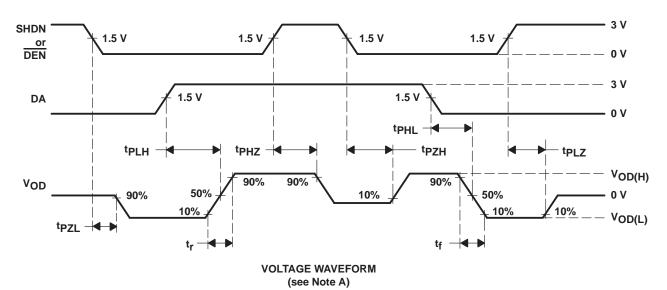


NOTES: A.  $C_L$  = 50 pF,  $R_L$  = 120  $\Omega$  B. The input waveform  $t_r$ ,  $t_f \le$  10 ns.

Figure 4. Single-Ended Driver Propagation and Transition Times Test Circuits and Waveform

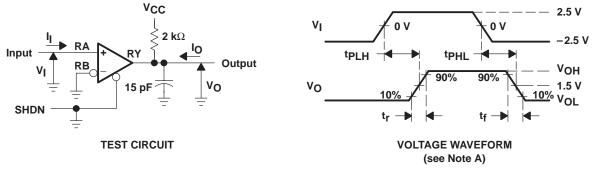


**TEST CIRCUIT** 



NOTE A: For the input waveform  $t_f$ ,  $t_f < = 10$  ns

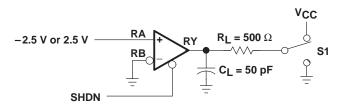
Figure 5. Differential Driver Propagation and Transition Times Test Circuit and Waveforms



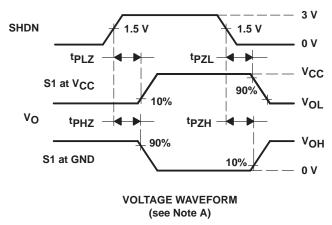
NOTE A: For the input waveform  $t_r$ ,  $t_f < = 10$  ns

Figure 6. Receiver Propagation and Transition Times Test Circuit and Waveform





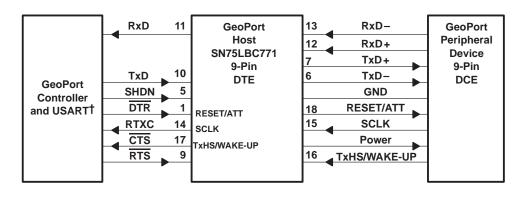
#### **TEST CIRCUIT**

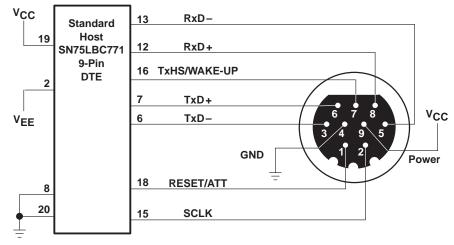


NOTE A: For the input waveform  $t_r$ ,  $t_f < = 10$  ns

Figure 7. Receiver Enable and Disable Test Circuit and Waveforms

#### **APPLICATION INFORMATION**





 $<sup>\</sup>dagger$  USART = universal synchronous asynchronous receiver transmitter

Figure 8. GeoPort 9-Pin DTE Connection Application

#### generator characteristics

PARAMETER		TEST O	TEST CONDITIONS		232/V.28		423/V.10		562	
	FARAMETER		CNDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		Open circuit			25	4	6		13.2	V
IVOI	Output voltage magnitude	$3 \text{ k}\Omega \leq \text{RL} \leq 7$	7 kΩ	5	15	NA		3.7		V
		R <sub>L</sub> = 450 Ω		NA		3.6		NA		V
los	Short-circuit output current	V <sub>O</sub> = 0			100		150		60	mA
R(OFF)	Power-off source resistance	$V_{CC} = 0$ ,	VO  < 2 V	300		NA		300		Ω
I <sub>O(OFF)</sub>	Power-off output current	$V_{CC} = 0$ ,	VO  < 6 V	NA			±100	NA		μΑ
SR	Output voltage slew rate				30	NA		4	30	V/μs
		±3.3 V to ±3.3	3 V	NA		NA		0.22	2.1	μs
t <sub>t</sub>	Output transition time	±3 V to ±3 V			0.04	NA		NA		ui‡
		10% to 90%	·	NA			0.3	NA		ui‡
VO(RING)	Output voltage ring		·	NA			10%		5%	·

<sup>‡</sup> ui is the unit interval and is the inverse of the signaling rate (bit time).



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### **APPLICATION INFORMATION**

### receiver characteristics

	PARAMETER	TEST CONDITIONS	232/V.28		423/V.10		562		UNIT
	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>I</sub>	Input voltage			25		10		25	V
VIT	Input voltage threshold	V <sub>I</sub>   < 15 V	-3	3	NA		-3	3	V
	input voitage triresnoid	V <sub>I</sub>   < 10 V	NA		-0.2	0.2	NA		V
Rį	Innut registance	3 V <  V <sub>I</sub>   < 15 V	3	7	NA		3	7	kΩ
	Input resistance	V <sub>I</sub>   < 10 V	NA		4		NA		kΩ

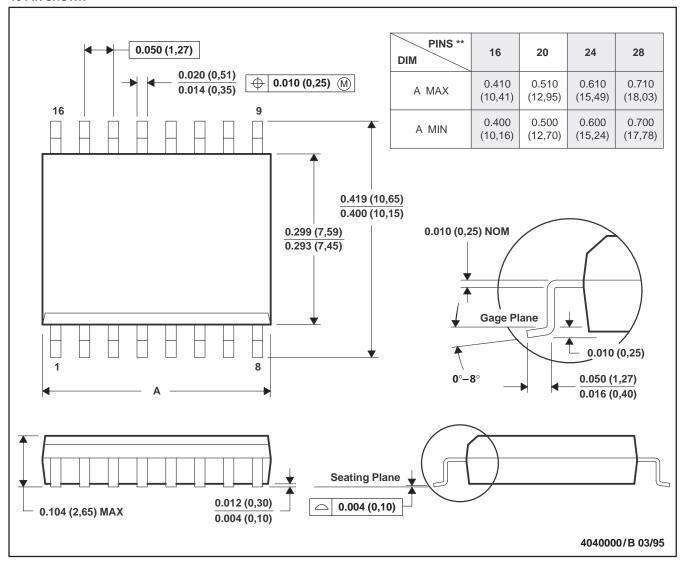
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#### **MECHANICAL INFORMATION**

#### DW (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

**16 PIN SHOWN** 



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013



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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN75LBC771DW	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC771
SN75LBC771DW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC771

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LBC771DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75LBC771DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC771DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC771DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6

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