



HIGH EFFICIENCY CLASS-G ADSL LINE DRIVER

FEATURES

- Low Total Power Consumption Increases ADSL Line Card Density (20 dBm on Line)
 - 600 mW w/Active Termination (Full Bias)
 - 530 mW w/Active Termination (Low Bias)
- Low MTPR of -74 dBc (All Bias Conditions)
- High Output Current of 500 mA (typ)
- Wide Supply Voltage Range of ± 5 V to ± 15 V [$V_{CC(H)}$] and ± 3.3 V to ± 15 V [$V_{CC(L)}$]
- Wide Output Voltage Swing of 43 Vpp Into 100- Ω Differential Load [$V_{CC(H)} = \pm 12$ V]
- Multiple Bias Modes Allow Low Quiescent Power Consumption for Short Line Lengths
 - 160-mW/ch Full Bias Mode
 - 135-mW/ch Mid Bias Mode
 - 110-mW/ch Low Bias Mode
 - 75-mW/ch Terminate Only Mode
 - 13-mW/ch Shutdown Mode
- Low Noise for Increased Receiver Sensitivity
 - $3.3 \text{ pA}/\sqrt{\text{Hz}}$ Noninverting Current Noise
 - $9.5 \text{ pA}/\sqrt{\text{Hz}}$ Inverting Current Noise
 - $3.5 \text{ nV}/\sqrt{\text{Hz}}$ Voltage Noise

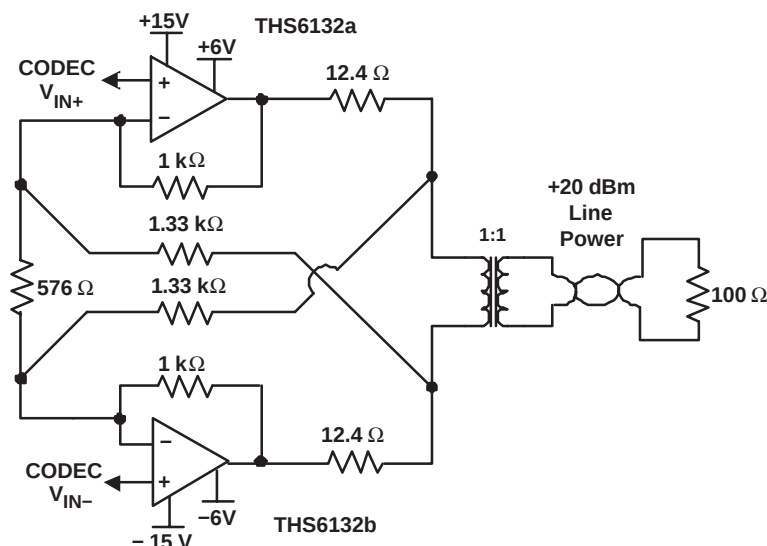
APPLICATIONS

- Ideal for Active Termination Full Rate ADSL DMT applications (20-dBm Line Power)

DESCRIPTION

The THS6132 is a Class-G current feedback differential line driver ideal for full rate ADSL DMT systems. Its extremely low power consumption of 600 mW or lower is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique patent pending architecture of the THS6132 allows the quiescent current to be much lower than existing line drivers while still achieving very high linearity. In addition, the multiple bias settings of the amplifiers allow for even lower power consumption for line lengths where the full performance of the amplifier is not required. The output voltage swing has been vastly improved over first generation Class-G amplifiers and allows the use of lower power supply voltages that help conserve power. For maximum flexibility, the THS6132 can be configured in classical Class-AB mode requiring only as few as one power supply.

Typical ADSL CO Line Driver Circuit Utilizing Active Impedance Supporting A 6.3 Crest Factor



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	T _A	ORDER NUMBER	TRANSPORT MEDIA
THS6132VFP	TQFP-32 PowerPAD™	VFP-32	THS6132	-40°C to 85°C	THS6132VFP	Tube
					THS6132VFPR	Tape and reel
THS6132RGW	Leadless 25-pin 5,mm x 5, mm PowerPAD™	RGW-25	6132		THS6132RGWR	Tape and reel

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ _{JA}	Θ _{JC}	T _A ≤ 25°C POWER RATING(1)	T _A = 70°C POWER RATING(1)	T _A = 85°C POWER RATING(1)
VFP-32	29.4°C/W	0.96°C/W	3.57 W	2.04 W	1.53 W
RGW-25	31°C/W	1.7°C/W	3.39 W	1.94 W	1.45 W

(1) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		THS6132
Supply voltage, V _{CC(H)} and V _{CC(L)} (2)		±16.5 V
Input voltage, V _I		±V _{CC(L)}
Output current, I _O (3)		900 mA
Differential input voltage, V _{IO}		±2 V
Maximum junction temperature, T _J (see Dissipation Rating Table for more information)		150°C
Operating free-air temperature, T _A		-40°C to 85°C
Storage temperature, T _{Stg}		65°C to 150°C
Lead temperature, 1,6 mm (1/16-inch) from case for 10 seconds		300°C
ESD ratings	HBM	1 kV
	CDM	500 V
	MM	200 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) V_{CC(H)} must always be greater than or equal to V_{CC(L)} for proper operation. Class-AB mode operation occurs when V_{CC(H)} is equal to V_{CC(L)} and is considered acceptable operation for the THS6132 even though it is not fully specified in this mode of operation.

(3) The THS6132 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	+V _{CC(H)} to -V _{CC(H)}	±V _{CC(L)}	±15	±16	V
	+V _{CC(L)} to -V _{CC(L)}	±3.3	±5	±V _{CC(H)}	
Operating free-air temperature, T _A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C, V_{CC(H)} = ±15 V, V_{CC(L)} = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

NOISE/DISTORTION PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Multitone power ratio		Gain =+11, 163kHz to 1.1MHz DMT, +20 dBm Line Power, 1:1.1 transformer, active termination, synthesis factor = 4			-74		dBc
Receive band spill-over		Gain =+11, 25 kHz to 138 kHz with MTPR signal applied			-95		dBc
HD	Harmonic distortion (Differential Configuration, f = 1 MHz, V _O (PP) = 2 V, Gain = +10)	2 nd harmonic	Differential load = 100 Ω		-84		dBc
			Differential load = 25 Ω		-69		
		3 rd harmonic	Differential load = 100 Ω		-92		dBc
			Differential load = 25 Ω		-73		
V _n	Input voltage noise	f = 10 kHz			3.5		nV/√Hz
I _n	Input current noise	+Input	f = 10 kHz		3.3		pA/√Hz
		-Input			9.5		
Crosstalk		f = 1 MHz, R _L = 100 Ω,	V _O (PP) = 2 V, Gain = +2		-52		dBc
OUTPUT CHARACTERISTICS							
V _O	Single-ended output voltage swing	V _{CC} (H) = ±12 V	R _L = 100 Ω	±10.4	±10.8		V
			R _L = 30 Ω	±9.9	±10.4		
		V _{CC} (H) = ±15 V	R _L = 100 Ω	±13.3	±13.8		V
			R _L = 50 Ω	±13	±13.6		
Output voltage transition from V _{CC} (L) to V _{CC} (H) (Point where I _{CC} (L) = I _{CC} (H))		R _L = 50 Ω	V _{CC} (L) = ±5 V		±3.1		V
			V _{CC} (L) = ±6 V		±3.9		
I _O	Output current (1)	R _L = 10 Ω	V _{CC} (H) = ±12 V		±500		mA
			V _{CC} (H) = ±15 V	±400	±500		
I _(SC)	Short-circuit current (1)	R _L = 1 Ω	V _{CC} (H) = ±15 V		±750		mA
Output resistance		Open-loop			5		Ω
Output resistance—terminate mode		f = 1 MHz,	Gain = +10		0.35		Ω
Output resistance—shutdown mode		f = 1 MHz,	Open-loop		5.5		kΩ

(1) A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$, $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\text{ }\Omega$ (unless otherwise noted)

POWER SUPPLY						
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX
$V_{CC(x)}$	Operating range	$\pm V_{CC(H)}$		$\pm V_{CC(L)}$	± 15	± 16.5
		$\pm V_{CC(L)}$		± 3	± 5	$\pm V_{CC(H)}$
I_{CC}	Quiescent current (each driver) Full-bias mode (Bias-1 = 1, Bias-2 = 1, Bias-3 = X) (I_{CC} trimmed with $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$)	$V_{CC(L)} = \pm 5\text{ V};$ ($V_{CC(H)} = \pm 15\text{ V}$)	$T_A = 25^\circ\text{C}$	5.7	6.4	7.5
			$T_A = \text{full range}$			8.1
		$V_{CC(L)} = \pm 6\text{ V};$ ($V_{CC(H)} = \pm 15\text{ V}$)	$T_A = 25^\circ\text{C}$		6.7	
			$T_A = \text{full range}$			
		$V_{CC(H)} = \pm 12\text{ V};$ ($V_{CC(L)} = \pm 5\text{ V}$)	$T_A = 25^\circ\text{C}$		3.1	
			$T_A = \text{full range}$			
		$V_{CC(H)} = \pm 15\text{ V};$ ($V_{CC(L)} = \pm 5\text{ V}$)	$T_A = 25^\circ\text{C}$	2.9	3.25	3.75
			$T_A = \text{full range}$			4.25
	Quiescent current (each driver) Variable bias modes, $V_{CC(L)} = \pm 5\text{ V}$	Mid; Bias-1 = 1, Bias-2 = 0, Bias-3 = 1		5.0	5.6	6.8
		Low; Bias-1 = 1, Bias-2 = 0, Bias-3 = 0		4.25	4.8	6.0
		Terminate; Bias-1 = 0, Bias-2 = 1, Bias-3 = X ⁽¹⁾		3.2	3.8	4.5
		Shutdown; Bias-1 = 0, Bias-2 = 0, Bias-3 = X ⁽¹⁾			1	1.3
	Quiescent current (each driver) Variable bias modes, $V_{CC(H)} = \pm 15\text{ V}$	Mid; Bias-1 = 1, Bias-2 = 0, Bias-3 = 1		2.4	2.7	3.0
		Low ; Bias-1 = 1, Bias-2 = 0, Bias-3 = 0		1.9	2.15	2.4
		Terminate; Bias-1 = 0, Bias-2 = 1, Bias-3 = X ⁽¹⁾		1.1	1.3	1.5
		Shutdown ; Bias-1 = 0, Bias-2 = 0, Bias-3 = X ⁽¹⁾			0.1	0.5
PSRR	Power supply rejection ratio ($\Delta V_{CC(x)} = \pm 1\text{ V}$)	$V_{CC(L)} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	-70	-82	
			$T_A = \text{full range}$	-68		
		$V_{CC(H)} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	-70	-82	
			$T_A = \text{full range}$	-68		

(1) X is used to denote a logic state of either 1 or 0.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$, $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\text{ }\Omega$ (unless otherwise noted)

DYNAMIC PERFORMANCE						
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX
BW	Single-ended small-signal bandwidth (-3 dB), $V_O = 0.1\text{ V}_{\text{rms}}$	$R_L = 100\text{ }\Omega$	Gain = +1, $R_F = 750\text{ }\Omega$		80	
			Gain = +2, $R_F = 620\text{ }\Omega$		70	
			Gain = +5, $R_F = 500\text{ }\Omega$		60	
			Gain = +10, $R_F = 1\text{ k}\Omega$		20	
		$R_L = 25\text{ }\Omega$	Gain = +1, $R_F = 750\text{ }\Omega$		60	
			Gain = +2, $R_F = 620\text{ }\Omega$		55	
			Gain = +5, $R_F = 500\text{ }\Omega$		50	
			Gain = +10, $R_F = 1\text{ k}\Omega$		17	
SR	Single-ended slew-rate ⁽¹⁾	$V_O = 20\text{ V}_{\text{PP}}$	Gain = +10		300	
						V/ μs

(1) Slew-rate is defined from the 25% to the 75% output levels

DC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage	V _{CC(L)} = ± 5 V, ±6 V	T _A = 25°C		1	15	mV
			T _A = full range			20	
	Differential offset voltage		T _A = 25°C		0.3	6	
			T _A = full range			8	
	Offset drift		T _A = full range		40		μV/°C
I _{IB}	−Input bias current	V _{CC(L)} = ±5 V, ±6 V	T _A = 25°C		1	15	μA
	+ Input bias current		T _A = full range			20	
			T _A = 25°C		1.5	15	
			T _A = full range			20	
Z _{OL}	Open loop transimpedance	R _L = 1 kΩ			2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$, $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\text{ }\Omega$ (unless otherwise noted)

INPUT CHARACTERISTICS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{ICR}	Input common-mode voltage range(1)	V _{CC(L)} = ±5 V	T _A = 25°C	±2.7	±3.0		V
			T _A = full range	±2.6			
		V _{CC(L)} = ±6 V	T _A = 25°C		±4.0		
REF pin input voltage range		V _{CC-(L)} = ±5 V			±2.5		V
		V _{CC(L)} = ±6 V			±3.5		
CMRR	Common-mode rejection ratio	V _{CC(L)} = ±5 V, ±6 V	T _A = 25°C	60	67		dB
			T _A = full range	57			
R _I	Input resistance	+ Input			800		kΩ
		– Input			45		Ω
C _I	Differential Input capacitance				1.2		pF

(1) To conserve as much power as possible, the input stage of the THS6132 is powered from the $V_{CC(L)}$ supplies and is limited by the $V_{CC(L)}$ supply voltage. For Class-AB operation, connect the $V_{CC(L)}$ supplies to $V_{CC(H)}$.

LOGIC CONTROL CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Bias pin voltage for logic 1	Relative to DGND pin voltage	2.0			V
V _{IL}	Bias pin voltage for logic 0	Relative to DGND pin voltage			0.8	V
I _{IH}	Bias pin current for logic 1	V _{IH} = 5 V, DGND = 0 V		–0.1	–0.2	μA
I _{IL}	Bias pin current for logic 0	V _{IL} = 0 V, DGND = 0 V		–0.1	–0.2	μA
Transition time—logic 0 to logic 1 ⁽¹⁾				0.1		μs
Transition time—logic 1 to logic 0 ⁽¹⁾				0.2		μs
DGND useable range			–V _{CC(H)}		+V _{CC(H)} –5	V

(1) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE				
BIAS-1	BIAS-2	BIAS-3	FUNCTION	DESCRIPTION
1	1	X ⁽¹⁾	Full bias mode	Amplifiers ON with lowest distortion possible
1	0	1	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
1	0	0	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
0	1	X ⁽¹⁾	Terminate mode	Lowest power state with +Vin pins internally connect to REF pin and output has low impedance
0	0	X ⁽¹⁾	Shutdown mode	Amplifiers OFF and output has high impedance

(1) X is used to denote a logic state of either 1 or 0.

NOTE: The default state for all logic pins is a logic one (1).

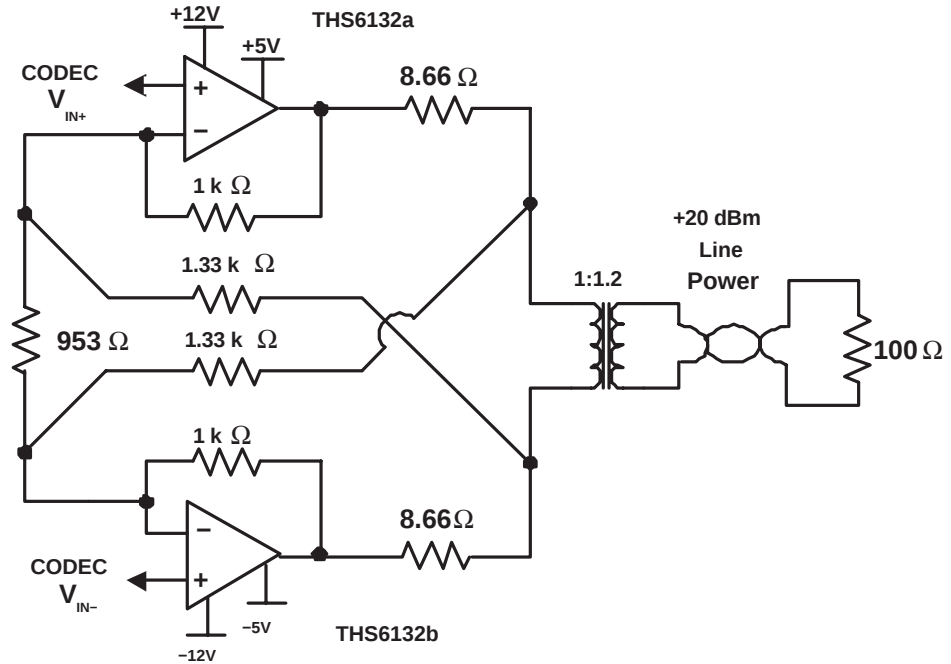
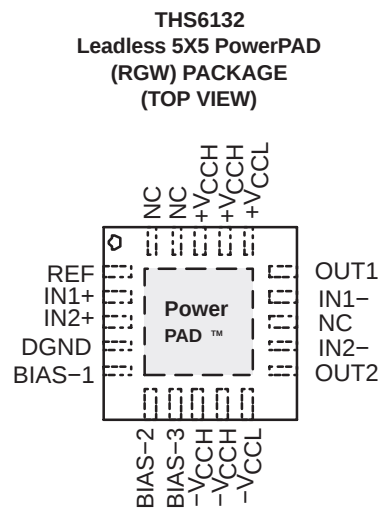
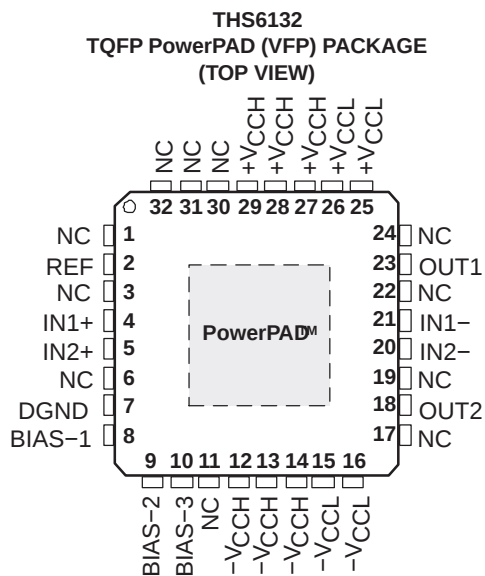


Figure 1. ± 12 V Active Termination ADSL CO Line Driver Circuit (Synthesis Factor = 4; CF = 5.6)

PIN ASSIGNMENTS



TYPICAL CHARACTERISTICS

Table of Graphs

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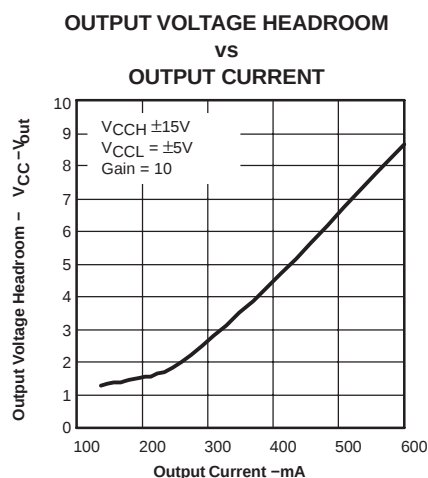


Figure 2

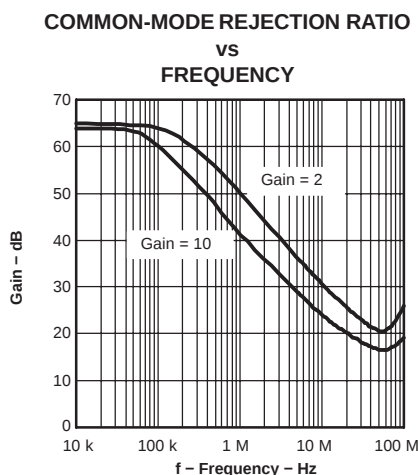


Figure 3

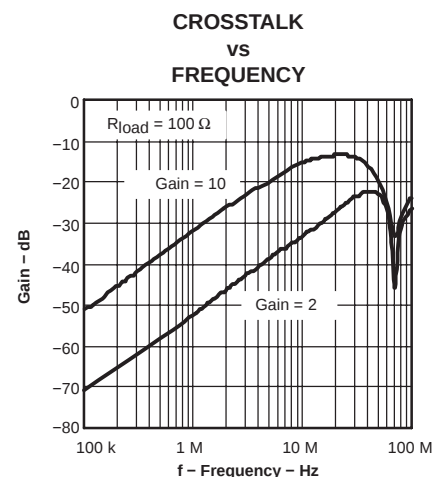


Figure 4

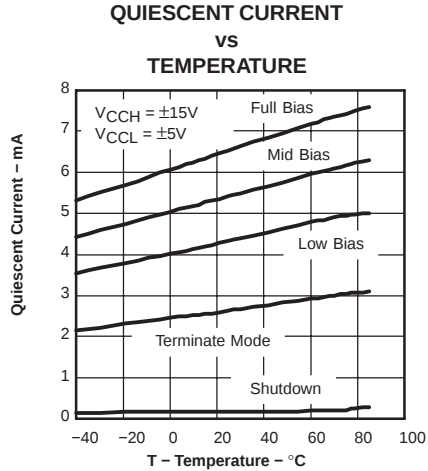


Figure 5

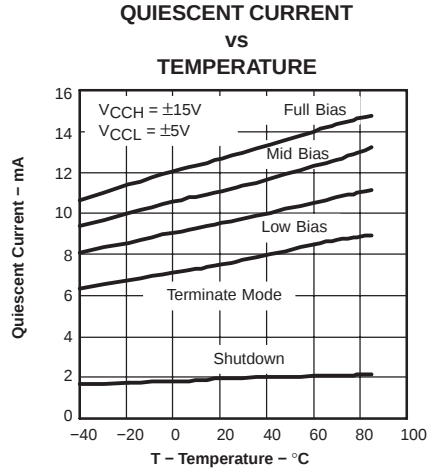


Figure 6

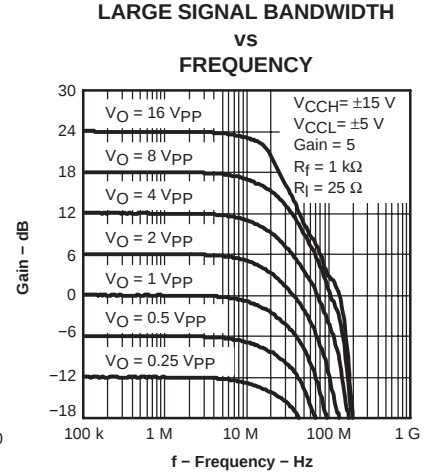


Figure 7

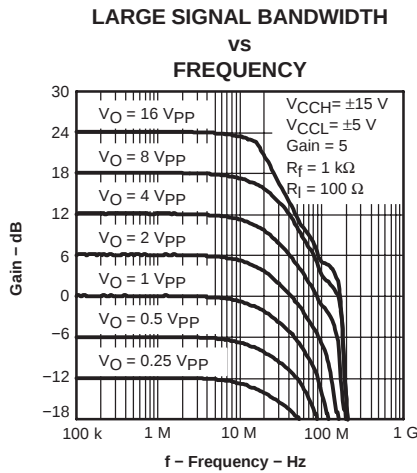


Figure 8

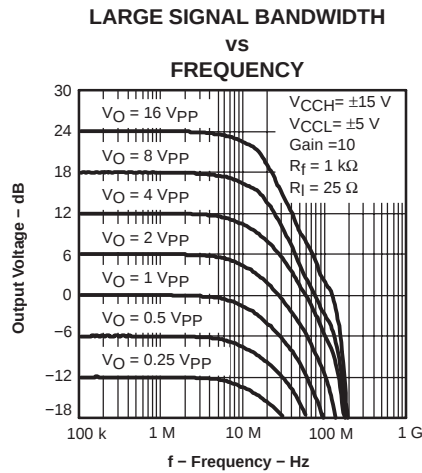


Figure 9

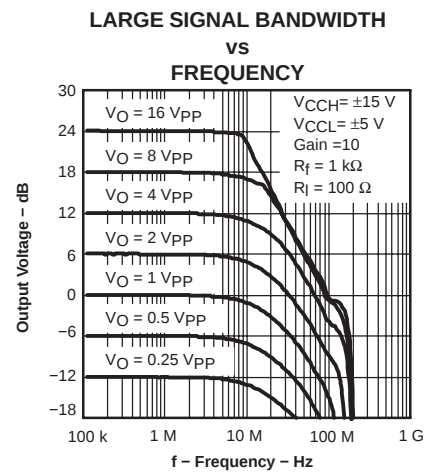


Figure 10

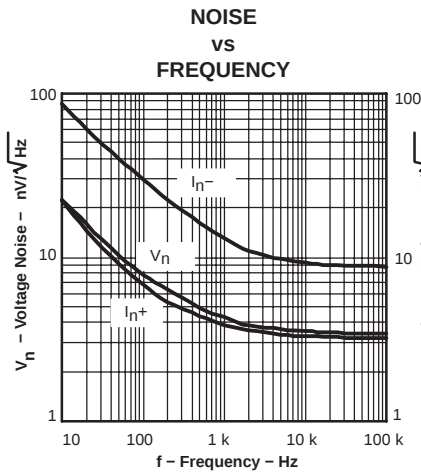


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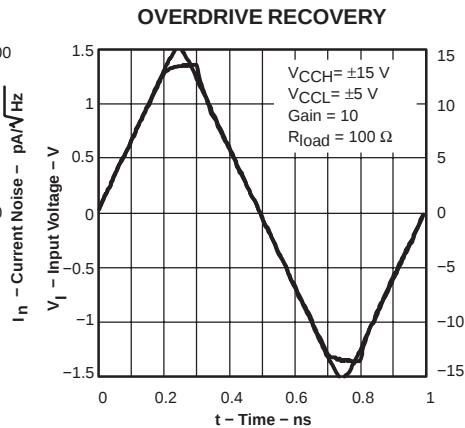


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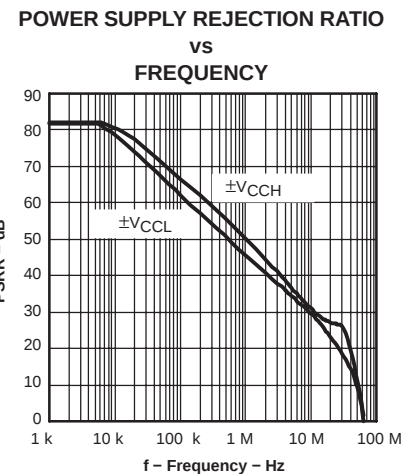


Figure 13

SMALL SIGNAL FREQUENCY RESPONSE

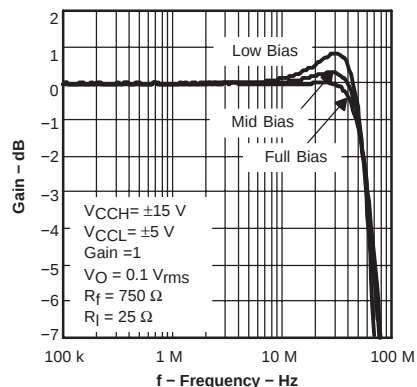


Figure 14

SMALL SIGNAL FREQUENCY RESPONSE

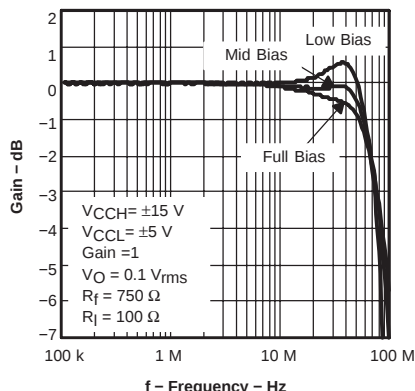


Figure 15

SMALL SIGNAL FREQUENCY RESPONSE

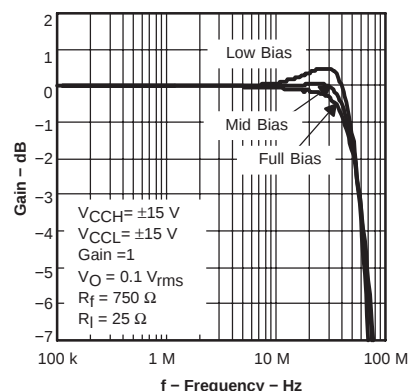


Figure 16

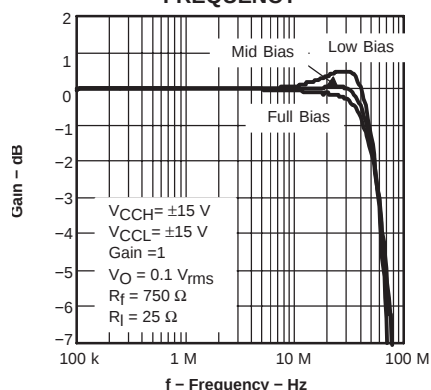
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 17

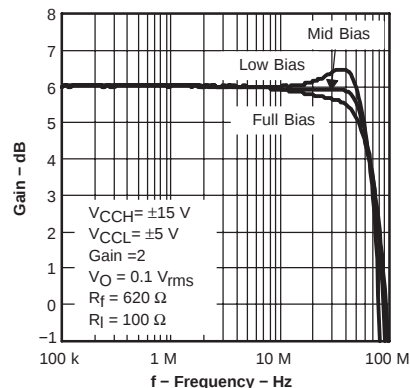
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 18

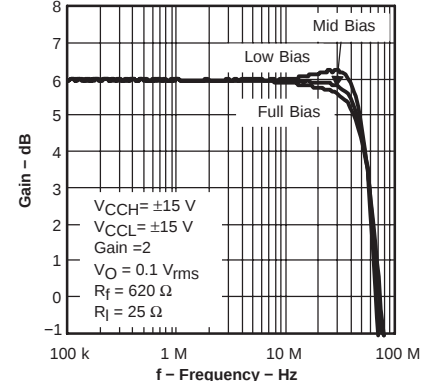
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 19

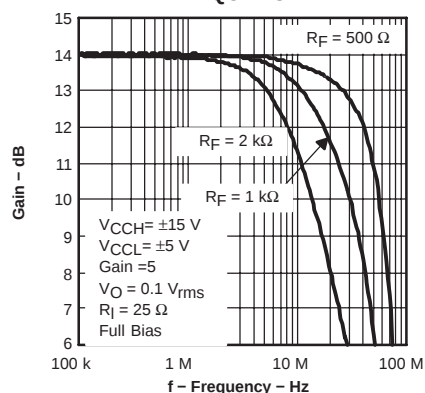
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 20

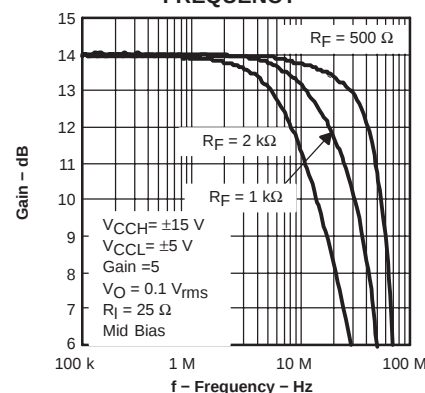
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 21

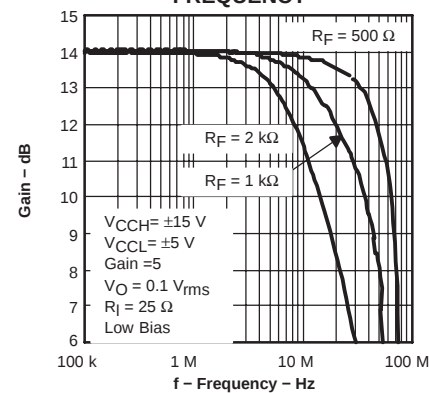
SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

Figure 22

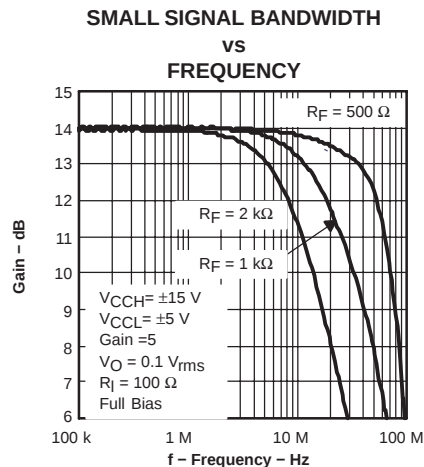


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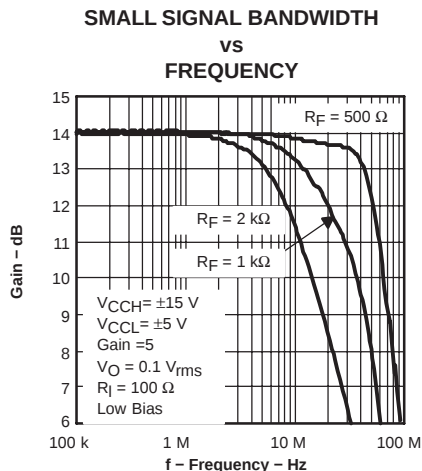


Figure 24

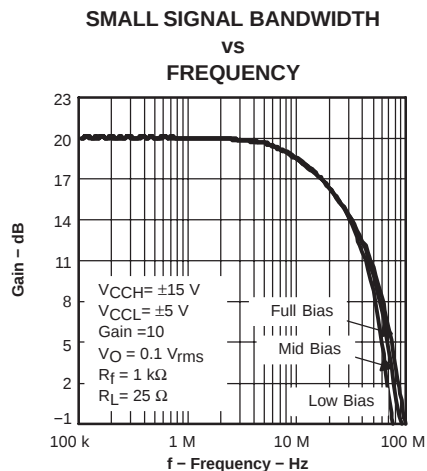


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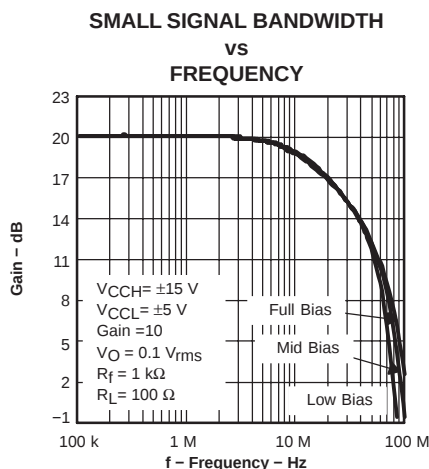


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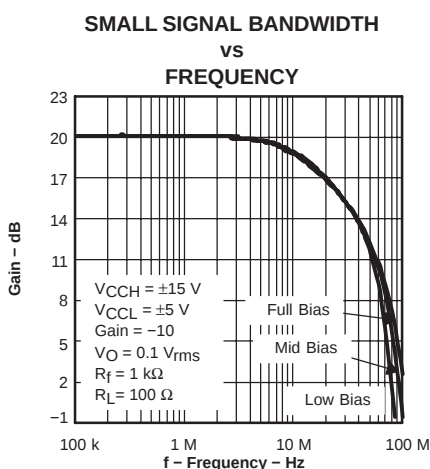


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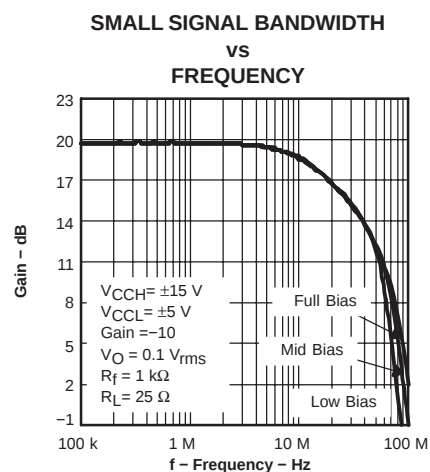


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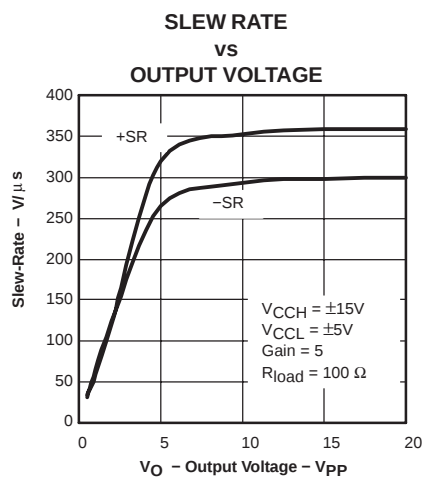


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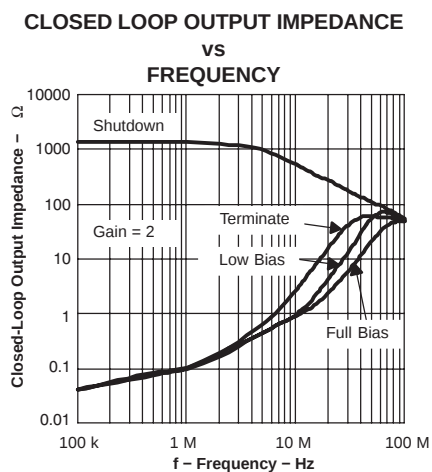


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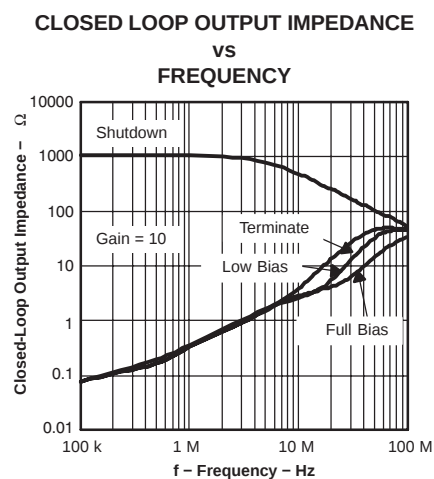


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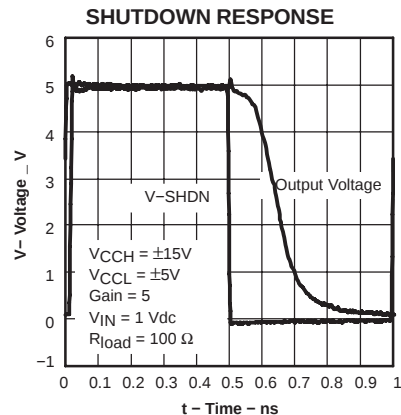


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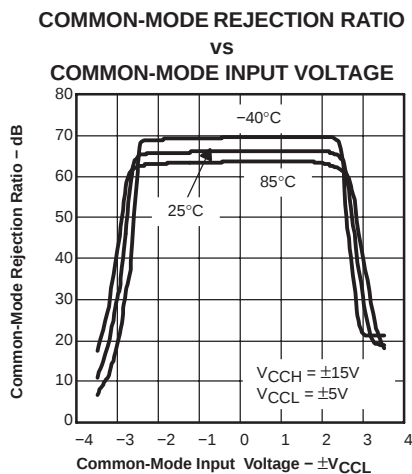


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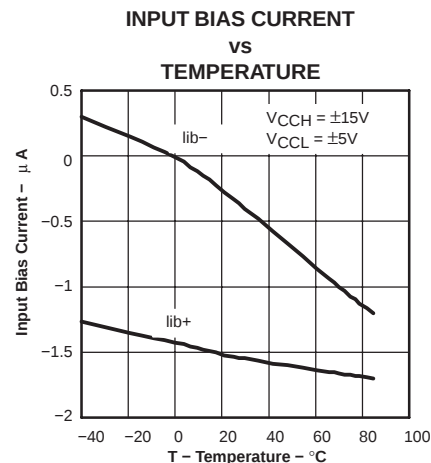


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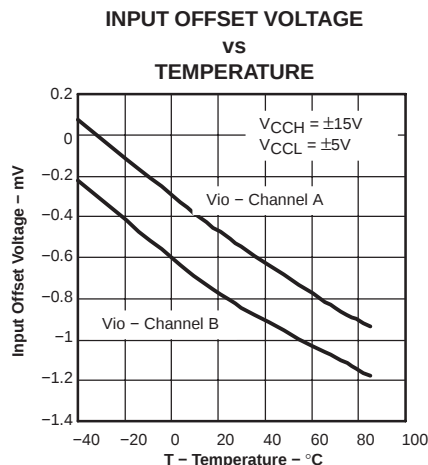


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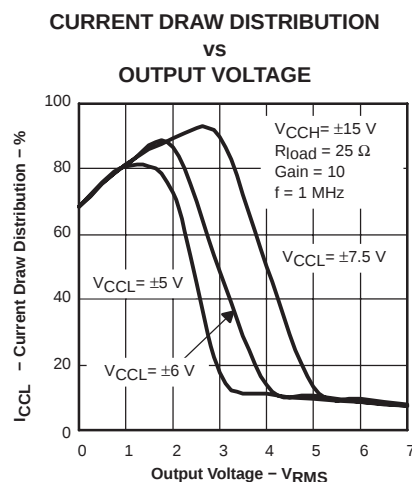


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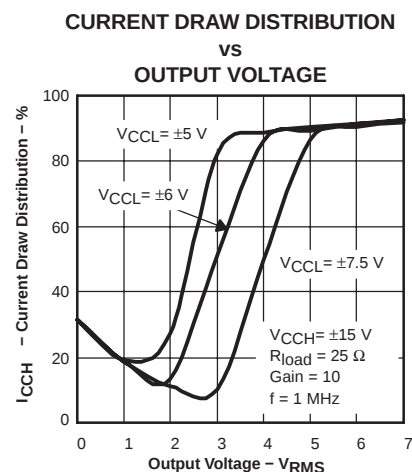


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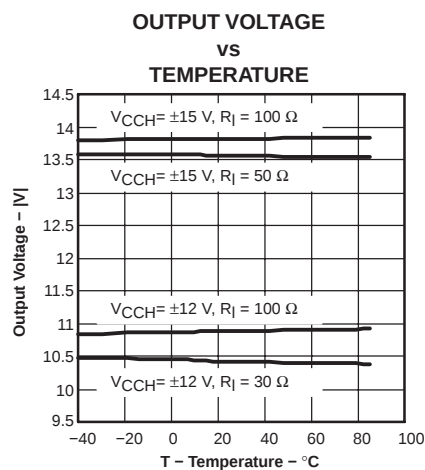


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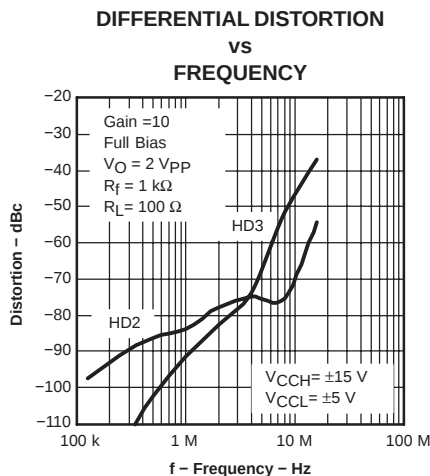


Figure 39

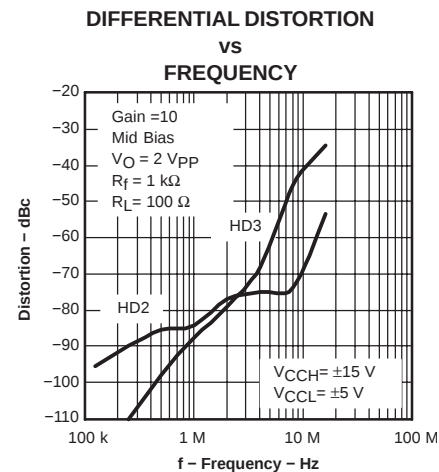


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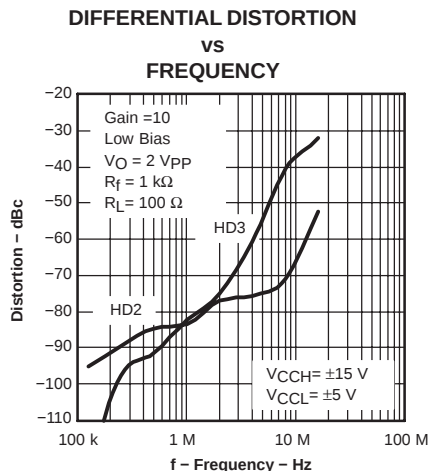


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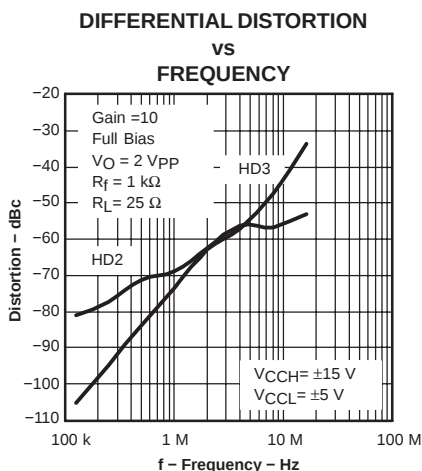


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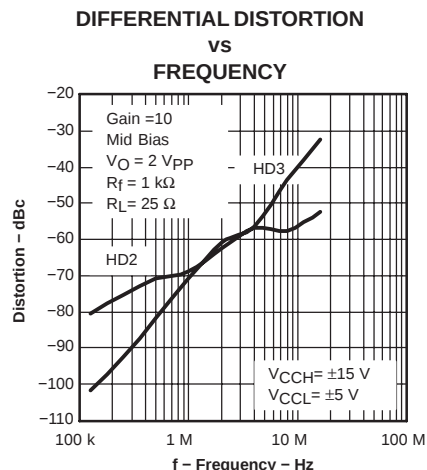


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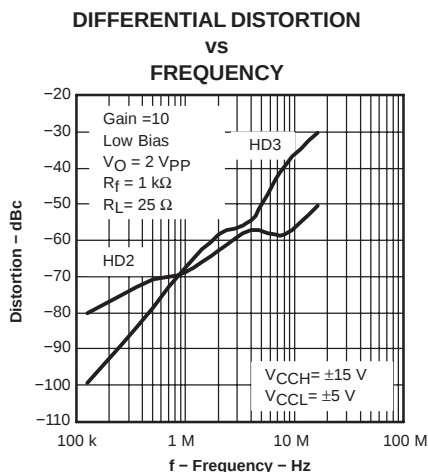


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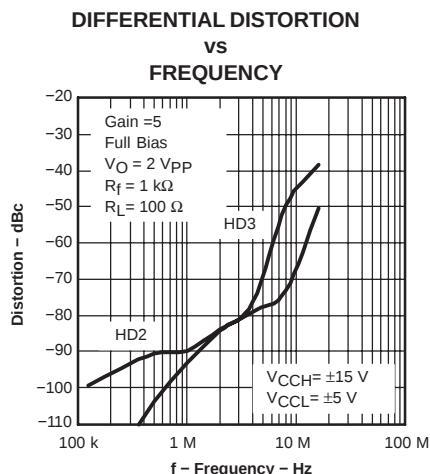


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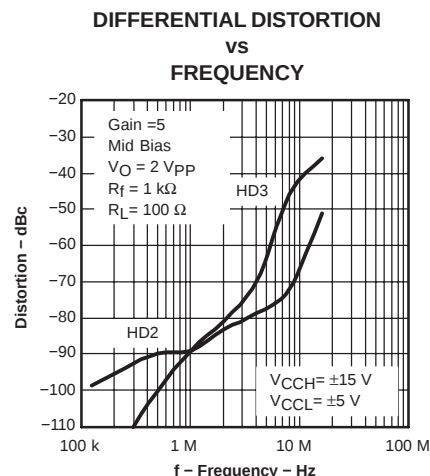


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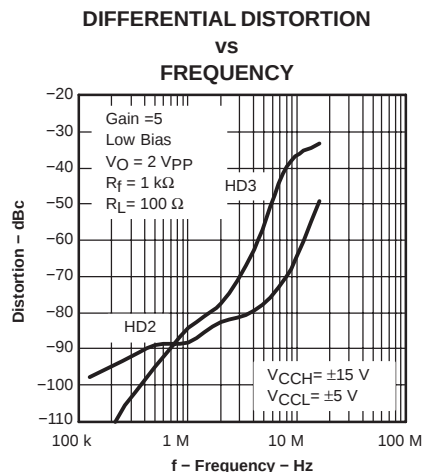


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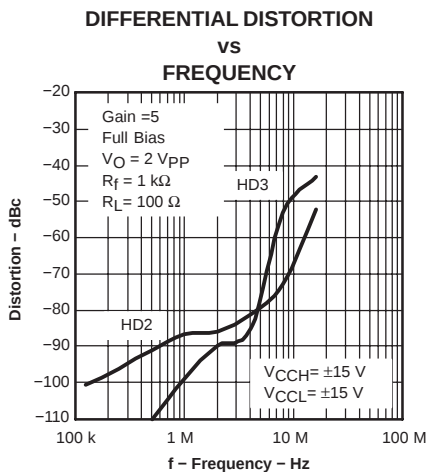


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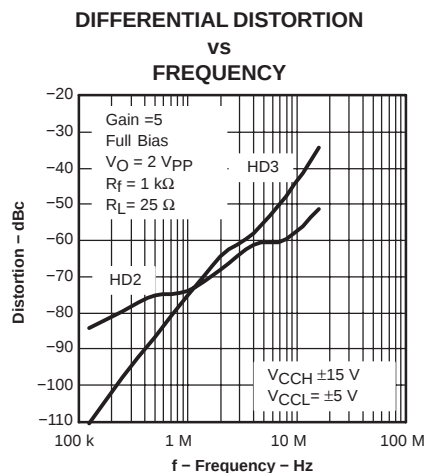


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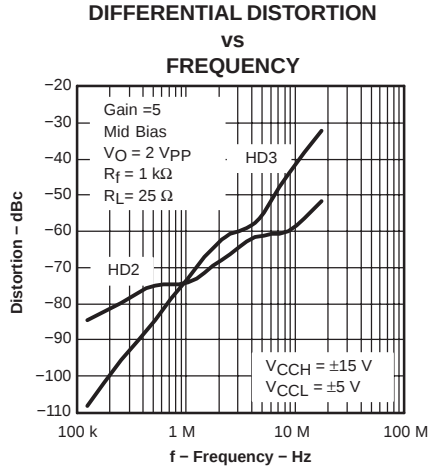


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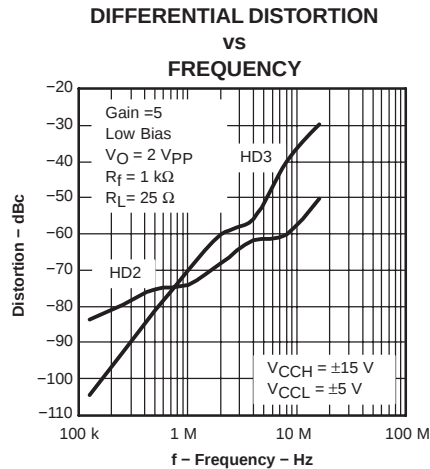


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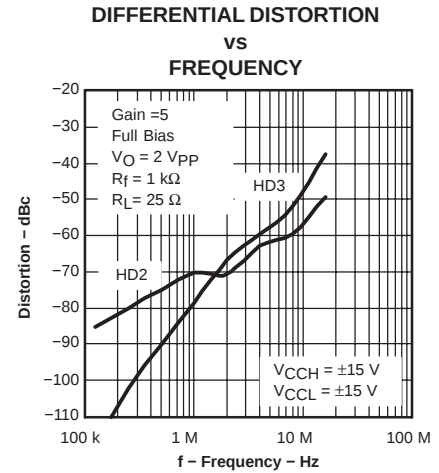


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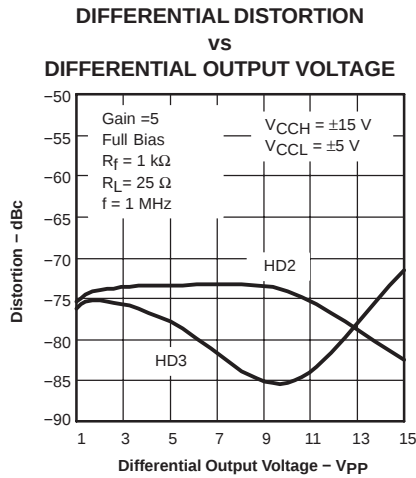


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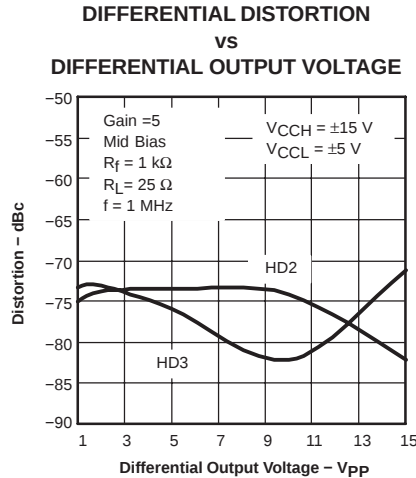


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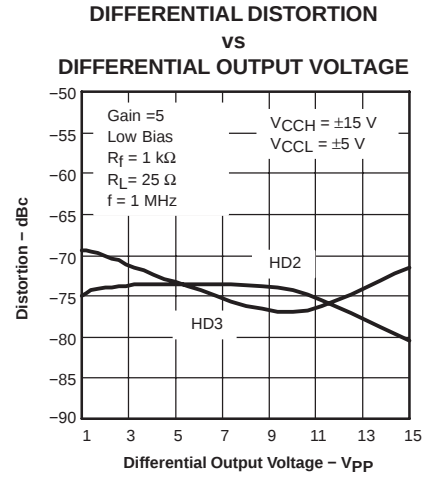


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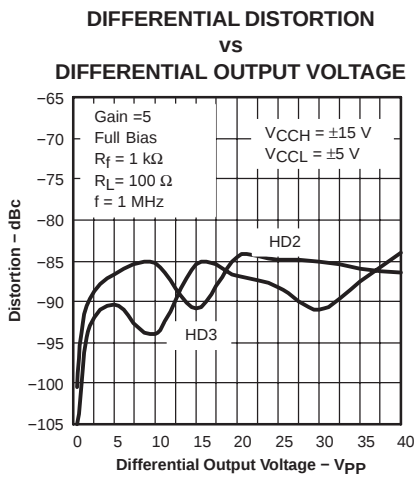


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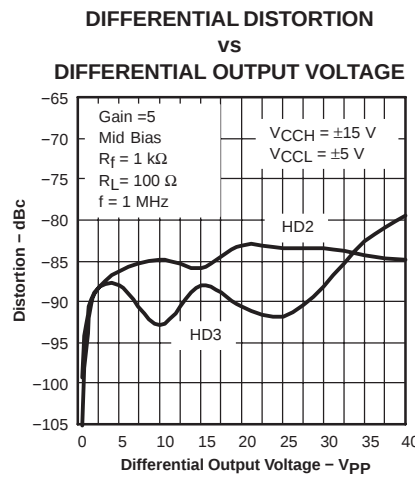


Figure 57

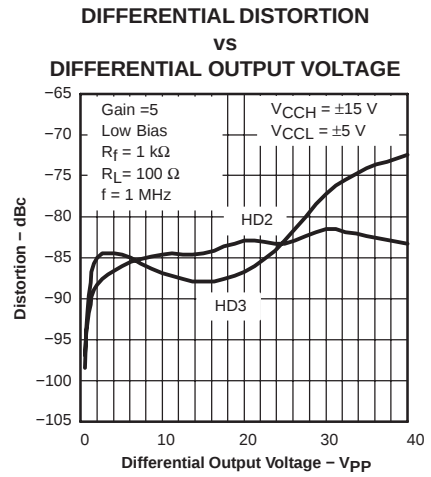


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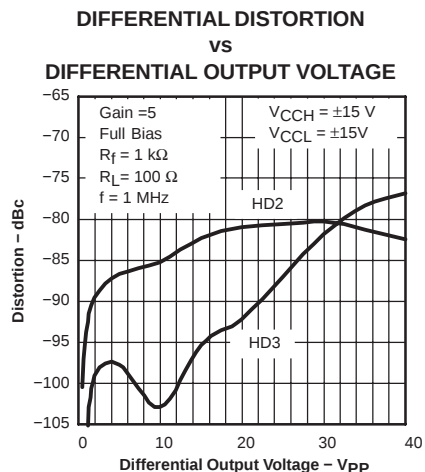


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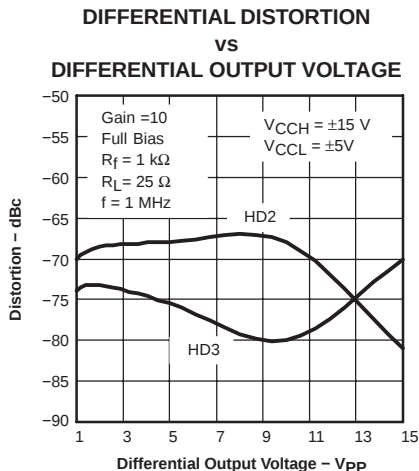


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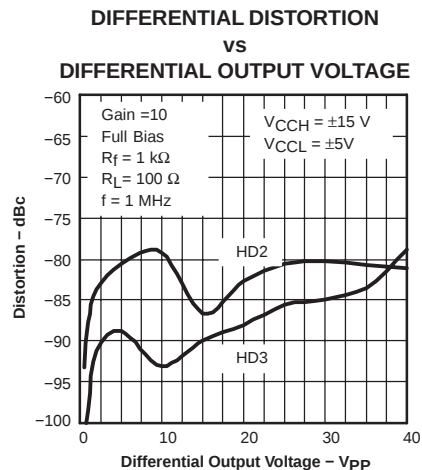


Figure 61

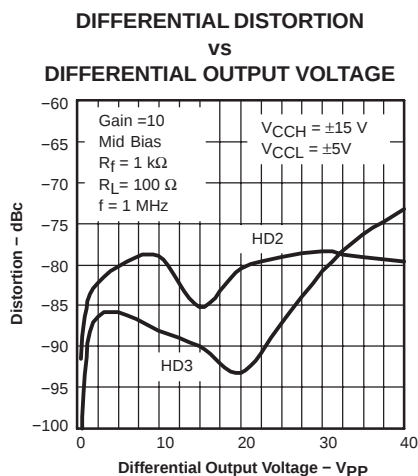


Figure 62

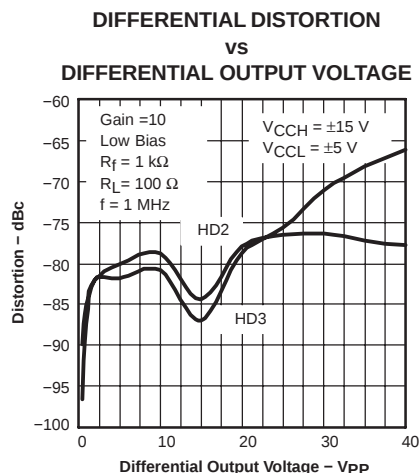


Figure 63

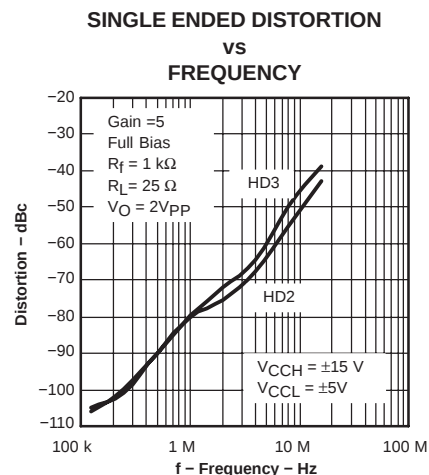


Figure 64

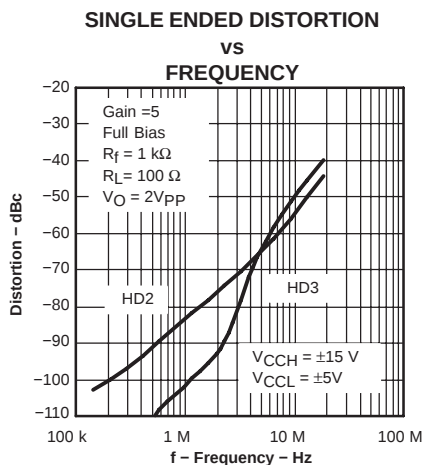


Figure 65

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6132VFP	Active	Production	HLQFP (VFP) 32	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6132
THS6132VFP.A	Active	Production	HLQFP (VFP) 32	250 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6132

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

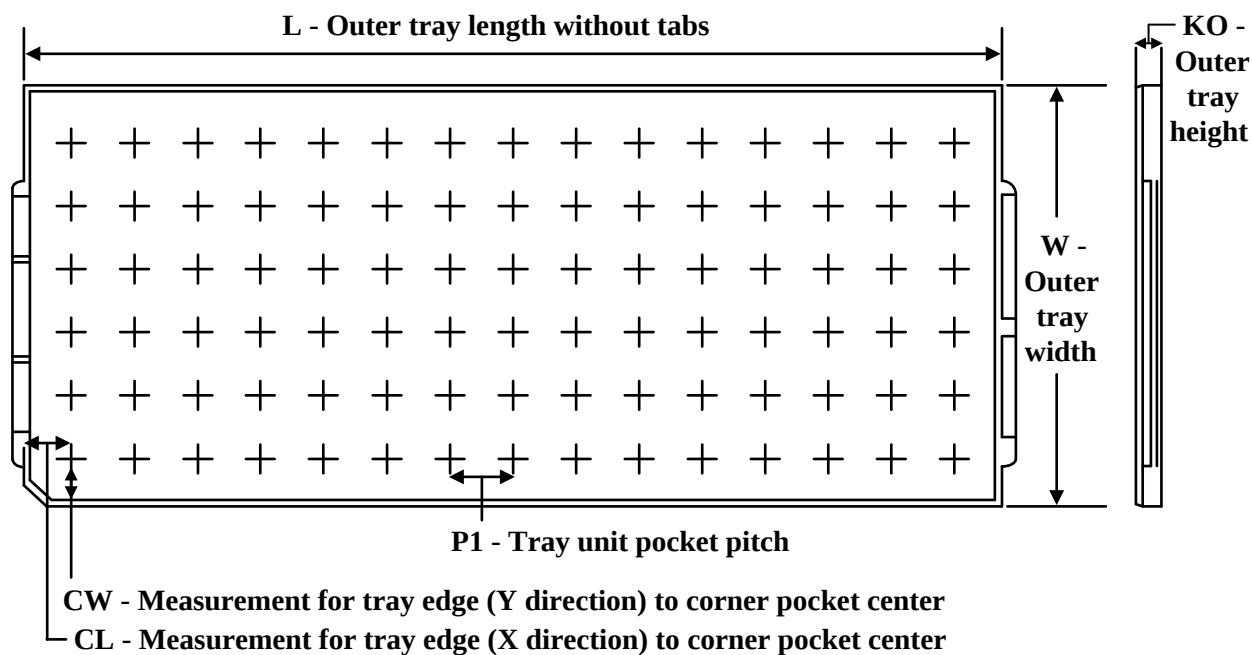
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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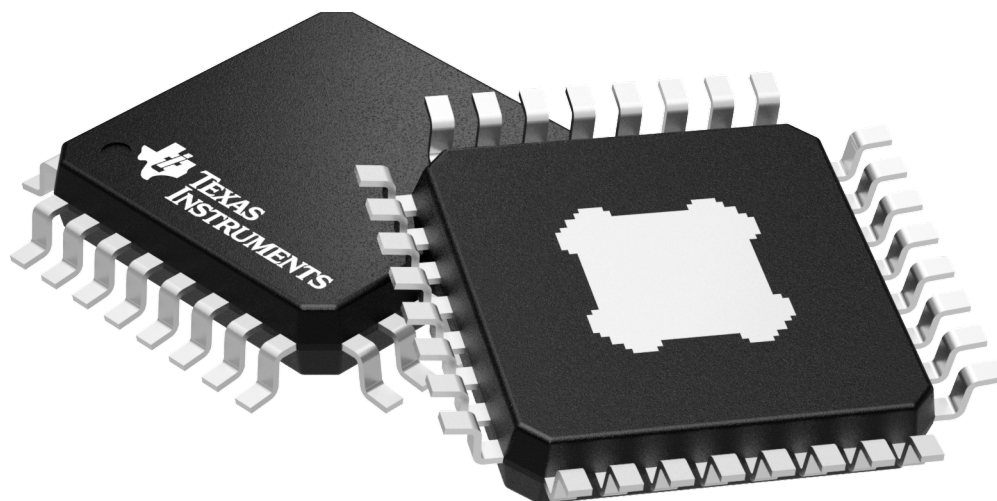
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
THS6132VFP	VFP	HLQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
THS6132VFP.A	VFP	HLQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

VFP (S-PQFP-G32)

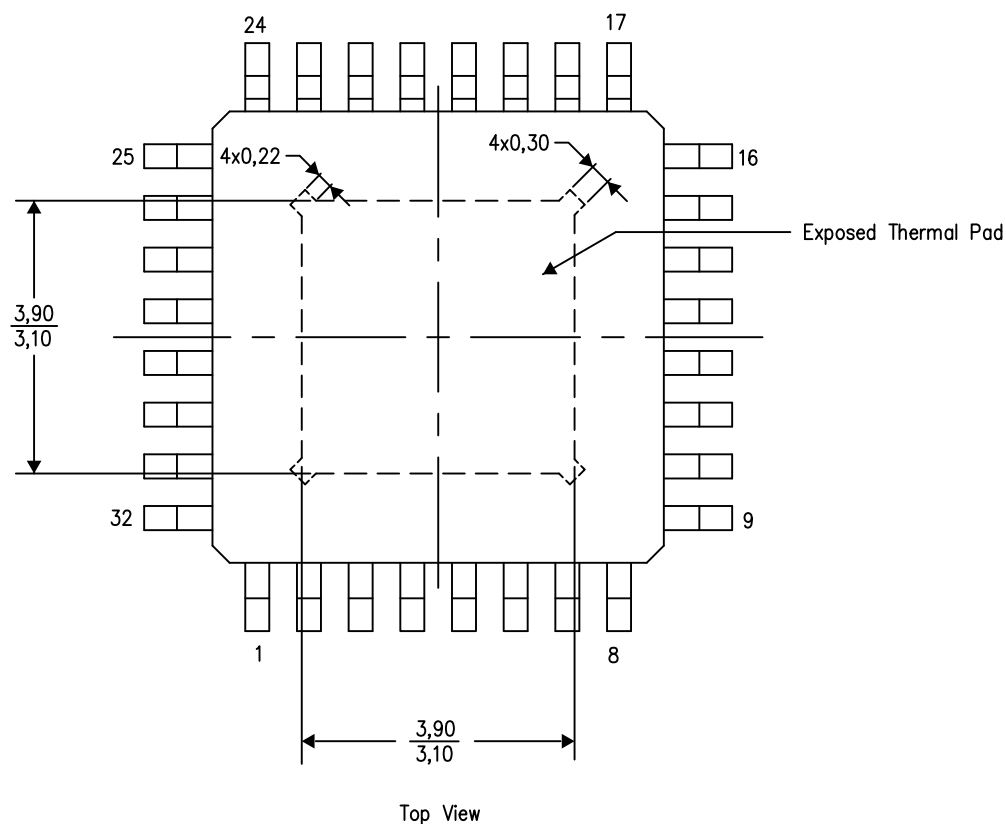
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

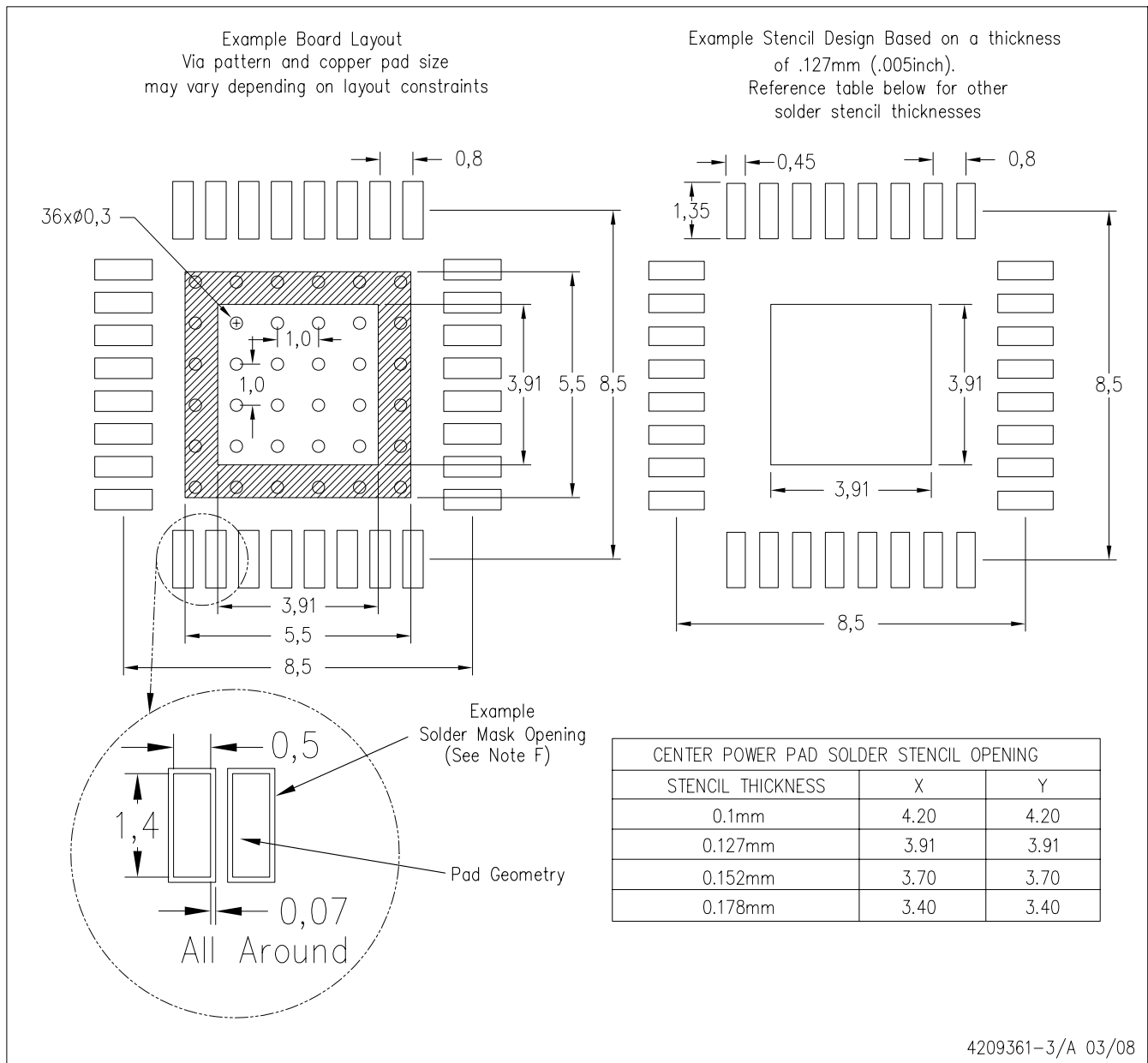


Exposed Thermal Pad Dimensions

4206318-2/E 06/13

NOTE: All linear dimensions are in millimeters

VFP (S-PQFP-G32) PowerPAD™



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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