TPS22950x 5.5-V, 3.2-A, 34-mΩ Adjustable Current Limited Load Switch

1 Features

- Input operating voltage range (V_{IN}): 1.8 V–5.5 V
- Output current limit (I_{LIMIT}): 0.05 A–3.5 A (typ.)
- TPS22950: Auto-retry current limit response
- TPS22950L: Latch off current limit response
- Thermal shutdown (TSD)
- ON-resistance (R_{ON}):
  - R_{ON} at V_{IN} = 5 V: 34 mΩ (typ.)
  - R_{ON} at V_{IN} = 3.3 V: 41 mΩ (typ.)
- Slow turn-ON timing limits inrush current (typ.):
  - t_{ON} at V_{IN} = 5 V: 800 µs
  - t_{ON} at V_{IN} = 3.3 V: 550 µs
- Always-ON reverse current blocking (TPS22950)
- Fault indication (FLT)
- Quick output discharge (QOD): 150 Ω
- Smart ON pin pulldown ($R_{PD,ON}$):
  - ON ≥ V_{IH} (I_{ON}): 50 nA (max.)
  - ON ≤ V_{IL} ($R_{PD,ON}$): 500 kΩ (typ.)
- Low power consumption:
  - ON state (I_Q): 40 µA (typ.)
  - OFF state (I_{SD}): 0.2 µA (typ.)
- UL 2367 Recognition – File No. E169910
  - Certified from I_{LIM} = 66 mA to 2.46 A

2 Application

- Personal electronics
- Tablets
- Notebooks
- Game consoles
- Accessories

3 Description

The TPS22950x is a small, single channel load switch with robust protection against fault cases with adjustable output current limiting, reverse current blocking, and thermal shutdown.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a smart pulldown is used to keep the ON pin from floating until system sequencing is complete. After the pin is deliberately driven high (>V_{IH}), the smart pulldown is disconnected to prevent unnecessary power loss.

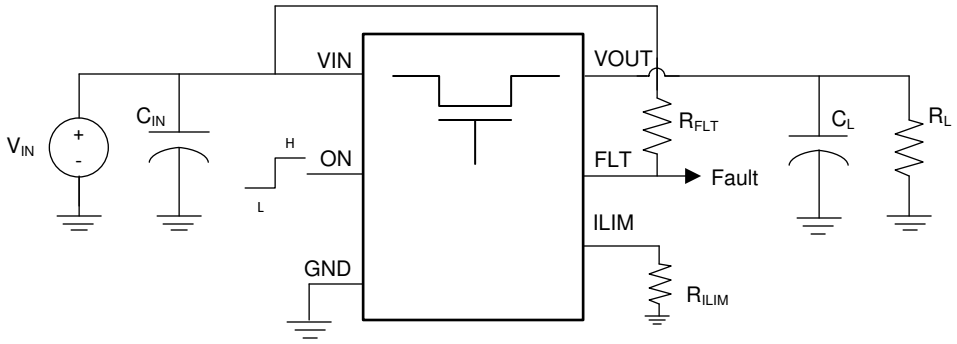
The TPS22950/C responds to overcurrent events with auto-retry behavior, while the TPS22950L uses a debounce time and latch off behavior.

TPS22950x is available in a standard WCSP package and leaded SOT package characterized for operation over an ambient temperature range of –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS22950, TPS22950L	WCSP (6)	1.106 mm × 0.706 mm
TPS22950C	DDC (SOT, 6)	2.90 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (February 2023)	Page
• Added the TPS22950C orderable to the data sheet	1

Changes from Revision * (December 2020) to Revision A (June 2022)	Page
• Added the TPS22950L orderable to the data sheet	1
• Updated ESD ratings table to the latest sandard	5
• Added line items in Electrical Characteristics to reflect TPS22950L parameters	5
• Updated the Overview section in Detailed Description to include device functionality	11
• Added a Current Limiting section to describe the latch off functionality of TPS22950L	13

5 Device Comparison Table

DEVICE NAME	ILIM Range	IMAX	ILIM Response	Debounce Time	RCB
TPS22950	0.05 A to 3.5 A	2.7A	Auto-Retry	No	Yes
TPS22950L	0.5 A to 3.5 A	2.7A	Latch Off	Yes	No
TPS22950C	0.5 A to 3.5 A	3.2A	Auto-Retry	No	Yes

6 Pin Configuration and Functions

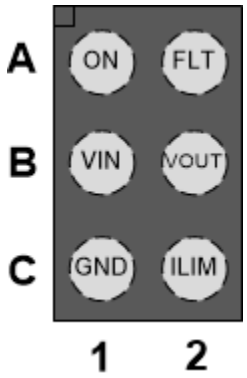


Figure 6-1. TPS22950x WCSP - 6 Top View

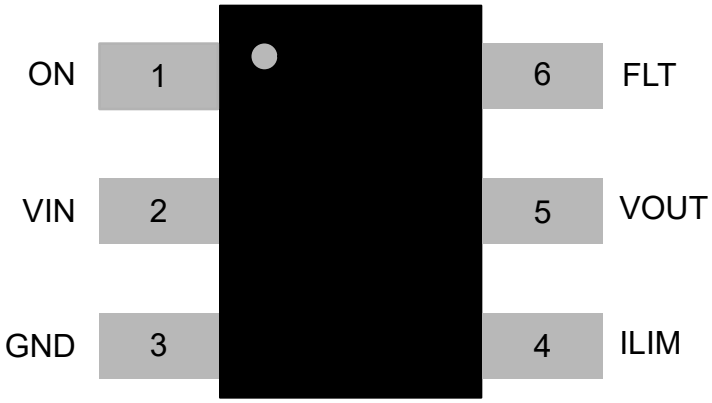


Figure 6-2. TPS22950x SOT- 6 Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	WCSP	SOT6		
ON	A1	1	I	Active high switch control input. Do not leave floating.
FLT	A2	6	O	Open-drain output, pulled low during thermal shutdown or reverse current-conditions.
VIN	B1	2	I	Switch input
VOUT	B2	5	O	Switch output
GND	C1	3	—	Device ground
ILIM	C2	4	O	Adjusts device current limit through a resistor to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{FLT}	Maximum FLT Pin Voltage	–0.3	6	V
I_{MAX}	Maximum Continuous Output Current(TPS22950C)		3.2	A
I_{MAX}	Maximum Continuous Output Current(TPS22950,TPS22950L)		2.7	A
$I_{MAX,PLS}$	Maximum Pulsed Output Current (T_J = 85°C, duty cycle = 2%)		4.1	A
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.8		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V
I_{LIM}	Output Current Limit (TPS22950)	0.05		3.5	A
I_{LIM}	Output Current Limit (TPS22950L)	0.5		3.5	A
T_A	Ambient temperature	–40		125	°C
TJ	Junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS22950		UNIT
		DDC(SOT)	YBH (WCSP)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.8	135.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.6	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.3	39.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	0.9	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS22950		UNIT
		DDC(SOT)	YBH (WCSP)	
		6 PINS	6 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	36.0	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Unless otherwise noted, the characteristics in the following table apply across the recommended operating input voltage range with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 5 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply (VIN)							
$I_{Q, VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, VOUT = Open	–40°C to 85°C		44	60	µA
			–40°C to 125°C			60	µA
$I_{SD, VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, VOUT = GND	25°C		0.2	0.4	µA
			–40°C to 85°C			9	µA
			–40°C to 125°C			46	µA
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	V_{IN} = 5 V, I_{OUT} = –200 mA	25°C		34	41	mΩ
			–40°C to 85°C			49	mΩ
			–40°C to 125°C			54	mΩ
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		41	51	mΩ
			–40°C to 85°C			62	mΩ
			–40°C to 125°C			68	mΩ
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		67	90	mΩ
			–40°C to 85°C			105	mΩ
			–40°C to 125°C			116	mΩ
Output Current Limit (ILIM)							
I_{LIM}	Output Current Limit	R_{ILIM} = 610 Ω V_{IN}- V_{OUT} = 0.5 V	–40°C to 125°C	1.54	2	2.46	A
		R_{ILIM} = 1.15 kΩ V_{IN}- V_{OUT} = 0.5 V	–40°C to 125°C	0.75	1	1.25	A
		R_{ILIM} = 2.21 kΩ V_{IN}- V_{OUT} = 0.5 V	–40°C to 125°C	0.38	0.5	0.62	A
		R_{ILIM} = 19.2 kΩ V_{IN}- V_{OUT} = 0.5 V	–40°C to 125°C	0.034	0.05	0.066	A
$I_{LIM,PEAK}$	Output Current Limit Peak (TPS22950L)	R_{ILIM} = 624 Ω V_{IN}- V_{OUT} = 1 V	–40°C to 125°C		2.1		A
		R_{ILIM} = 1.24 kΩ V_{IN}- V_{OUT} = 1 V	–40°C to 125°C		1		A
		R_{ILIM} = 2.49 kΩ V_{IN}- V_{OUT} = 1 V	–40°C to 125°C		0.52		A
t_{LIM}	Current Limit Response Time	Output hard short (I_{OUT} > I_{LIM})	–40°C to 125°C		5		µs
$t_{DEBOUNCE}$	Latch Off Debounce Time (TPS22950L)	V_{IN}- V_{OUT} = 0.5 V	–40°C to 125°C		120	188	µs
I_{HCD}	High current detection threshold (TPS22950L)	R_{ILIM} = 624 Ω	–40°C to 125°C	1.2	1.6	1.9	A
		R_{ILIM} = 1.25 kΩ	–40°C to 125°C	0.6	0.85	1.1	A
		R_{ILIM} = 2.5 kΩ	–40°C to 125°C	0.3	0.47	0.65	A

7.5 Electrical Characteristics (continued)

Unless otherwise noted, the characteristics in the following table apply across the recommended operating input voltage range with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 5 V and T_A = 25°C.

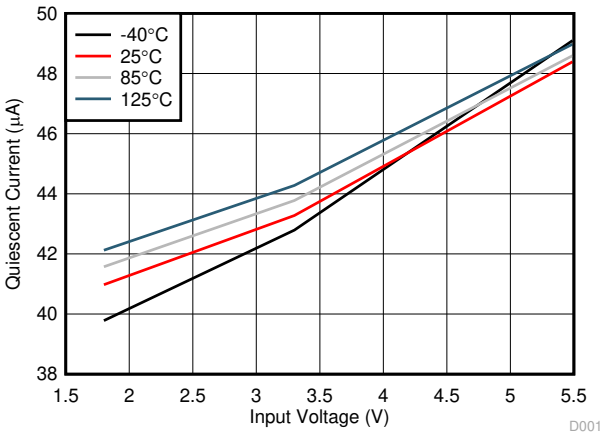
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reverse Current Blocking (TPS22950)							
V_{RCB}	Activation Threshold	V_{OUT} Rising; V_{OUT} > V_{IN}	–40°C to 125°C		44		mV
	Release Threshold	V_{OUT} Falling; V_{OUT} > V_{IN}	–40°C to 125°C		16		mV
t_{RCB}	Response Time	V_{OUT} = V_{IN} + 1 V	–40°C to 125°C		3		µs
$I_{OUT,RCB}$	Reverse Leakage Current into VOUT	V_{ON} ≤ V_{IL} V_{IN} = 0 V, V_{OUT} = 5 V	–40°C to 125°C			38	µA
Fault Indication (FLT)							
$V_{OL, FLT}$	Output Low Voltage	I_{FLT} = 1 mA	–40°C to 125°C			0.1	V
$t_{D,FLT}$	Fault Delay Time	V_{ON} ≥ V_{IH}	–40°C to 125°C		10		µs
I_{FLT}	Off State Leakage	V_{ON} ≤ V_{IL}	–40°C to 125°C			50	nA
Enable Pin (ON)							
$R_{PD, ON}$	Smart Pull Down Resistance	V_{ON} ≤ V_{IL}	–40°C to 125°C		500	650	kΩ
I_{ON}	ON Pin Leakage	V_{ON} ≥ V_{IH}	–40°C to 125°C			50	nA
R_{QOD}	Quick Output Discharge Resistance	V_{IN} = 5 V V_{ON} ≤ V_{IL}	–40°C to 125°C		100	160	Ω
		V_{IN} = 3.3 V V_{ON} ≤ V_{IL}	–40°C to 125°C		150	185	Ω
		V_{IN} = 1.8 V V_{ON} ≤ V_{IL}	–40°C to 125°C		200	355	Ω
Thermal Shutdown (TSD)							
TSD	Thermal Shutdown	Rising	N/A		170		°C
		Falling (Hysteresis)	N/A		150		°C

7.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 25°C with a load of C_L = 1 µF, R_L = 100 Ω

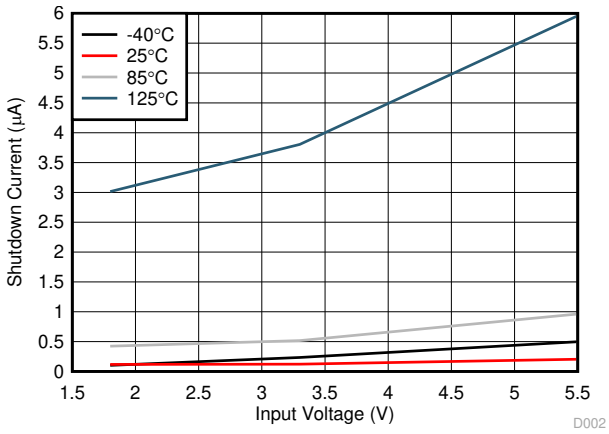
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5 V		800		µs
		V_{IN} = 3.3 V		550		µs
		V_{IN} = 1.8 V		400		µs
t_R	Output Rise Time	V_{IN} = 5 V		600		µs
		V_{IN} = 3.3 V		320		µs
		V_{IN} = 1.8 V		200		µs
t_D	Output Delay Time	V_{IN} = 5 V		260		µs
		V_{IN} = 3.3 V		250		µs
		V_{IN} = 1.8 V		260		µs
t_{OFF}	Turn OFF Time	V_{IN} = 5 V		20		µs
		V_{IN} = 3.3 V		15		µs
		V_{IN} = 1.8 V		17		µs
t_{FALL}	Output Fall Time	V_{IN} = 5 V		118		µs
		V_{IN} = 3.3 V		120		µs
		V_{IN} = 1.8 V		130		µs

7.7 Typical Characteristics



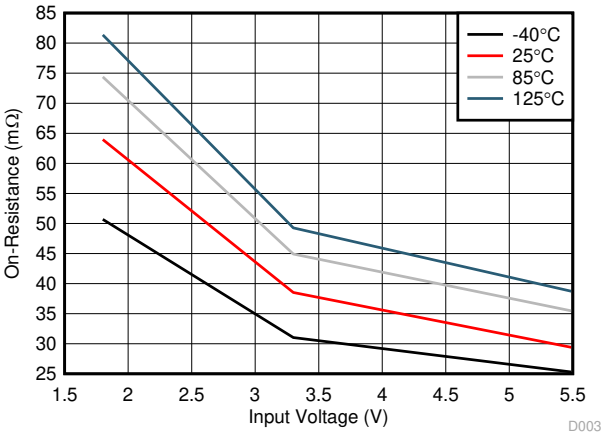
$V_{ON} \geq V_{IH}$

Figure 7-1. Quiescent Current vs Input Voltage



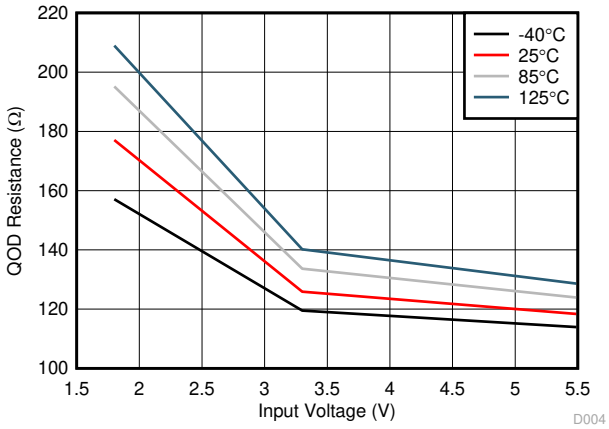
$V_{ON} \leq V_{IL}$

Figure 7-2. Shutdown Current vs Input Voltage



$V_{ON} \geq V_{IH}$ I_{OUT} = –200 mA

Figure 7-3. On-Resistance vs Input Voltage



$V_{ON} \leq V_{IL}$

Figure 7-4. QOD Resistance vs Input Voltage

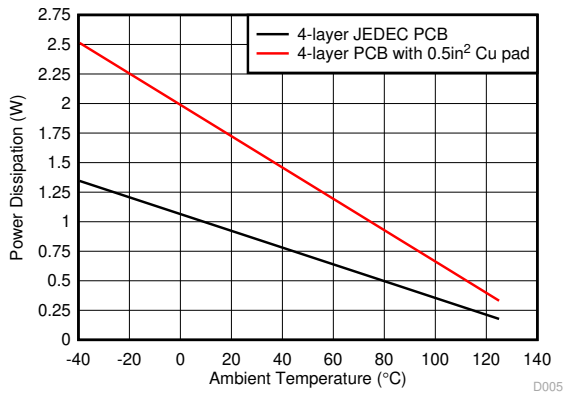


Figure 7-5. Maximum Power Dissipation vs Ambient Temperature

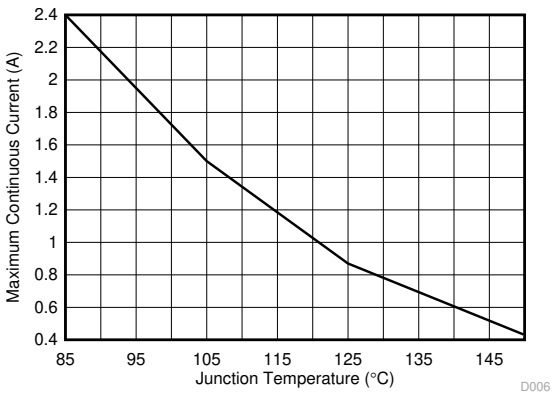
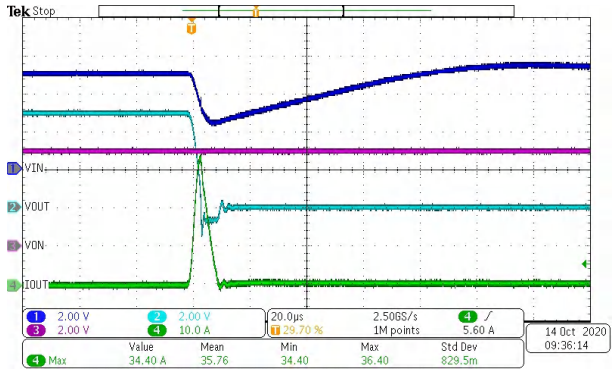


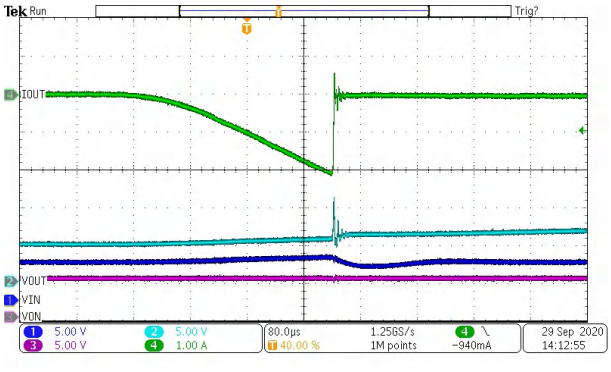
Figure 7-6. Maximum Continuous Current vs Junction Temperature

7.7 Typical Characteristics (continued)



V_{IN} = 5 V V_{ON} = 5 V

Figure 7-7. Short-Circuit Response



V_{IN} = 5 V V_{ON} = 5 V

Figure 7-8. Reverse Current Blocking

8 Parameter Measurement Information

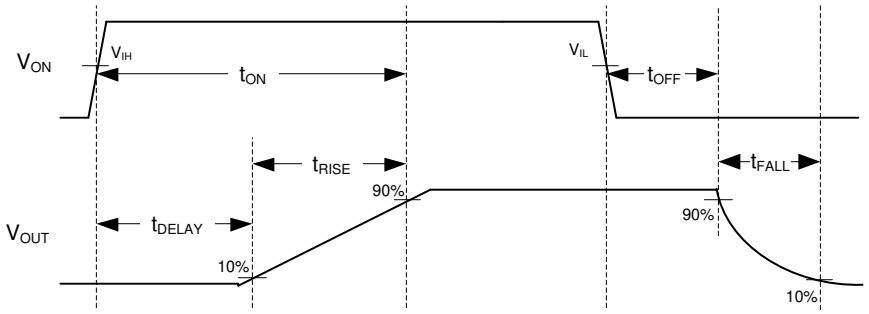


Figure 8-1. Timing Waveform

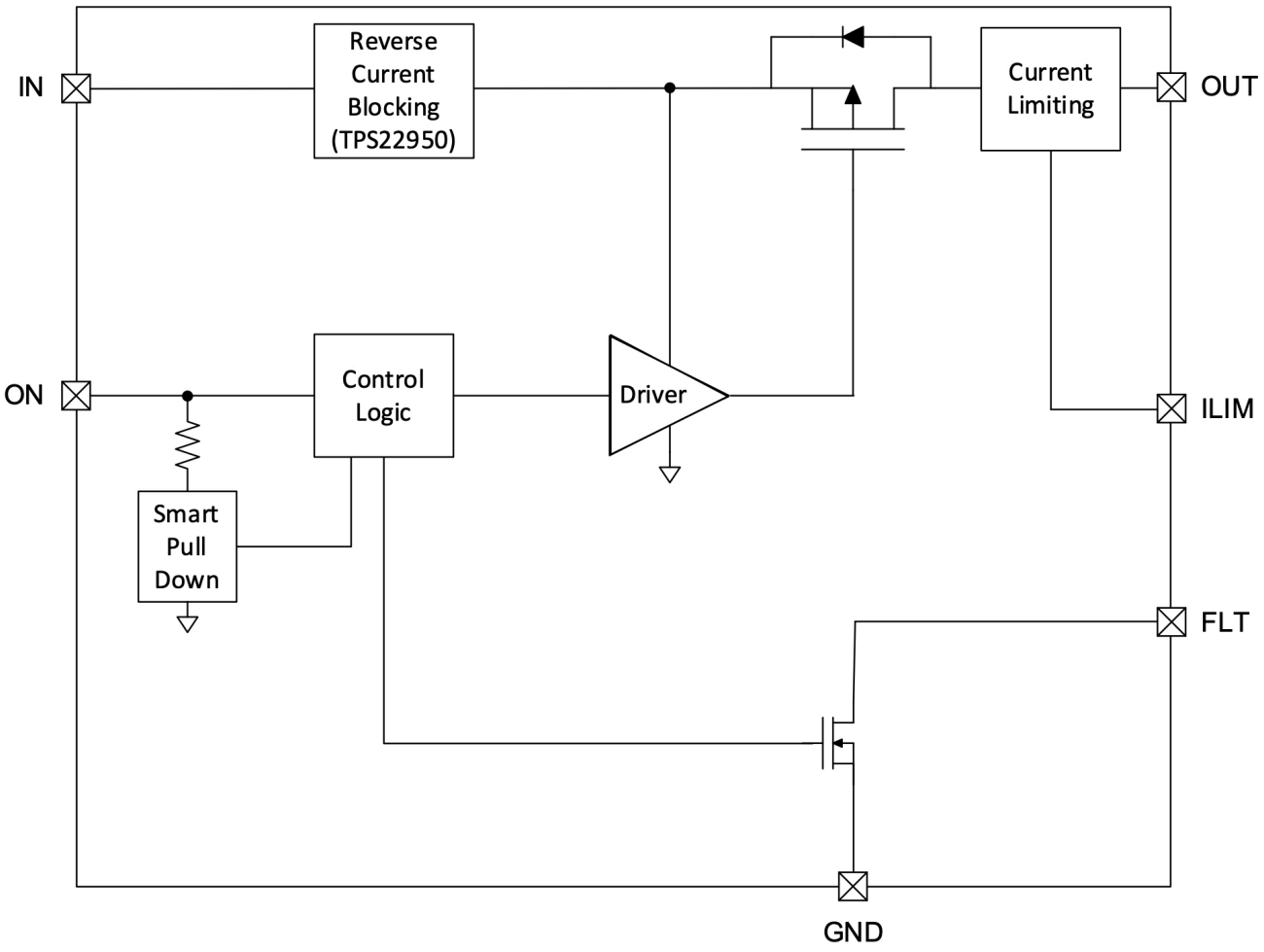
9 Detailed Description

9.1 Overview

The TPS22950x is a single channel load switch with a 34-mΩ power MOSFET capable of driving loads up to 3.2 A. While on, the device provides protection against fault cases though its adjustable output current limiting and thermal shutdown. The TPS22950 responds to overcurrent events with auto-retry behavior, while the TPS22950L uses a debounce time and latch off behavior. The TPS22950 also provides reverse current blocking for when VOUT exceeds VIN.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals, and a smart pulldown is used to keep the ON pin from floating until system sequencing is complete. When the device is turned off, quick output discharge is enabled, pulling the output voltage down to 0 V through a resistive path to GND.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Current Limiting (TPS22950, TPS22950C)

The TPS22950 responds to overcurrent conditions by limiting its output current to the I_{LIM} level shown in the figure below.

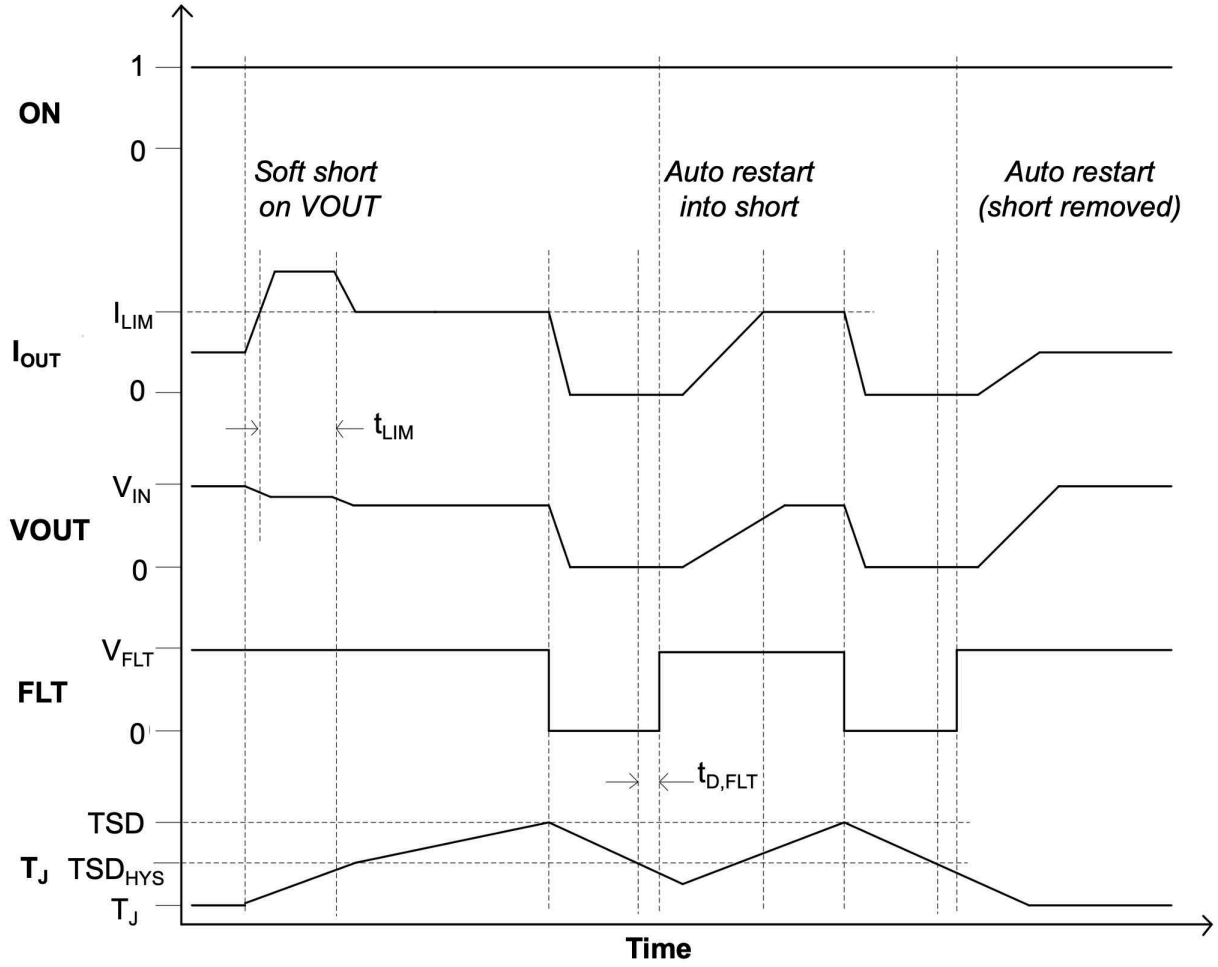


Figure 9-1. Output Current Limit for Short-Circuit Protection (t_{LIM})

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22950 ramps the output current to I_{LIM}. The TPS22950 device limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and the device turns itself off. The device remains off until the junction temperature has lowered to TSD_{HYS}, and the device turns itself back on. This action cycles until the overload condition is removed.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see figure below), and before this time the current is able to exceed I_{LIM}. In the case of a fast transient, the current-sense amplifier is over-driven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM}. Similar to the previous case, the TPS22950 limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

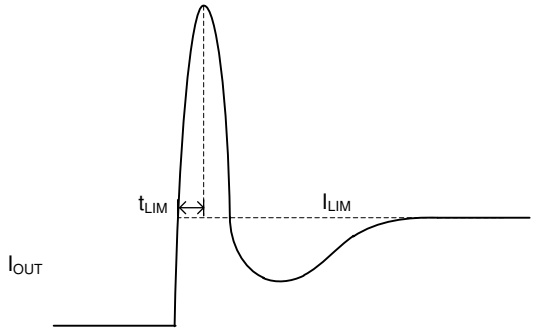


Figure 9-2. Transient Current Limit Waveform

9.3.2 Current Limiting (TPS22950L)

The TPS22950L responds to overcurrent conditions by limiting its output current to the current limit (I_{LIM}) level after initially peaking its current at $I_{LIM,PEAK}$. The behavior of the device is shown in Figure 9-3.

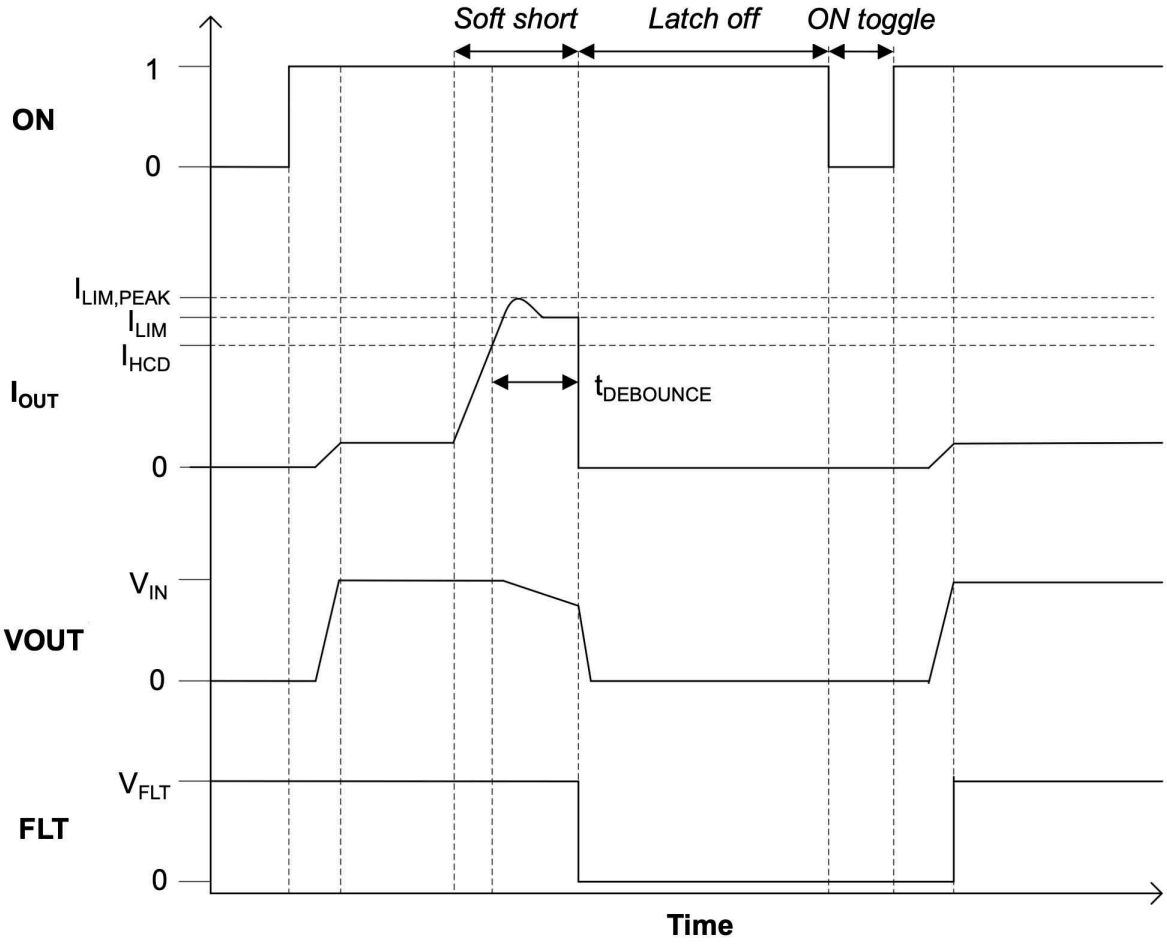


Figure 9-3. Output Current Limit Behavior

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22950L ramps the output current to I_{LIM}. The TPS22950L device limits the current to I_{LIM} until the overload

condition is removed. If the internal junction temperature of the device reaches thermal shutdown ,the device turns itself off. The device remains off until the junction temperature has lowered to TSD_{HYS}, and the device turns itself back on. If thermal shutdown is not reached, the device waits for the load current to exceed the high current detection level (I_{HCD}) for the $t_{DEBOUNCE}$ time and latch itself off. The FLT pin is pulled low, and the device is only able to turn on again by toggling the VIN or ON pins.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see Figure 9-4), and before this time the current is able to exceed I_{LIM}. In the case of a fast transient, the current-sense amplifier is over-driven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM}. Similar to the previous case, the TPS22950L limits the current to I_{LIM} until the overload condition is removed, the debounce time of 120 µs is reached, or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

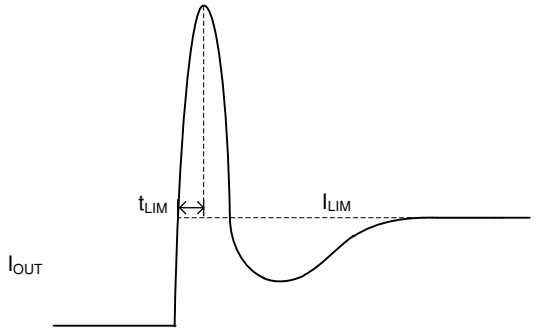


Figure 9-4. Transient Current Limit Waveform

9.3.3 Adjusting the Current Limit

The current limit is adjusted by connecting an external resistor from the ILIM pin to GND. The current limit resistor can be chosen using the equation:

$$I_{LIM} = 1.18 \times (R_{ILIM})^{-1.072} \quad (1)$$

The units for the equation are amps for I_{LIM} and kilohms for R_{ILIM}. For the TPS22950L, the device is only limiting current during a short period of time. Therefore, the peak value of the current ($I_{LIM,PEAK}$) may be more applicable for system considerations. The equation for this parameter is below:

$$I_{LIM,PEAK} = 1.31 \times (R_{ILIM})^{-1.042} \quad (2)$$

The R_{ILIM} resistor is also used to set the high current detection threshold for the TPS22950L, and that equation is shown below.

$$I_{HCD} = (0.988 / R_{ILIM}) + 0.06 \quad (3)$$

The units for the equation are amps for I_{HCD} and kilohms for R_{ILIM}.

9.3.4 Reverse Current Blocking (TPS22950, TPS22950C)

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN}, there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold is exceeded (about 900 mA), there is a delay time (t_{RCB}) before the switch turns off to stop the current flow. The switch remains off and block reverse current as long as the reverse voltage condition exists. After V_{OUT} has dropped below the release voltage threshold (V_{RCB}) the device turns back on. When the ON pin is pulled low, the device constantly blocks reverse current.

9.4 Device Functional Modes

The tables below summarize the Device Functional Modes.

Table 9-1. Output Connection Table

ON	Fault Condition	VOUT State	FLT State
L	N/A	Hi-Z	Hi-Z
H	None	VIN (via R_{ON})	Hi-Z
H	Output short	Current Limited	Hi-Z
H	Thermal shutdown	Hi-Z	L
H	Reverse current	Hi-Z	L

Table 9-2. Smart-ON Functional Modes ($R_{PD,ON}$)

ON	ON Pin
≤ V_{IL}	Pulldown active
≥ V_{IH}	No pulldown

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

10.2 Typical Application

This typical application demonstrates how the TPS22950x device can be used to set an adjustable current limit.

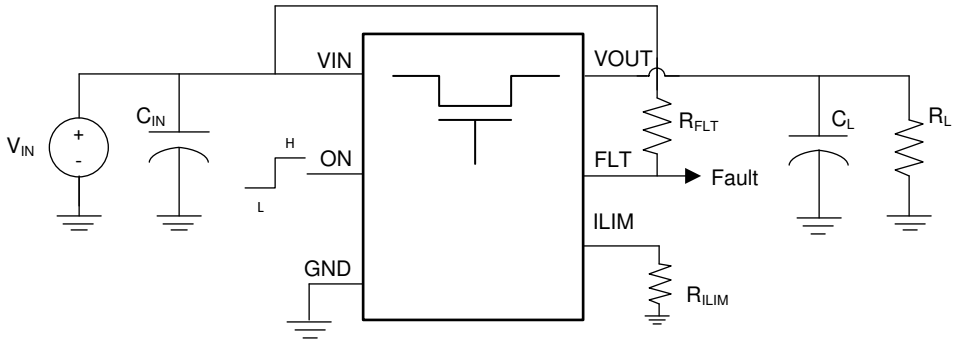


Figure 10-1. Typical Application

10.2.1 Design Requirements

For this example, the values below are used as the design parameters.

Table 10-1. Design Parameters

PARAMETER	VALUE
Input Voltage (V_{IN})	5 V
Load Current (mA)	100 mA
Typical Current Limit (mA)	500 mA

10.2.2 Detailed Design Procedure

In this example the nominal load current is 100 mA, so the current limit can be set to 500 mA without disrupting normal operation. Use Equation 4 to calculate the resistor needed on the ILIM pin.

$$I_{LIM} = 1.18 \times (R_{ILIM})^{-1.072} \quad (4)$$

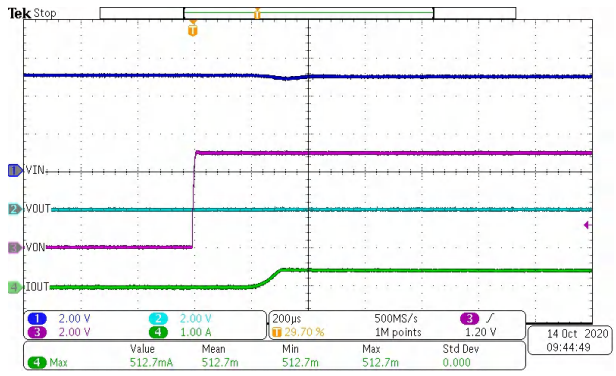
where

- I_{LIM} = Typical current limit setting
- R_{ILIM} = Resistor on the ILIM pin

Based on Equation 4, a 2.21-kΩ resistor must be used on the ILIM pin to set a typical current limit of 500 mA.

10.2.3 Application Curves

The below scope shot shows the device turning on into a fault condition and limiting the current to the specified amount of 500 mA.



R_{ILIM} = 2.5 kΩ V_{OUT} = GND

Figure 10-2. TPS22950 Turning On into an Output Short

10.3 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.8 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

10.4 Layout

10.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

10.4.2 Layout Example

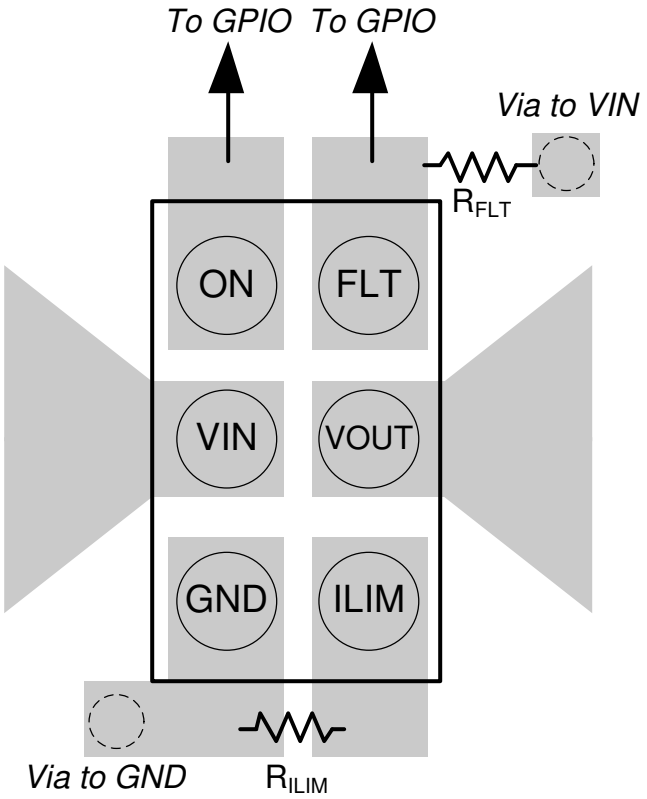


Figure 10-3. TPS22950x WCSP Layout Example

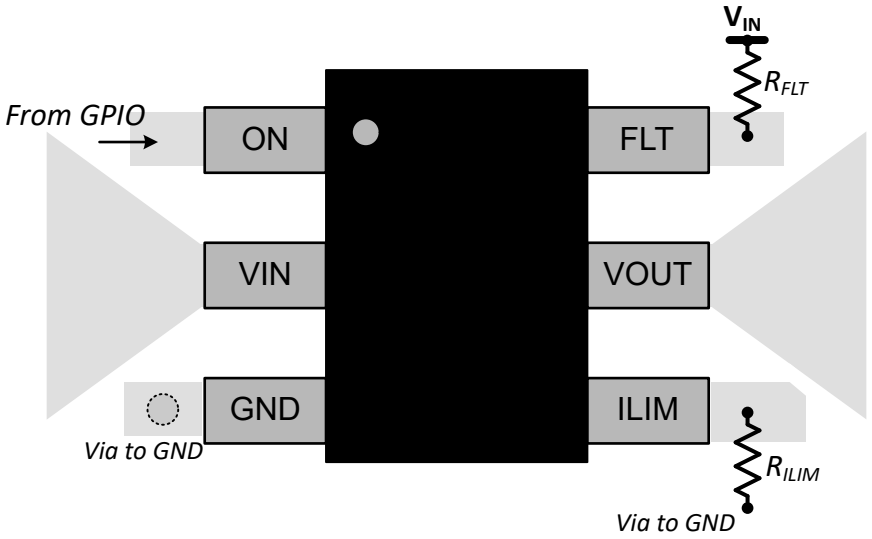


Figure 10-4. TPS22950C SOT6 Layout Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

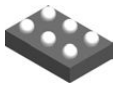
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

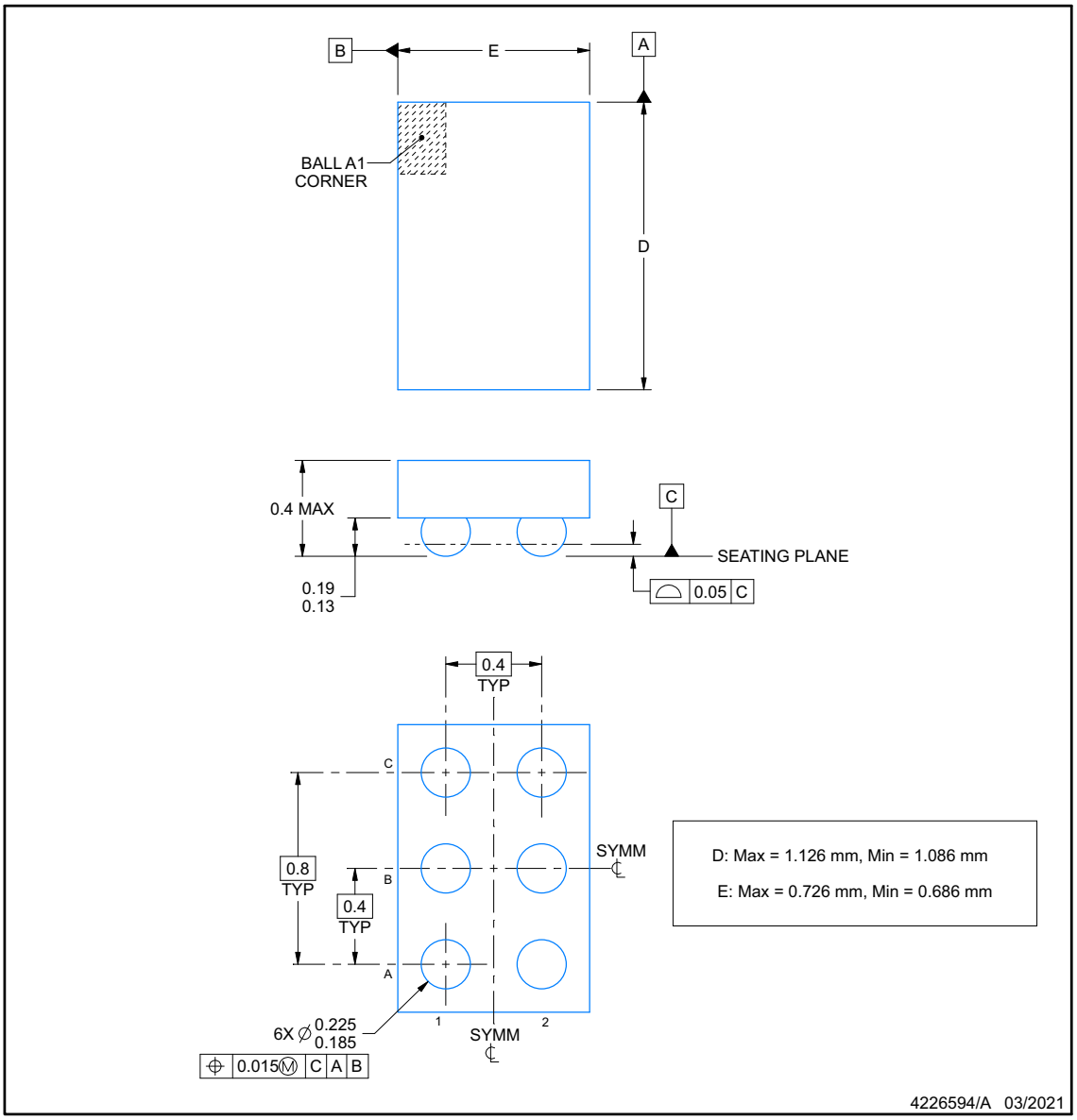
PACKAGE OUTLINE

YBH0006-C02



DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

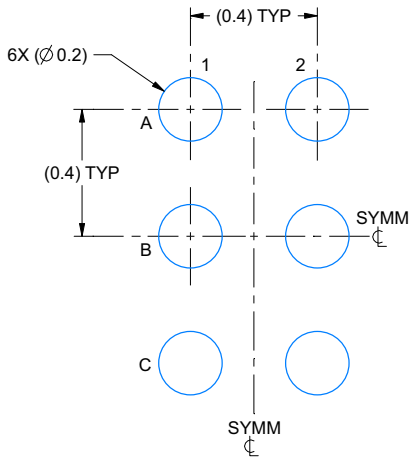
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

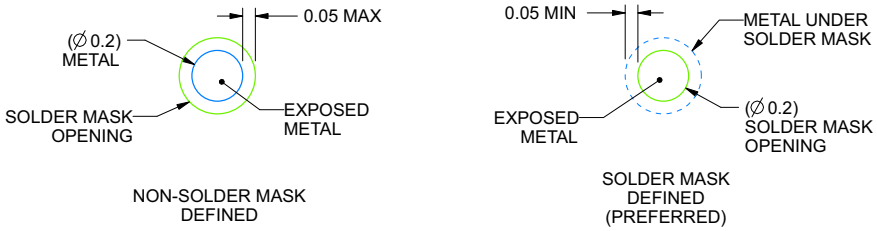
YBH0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226594/A 03/2021

NOTES: (continued)

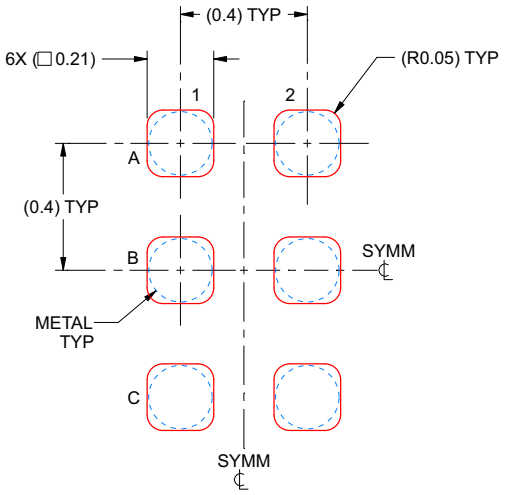
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226594/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22950CDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	950C
TPS22950CDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	950C
TPS22950LYBHR	Active	Production	DSBGA (YBH) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	4
TPS22950LYBHR.A	Active	Production	DSBGA (YBH) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	4
TPS22950YBHR	Active	Production	DSBGA (YBH) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	
TPS22950YBHR.A	Active	Production	DSBGA (YBH) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22950 :

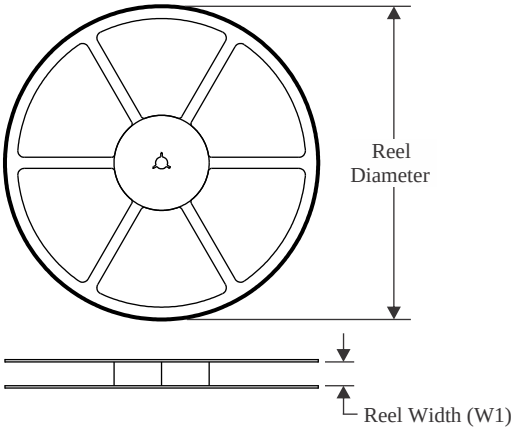
- Automotive : TPS22950-Q1

NOTE: Qualified Version Definitions:

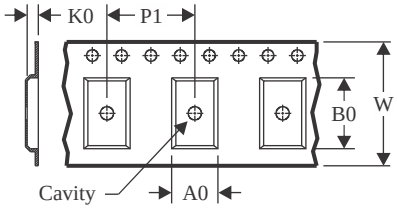
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

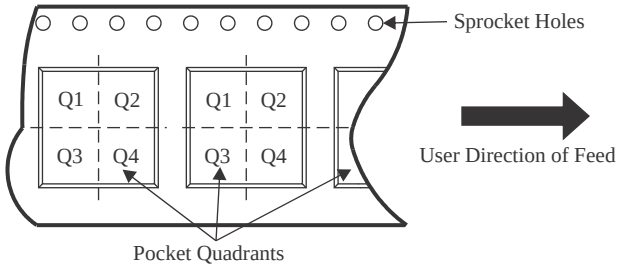


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

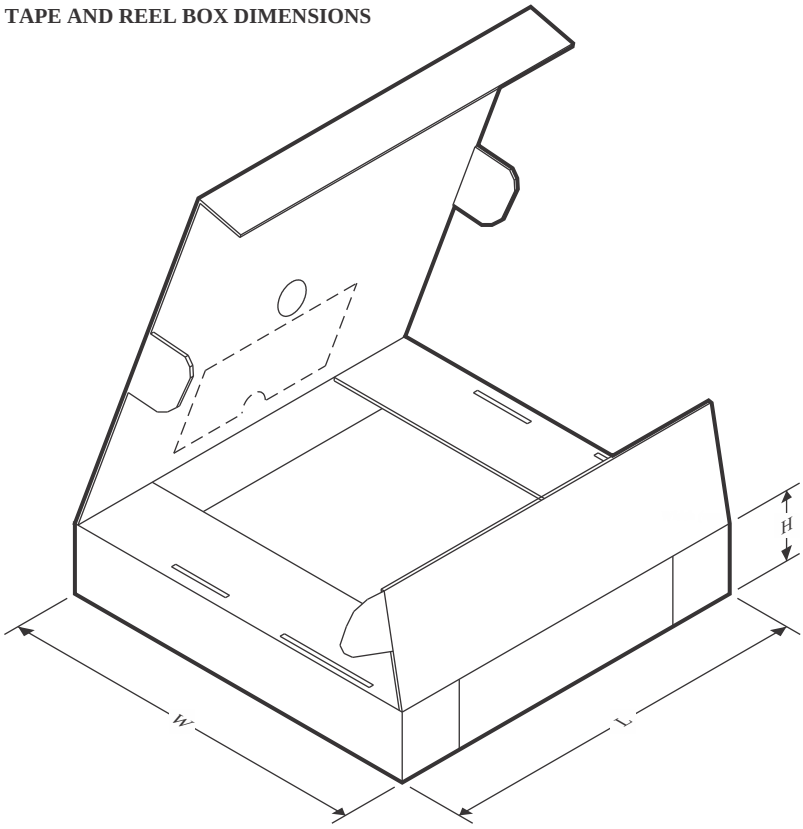
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22950CDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22950LYBHR	DSBGA	YBH	6	3000	180.0	8.4	0.8	1.21	0.43	2.0	8.0	Q1
TPS22950YBHR	DSBGA	YBH	6	3000	180.0	8.4	0.8	1.21	0.43	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

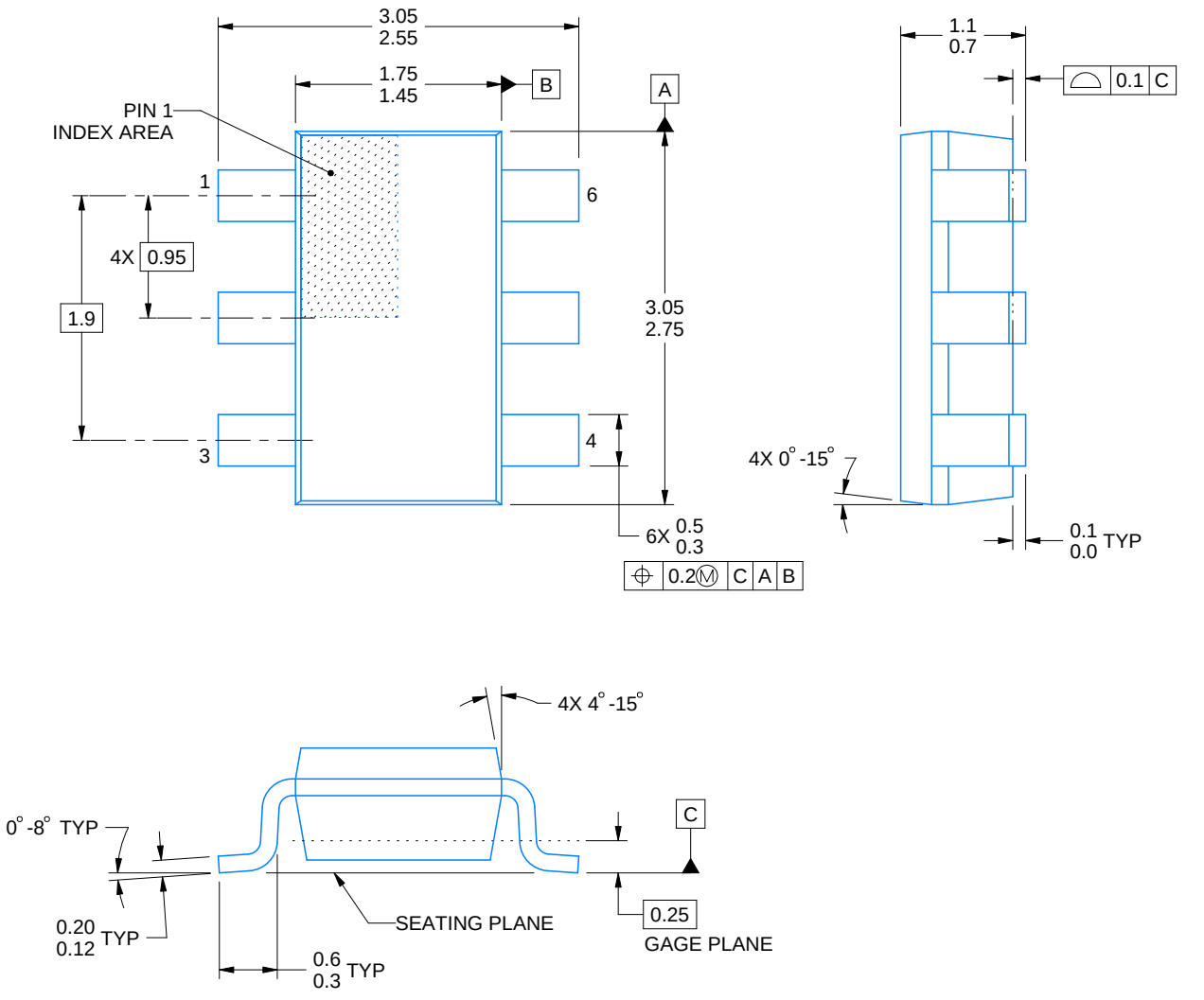
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22950CDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS22950LYBHR	DSBGA	YBH	6	3000	182.0	182.0	20.0
TPS22950YBHR	DSBGA	YBH	6	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

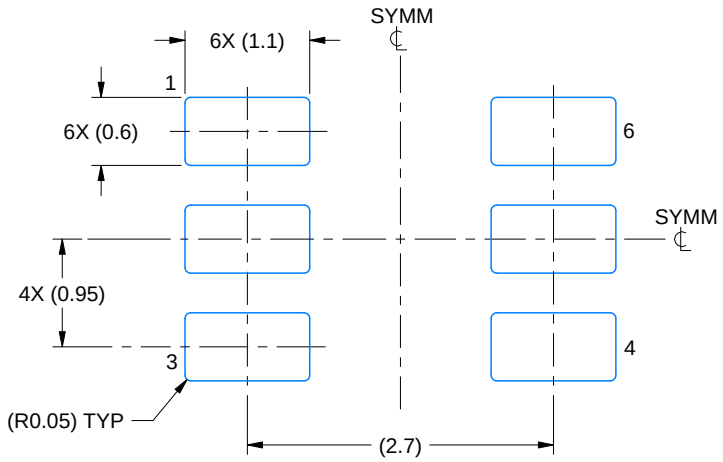
SMALL OUTLINE TRANSISTOR



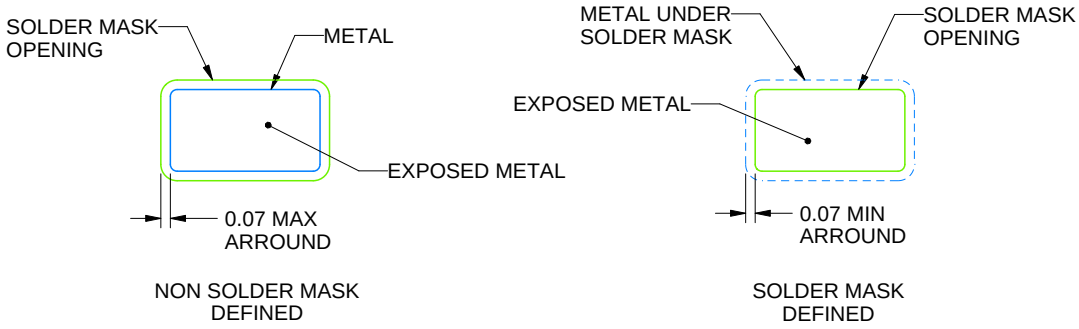
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

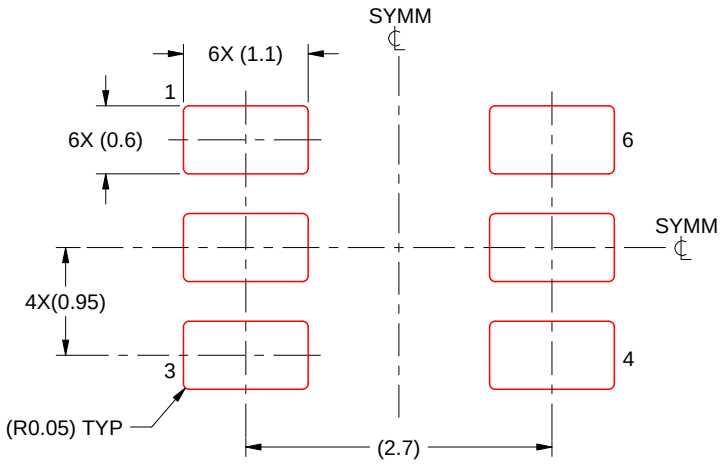


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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