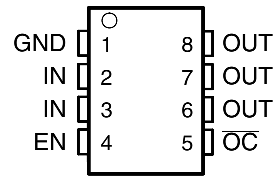
SGLS298B − SEPTEMBER 2005 − REVISED JUNE 2008

- **Qualified for Automotive Applications**
- **33-mΩ (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit and Thermal Protection**
- **Overcurrent Logic Output**
- **Operating Range . . . 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **Typical Rise Time . . . 6.1 ms**
- **Undervoltage Lockout**
- **Maximum Standby Supply Current . . . 10 μA**
- **No Drain-Source Back-Gate Diode**
- **Available in 8-pin SOIC Package**
- **Ambient Temperature Range, −40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**
- **UL Listed − File No. E169910**

D PACKAGE
(TOP VIEW)



description

The TPS203x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS203x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS203x devices differ only in short-circuit current threshold. The TPS2030 limits at 0.3-A load, the TPS2031 at 0.9-A load, the TPS2032 at 1.5-A load, the TPS2033 at 2.2-A load, and the TPS2034 at 3-A load (see Available Options). The TPS203x is available in an 8-pin small-outline integrated-circuit (SOIC) package and in an 8-pin dual in-line (DIP) package and operates over a junction temperature range of −40°C to 125°C.

GENERAL SWITCH CATALOG

33 mΩ, single TPS201xA 0.2 A – 2 A TPS202x 0.2 A – 2 A **TPS203x 0.2 A – 2 A**	**80 mΩ, dual** TPS2042 500 mA TPS2052 500 mA TPS2046 250 mA TPS2056 250 mA	**80 mΩ, triple** TPS2043 500 mA TPS2053 500 mA TPS2047 250 mA TPS2057 250 mA	**80 mΩ, quad** TPS2044 500 mA TPS2054 500 mA TPS2048 250 mA TPS2058 250 mA
80 mΩ, single TPS2014 600 mA TPS2015 1 A TPS2041 500 mA TPS2051 500 mA TPS2045 250 mA TPS2055 250 mA	**260 mΩ** IN1 IN2 OUT **1.3 Ω** TPS2100/1 IN1 500 mA IN2 10 mA TPS2102/3/4/5 IN1 500 mA IN2 100 mA		

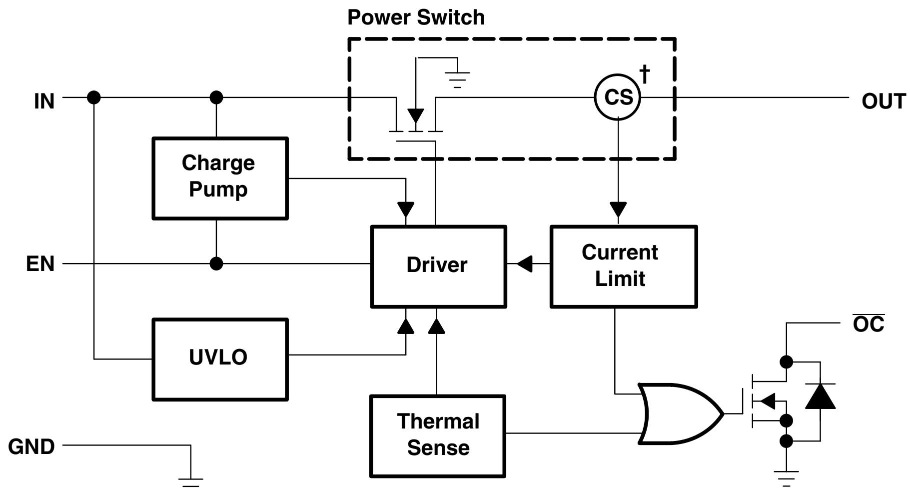
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS†

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES‡ SMALL OUTLINE (D)§
−40°C to 85°C	Active high	0.2	0.3	TPS2030IDRQ1¶
		0.6	0.9	TPS2031IDRQ1
		1	1.5	TPS2032IDRQ1¶
		1.5	2.2	TPS2033IDRQ1¶
		2	3	TPS2034IDRQ1¶

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2030IDRQ1)
¶ Product Preview

TPS2030 functional block diagram



†Current Sense

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input. Logic high turns on power switch.
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent. Logic output active low
OUT	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

enable (EN)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic low is present on EN . A logic high input on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1)	−0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1)	−0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(EN)}$	−0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$	internally limited
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Electrostatic discharge (ESD) protection: Human body model	2 kV
Machine model	200V
Charged device model (CDM)	750 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(IN)}$	2.7	5.5	V
	$V_{I(EN)}$	0	5.5	V
Continuous output current, I_O	TPS2030	0	0.2	A
	TPS2031	0	0.6	
	TPS2032	0	1	
	TPS2033	0	1.5	
	TPS2034	0	2	
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, EN = 5 V, T_J = –40°C to 125°C (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 1.8 A‡		33	36	mΩ
			T_J = 85°C,	I_O = 1.8 A‡		38	46	
			T_J = 125°C,	I_O = 1.8 A‡		44	50	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 1.8 A‡		37	41	
			T_J = 85°C,	I_O = 1.8 A‡		43	52	
			T_J = 125°C,	I_O = 1.8 A‡		51	61	
		$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 0.18 A		30	34	
			T_J = 85°C,	I_O = 0.18 A		35	50	
			T_J = 125°C,	I_O = 0.18 A		39	55	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 0.18 A		33	37	
			T_J = 85°C,	I_O = 0.18 A		39	55	
			T_J = 125°C,	I_O = 0.18 A		44	66	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF,	T_J = 25°C, R_L = 10 Ω			6.1		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 μF,	T_J = 25°C, R_L = 10 Ω			8.6		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF,	T_J = 25°C, R_L = 10 Ω			3.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 μF,	T_J = 25°C, R_L = 10 Ω			3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
‡ Not production tested

enable input (EN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.5	
I_I	Input current	EN = 0 V or EN = $V_{I(IN)}$	−0.5		0.5	μA
t_{on}	Turnon time	C_L = 100 μF, R_L = 10 Ω			20	ms
t_{off}	Turnoff time	C_L = 100 μF, R_L = 10 Ω			40	

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V, OUT connected to GND, Device enable into short circuit	TPS2030	0.22	0.3	0.4	A
			TPS2031	0.66	0.9	1.1	
			TPS2032	1.1	1.5	1.8	
			TPS2033	1.65	2.2	2.7	
			TPS2034	2.2	3	3.8	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, EN = 5 V, T_A = –40°C to 125°C (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	EN = 0	T_J = 25°C		0.3	1	μA
			−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	EN = $V_{I(IN)}$	T_J = 25°C		58	75	μA
			−40°C ≤ T_J ≤ 125°C		75	100	
Leakage current	OUT connected to ground	EN = 0	−40°C ≤ T_J ≤ 125°C		10		μA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	T_J = 25°C		100		mV

overcurrent ($\overline{OC}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output low voltage	I_O = 10 mA, $V_{OL(\overline{OC})}$			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1	μA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

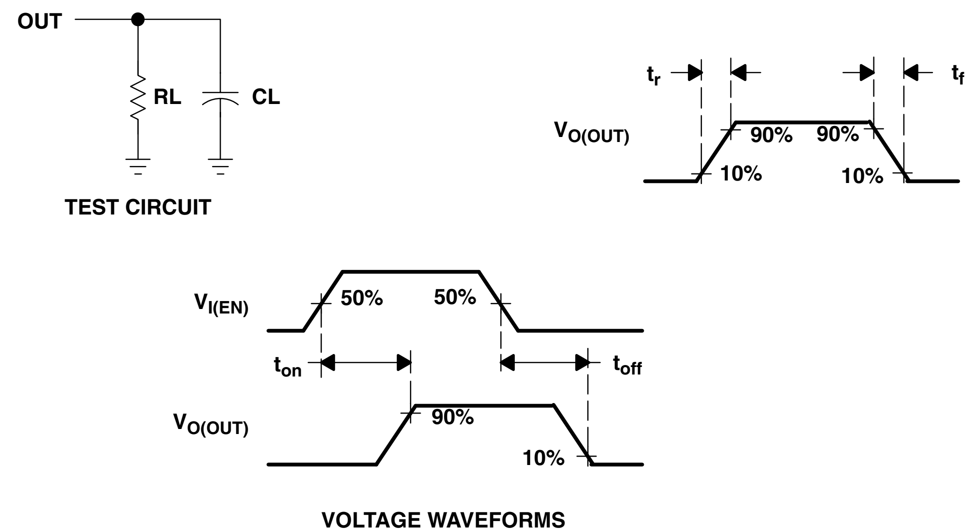


Figure 1. Test Circuit and Voltage Waveforms

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0.9-Ω Load Connected to an Enabled TPS2034 Device	21
0.5-Ω Load Connected to an Enabled TPS2034 Device	22

PARAMETER MEASUREMENT INFORMATION

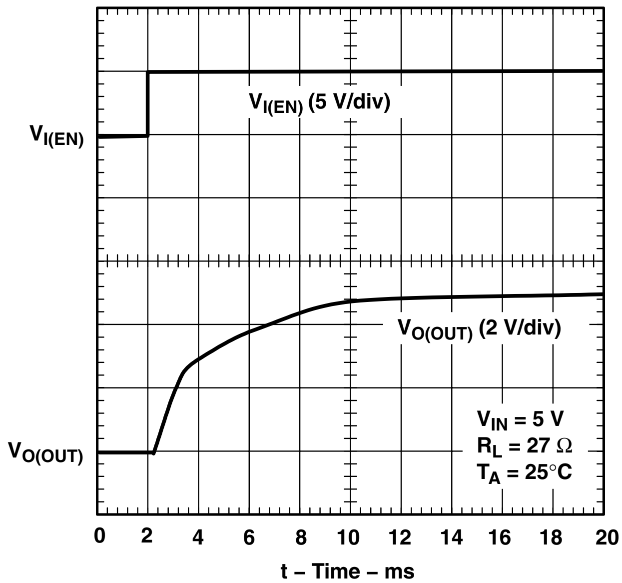

Figure 2. Turnon Delay and Rise Time

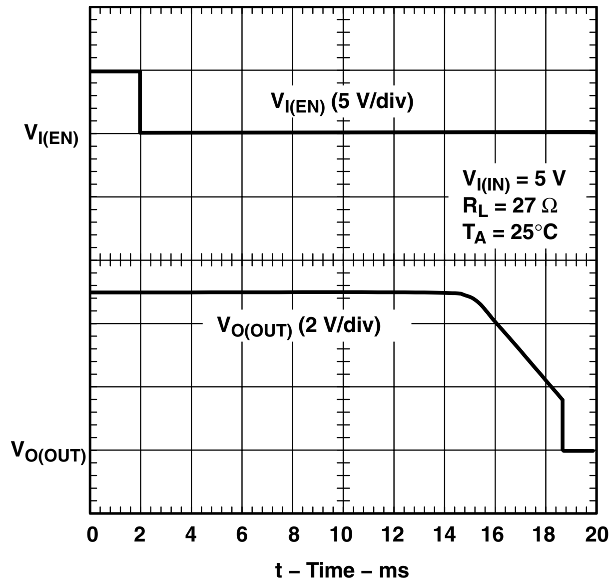

Figure 3. Turnoff Delay and Fall Time

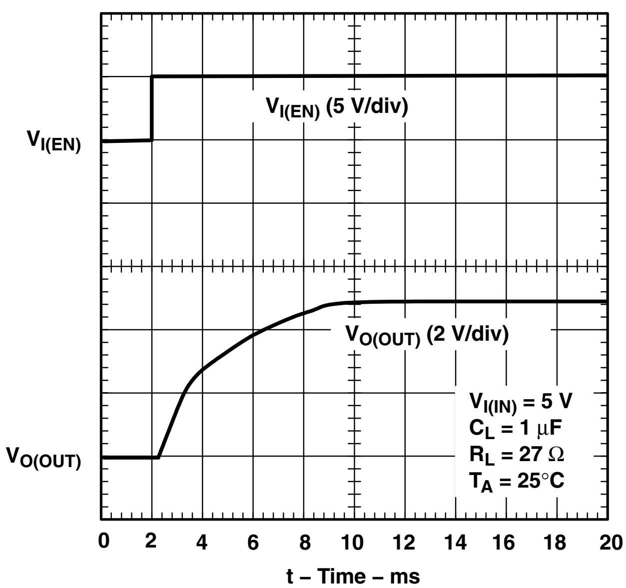

Figure 4. Turnon Delay and Rise Time With 1-μF Load

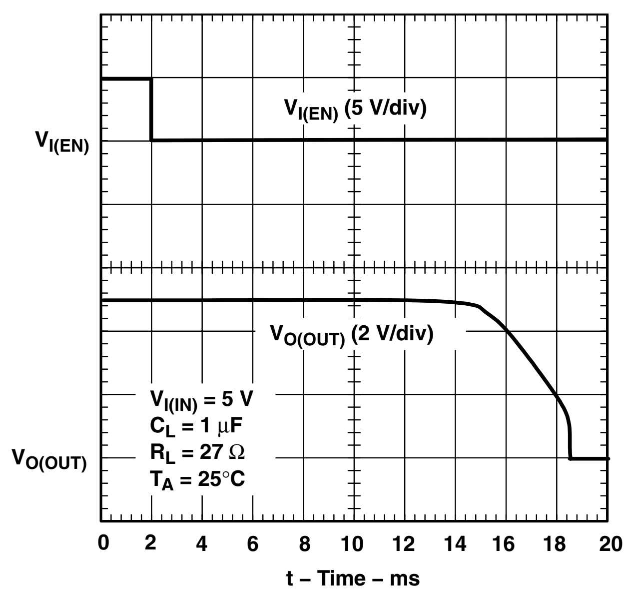

Figure 5. Turnoff Delay and Fall Time With 1-μF Load

PARAMETER MEASUREMENT INFORMATION

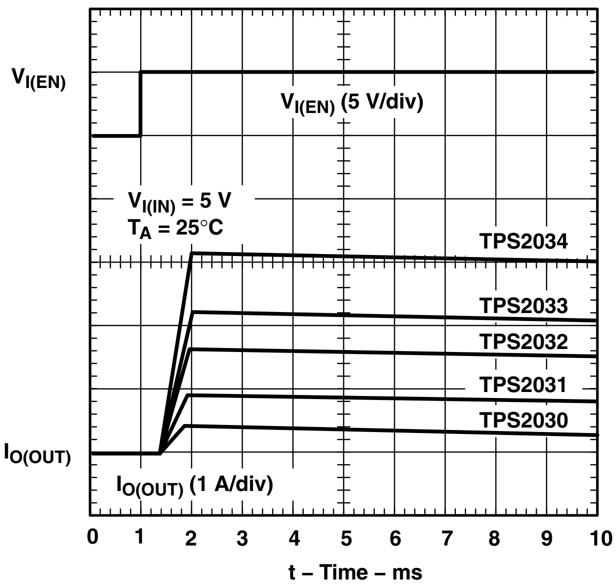

Figure 6. Device Enabled Into Short

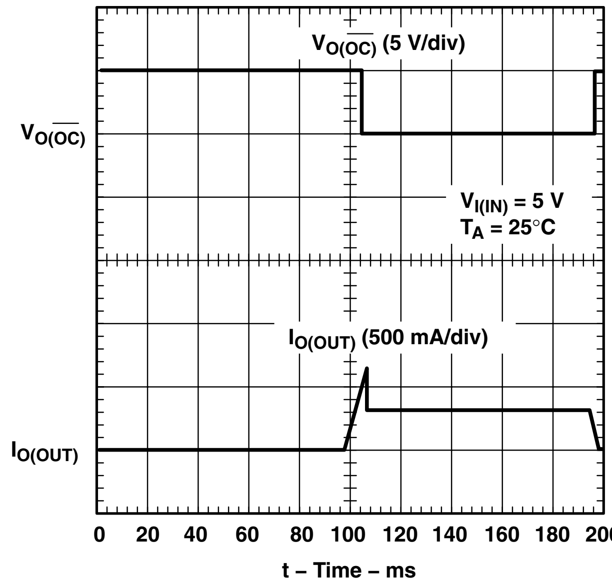

Figure 7. TPS2030, Ramped Load on Enabled Device

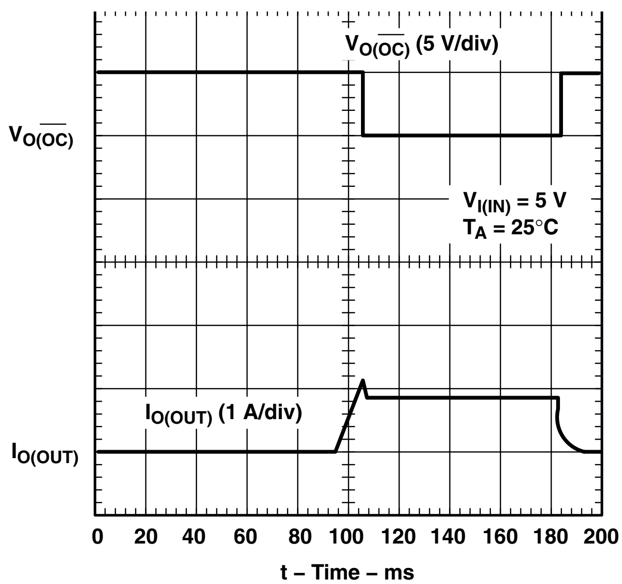

Figure 8. TPS2031, Ramped Load on Enabled Device

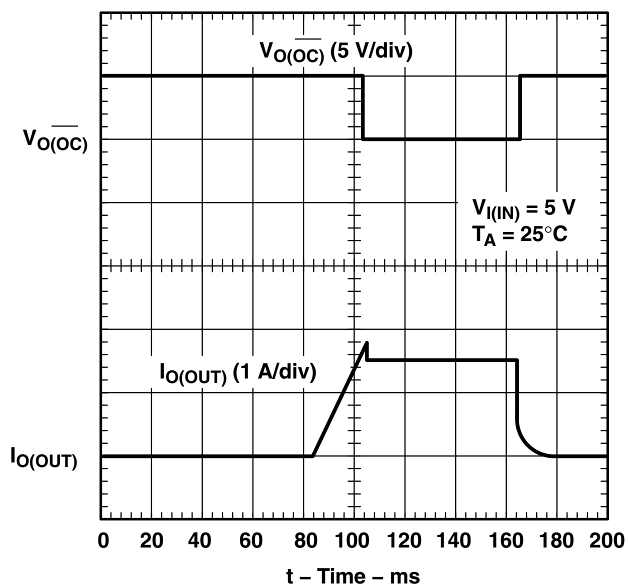

Figure 9. TPS2032, Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

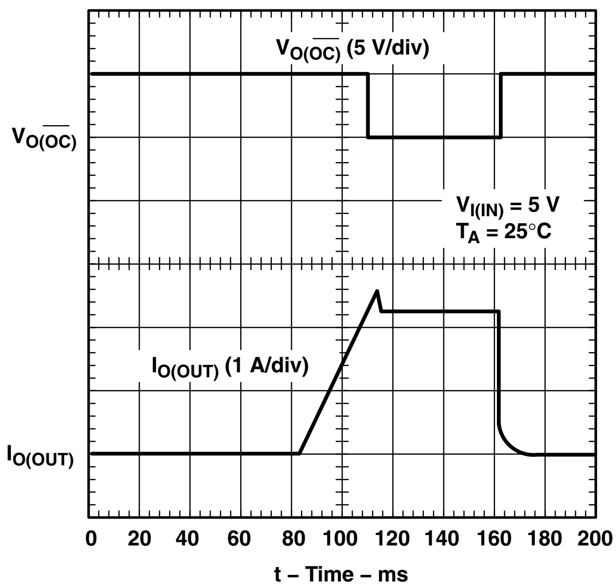

Figure 10. TPS2033, Ramped Load on Enabled Device

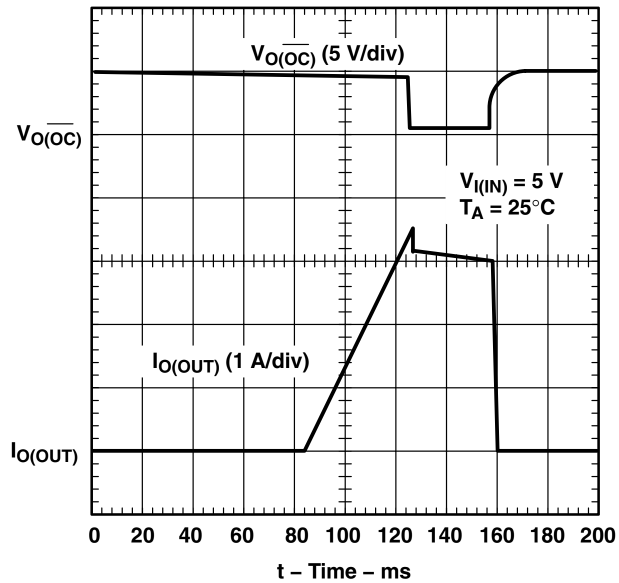

Figure 11. TPS2034, Ramped Load on Enabled Device

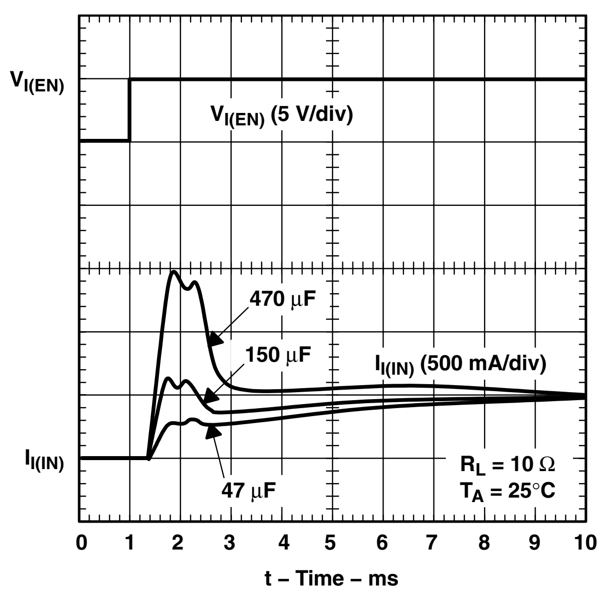

Figure 12. TPS2034, Inrush Current

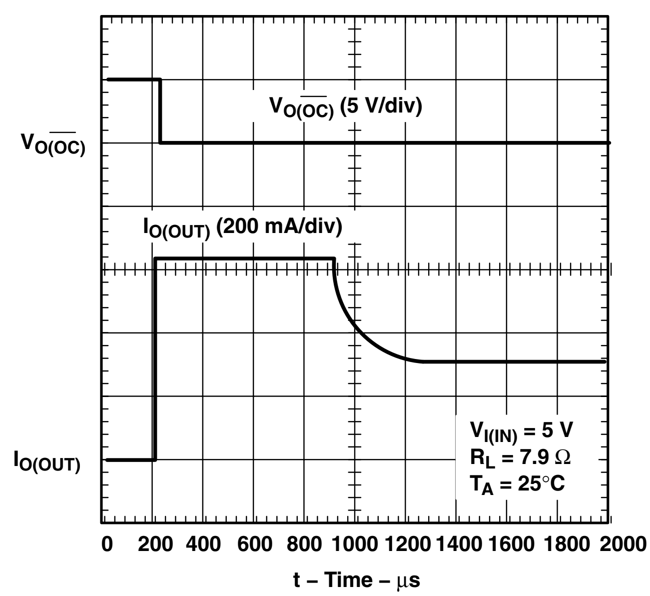

Figure 13. 7.9-Ω Load Connected to an Enabled TPS2030 Device

PARAMETER MEASUREMENT INFORMATION

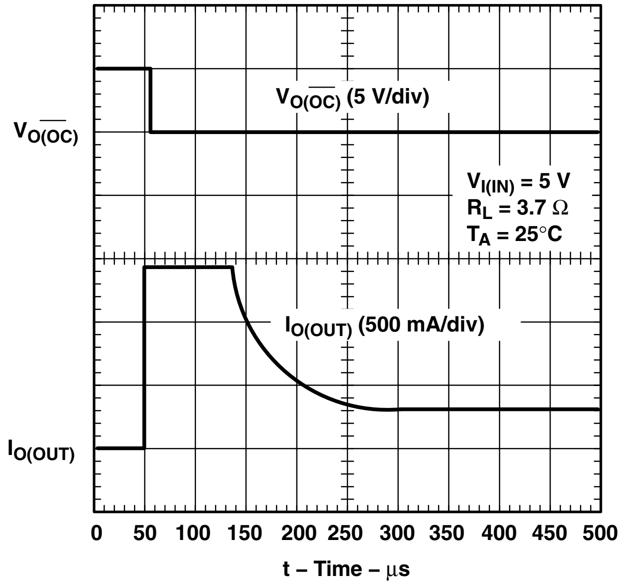

Figure 14. 3.7-Ω Load Connected to an Enabled TPS2030 Device

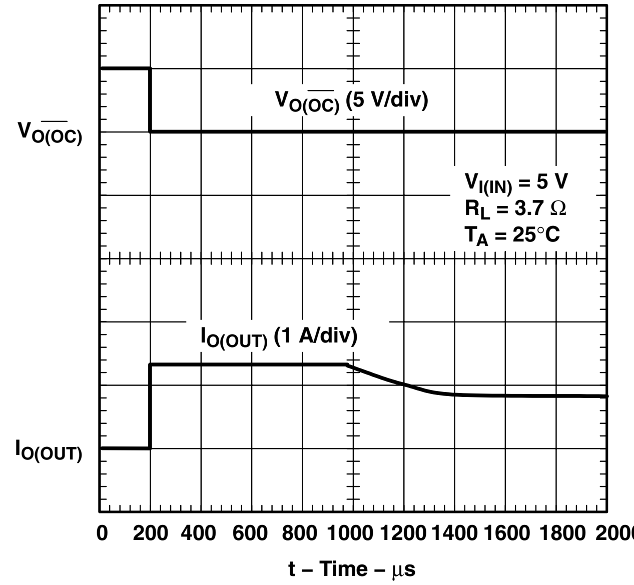

Figure 15. 3.7-Ω Load Connected to an Enabled TPS2031 Device

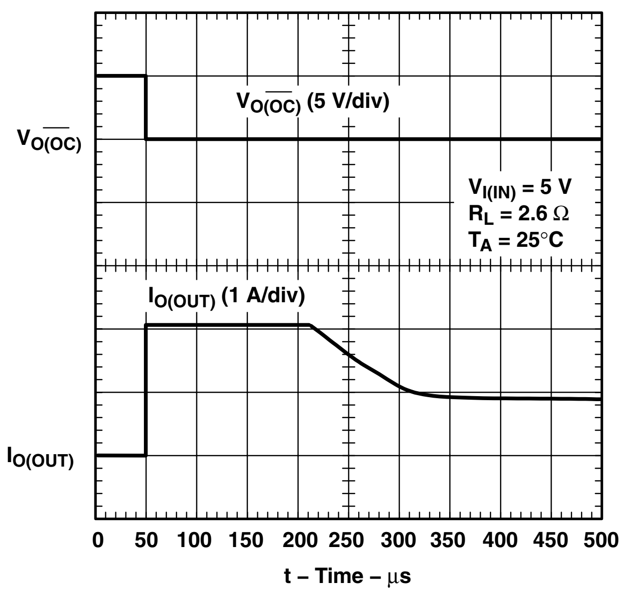

Figure 16. 2.6-Ω Load Connected to an Enabled TPS2031 Device

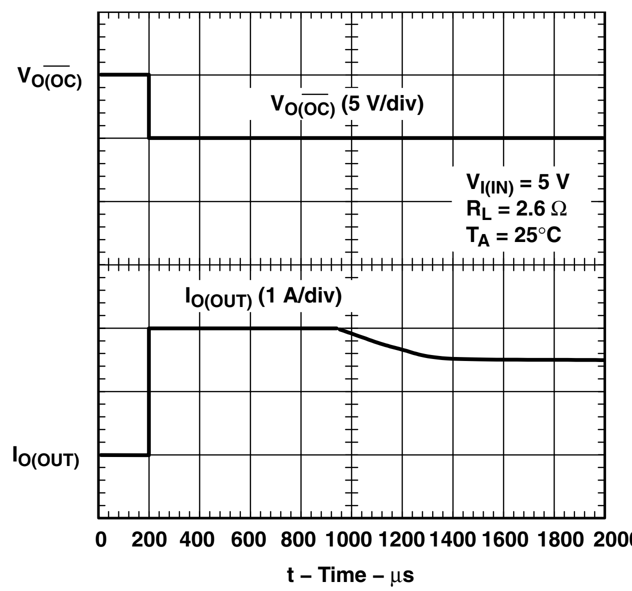

Figure 17. 2.6-Ω Load Connected to an Enabled TPS2032 Device

PARAMETER MEASUREMENT INFORMATION

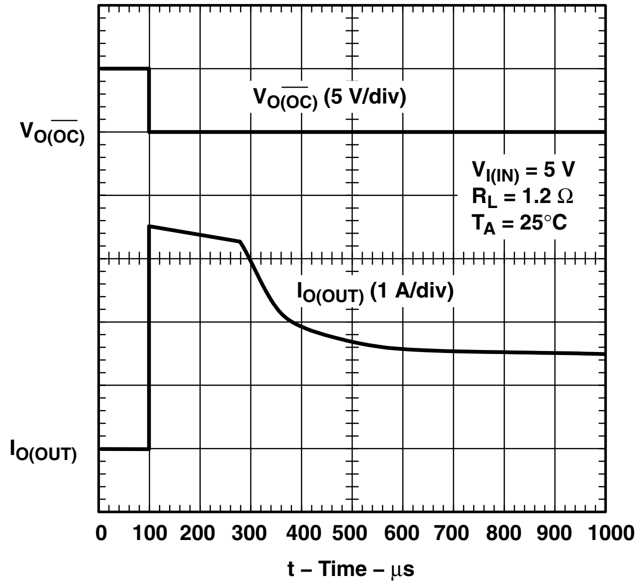

Figure 18. 1.2-Ω Load Connected to an Enabled TPS2032 Device

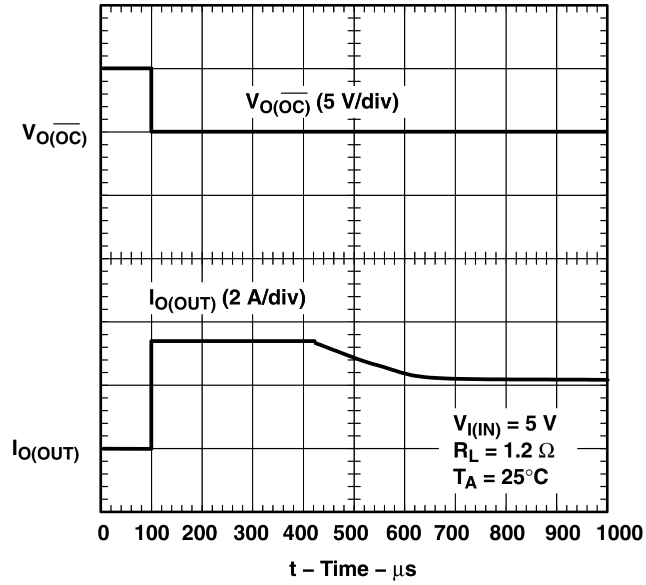

Figure 19. 1.2-Ω Load Connected to an Enabled TPS2033 Device

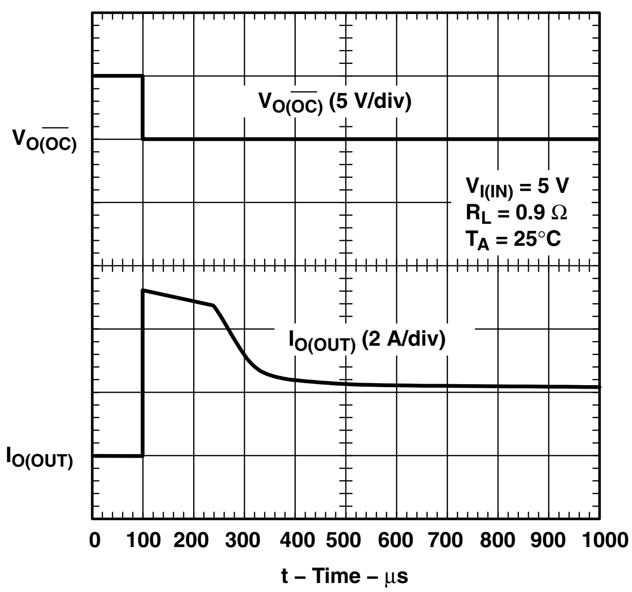

Figure 20. 0.9-Ω Load Connected to an Enabled TPS2033 Device

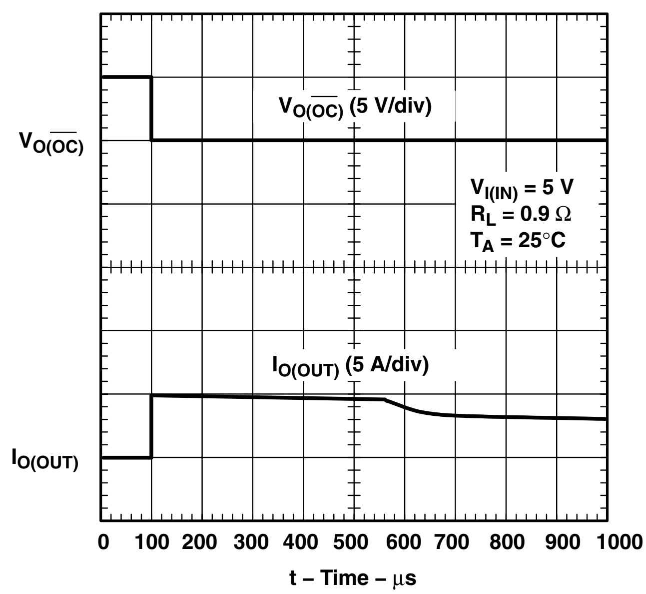

Figure 21. 0.9-Ω Load Connected to an Enabled TPS2034 Device

PARAMETER MEASUREMENT INFORMATION

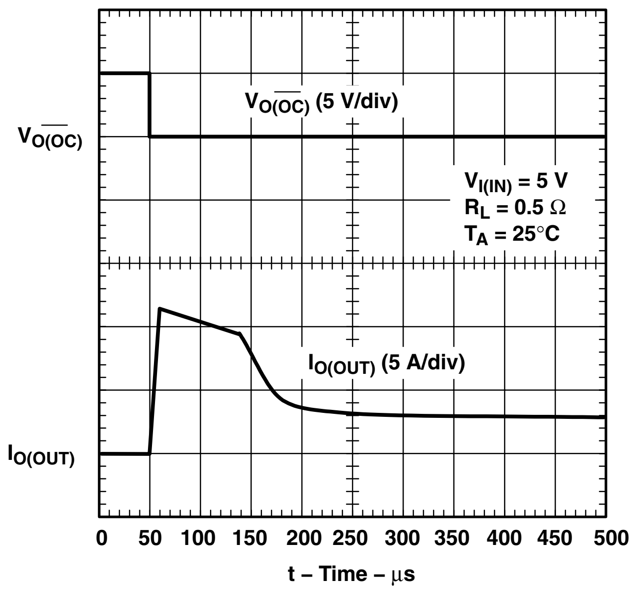

Figure 22. 0.5-Ω Load Connected to an Enabled TPS2034 Device

TYPICAL CHARACTERISTICS

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	Supply current (enabled)	vs Junction temperature	27
	Supply current (disabled)	vs Junction temperature	28
	Supply current (enabled)	vs Input voltage	29
	Supply current (disabled)	vs Input voltage	30
I_{OS}	Short-circuit current limit	vs Input voltage	31
		vs Junction temperature	32
$r_{DS(on)}$	Static drain-source on-state resistance	vs Input voltage	33
		vs Junction temperature	34
		vs Input voltage	35
		vs Junction temperature	36
V_I	Input voltage	Undervoltage lockout	37

TYPICAL CHARACTERISTICS

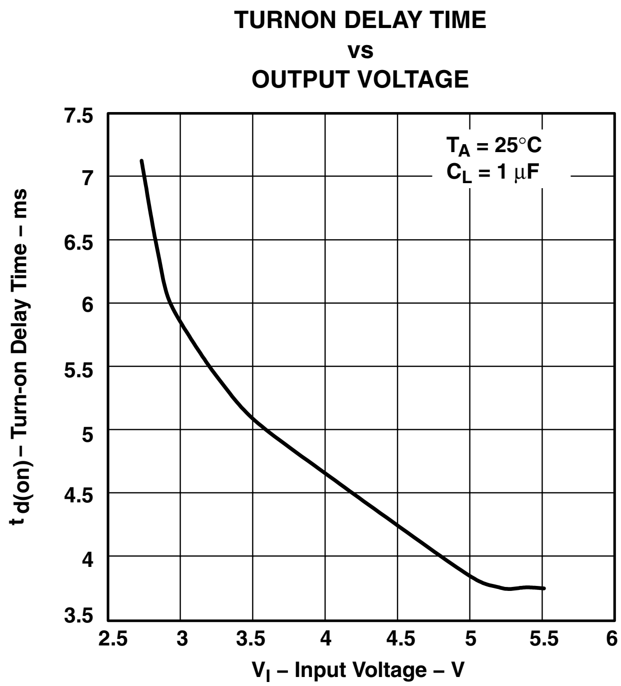


Figure 23

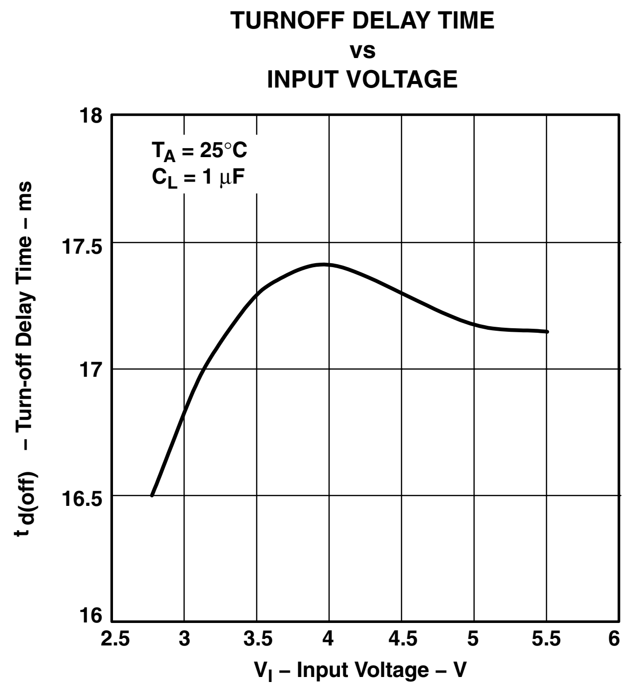


Figure 24

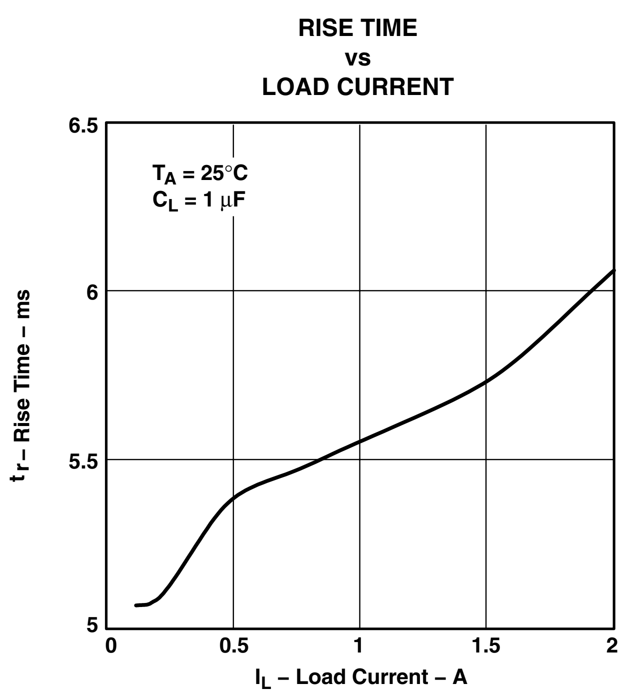


Figure 25

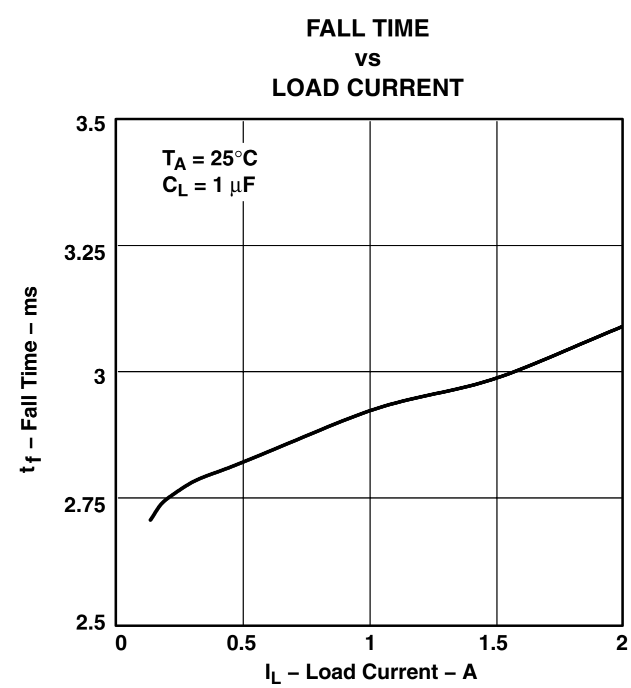


Figure 26

TYPICAL CHARACTERISTICS

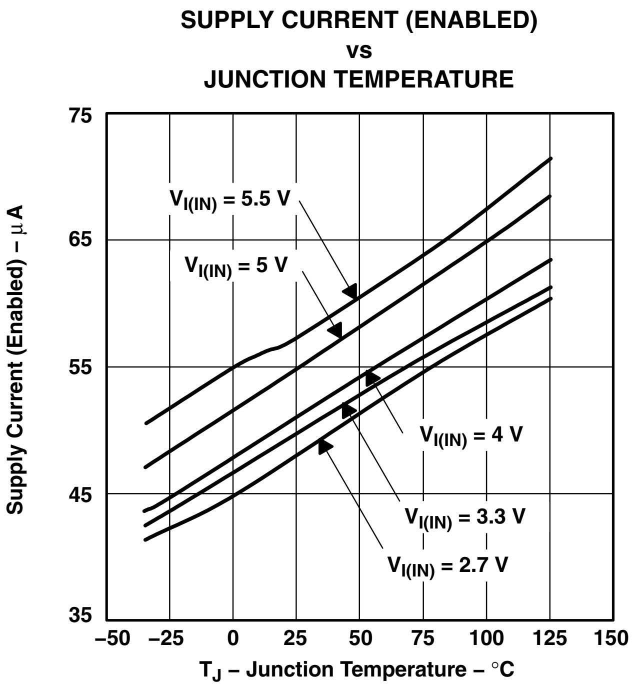
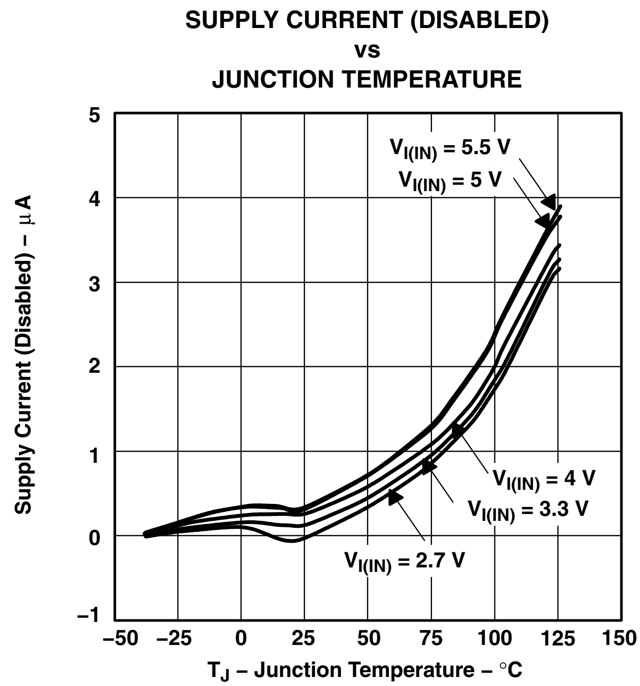


Figure 27



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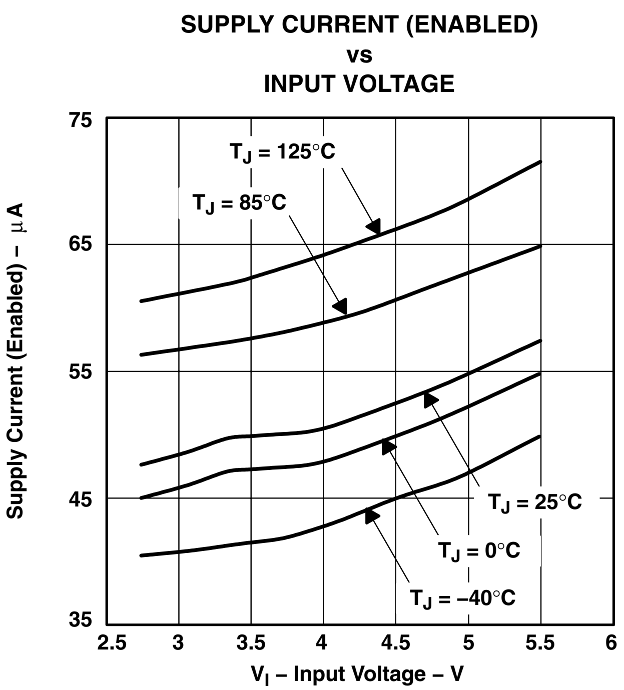

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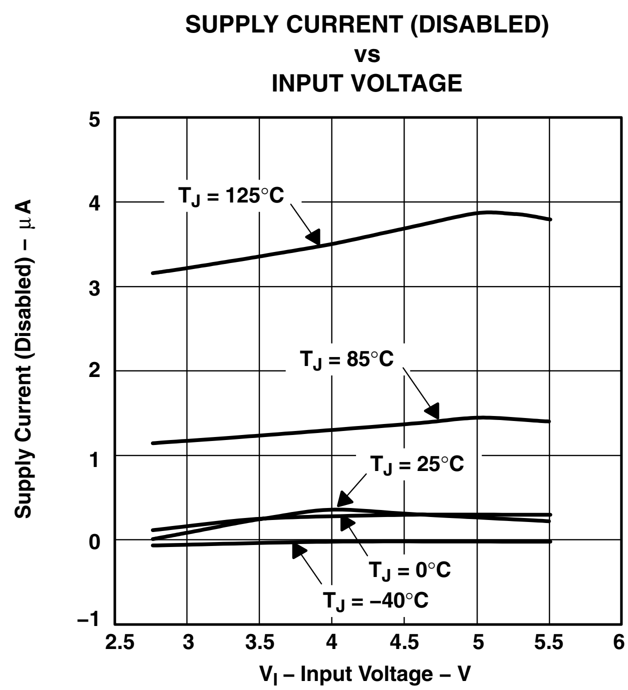

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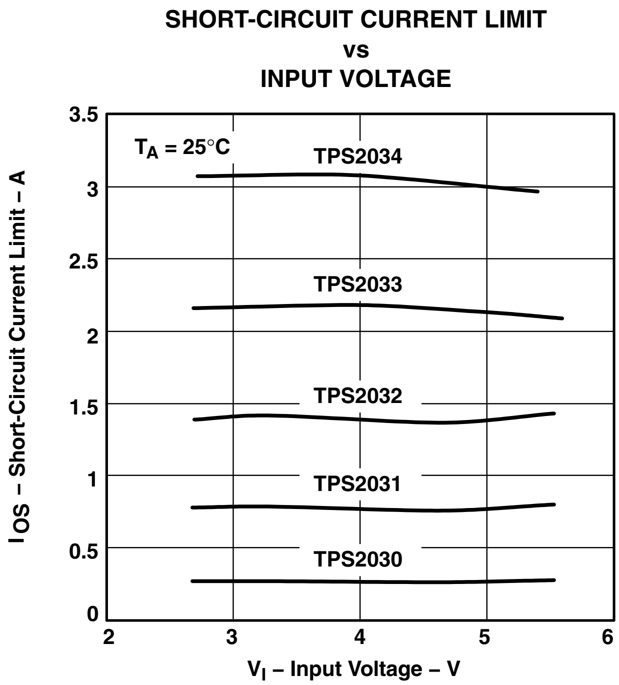

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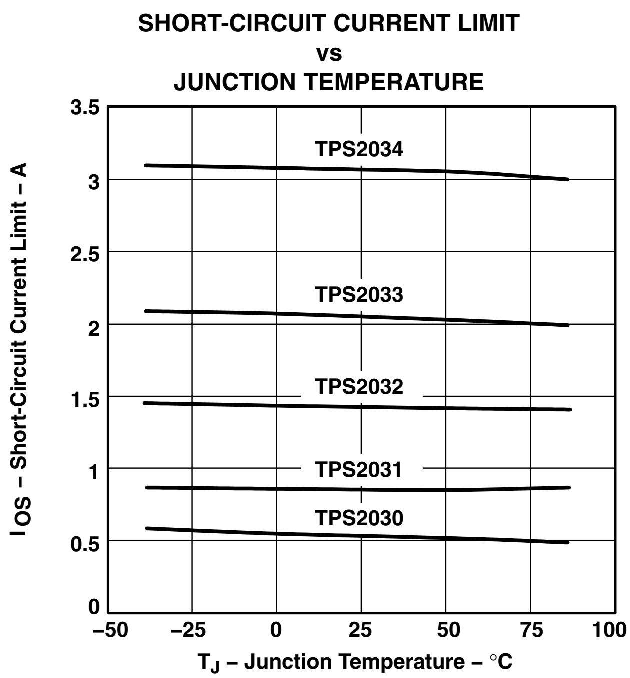

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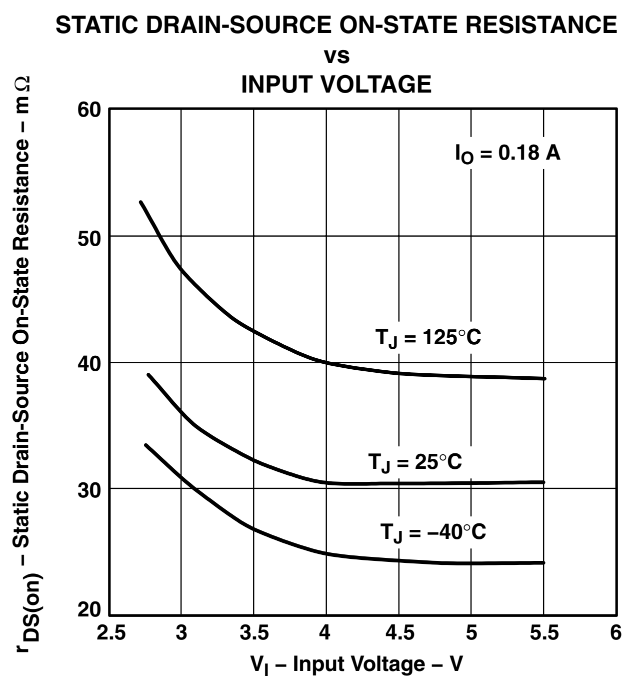

Figure 33

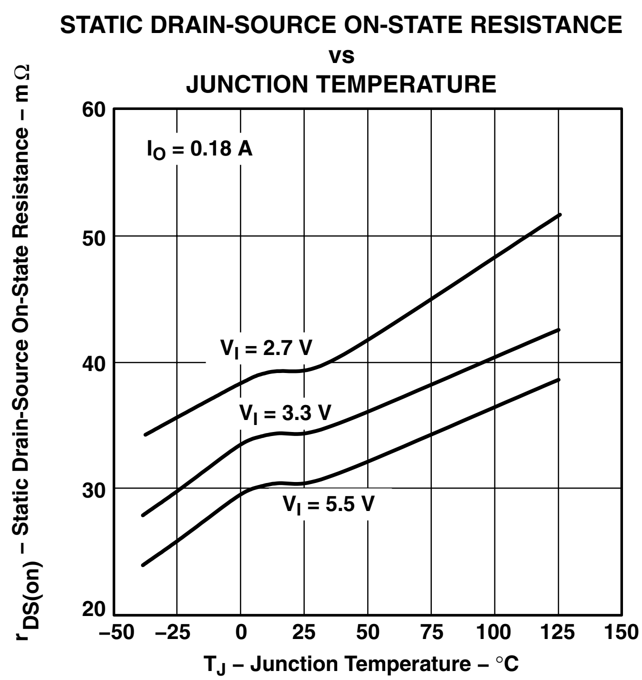

Figure 34

TYPICAL CHARACTERISTICS

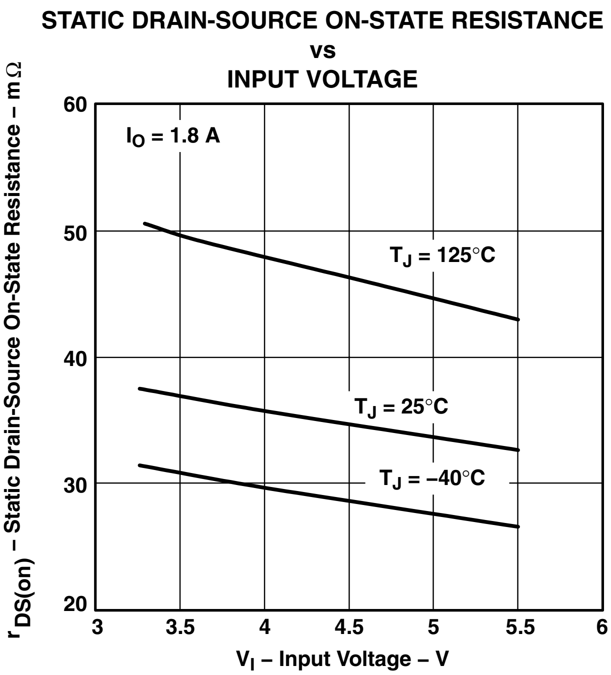

Figure 35

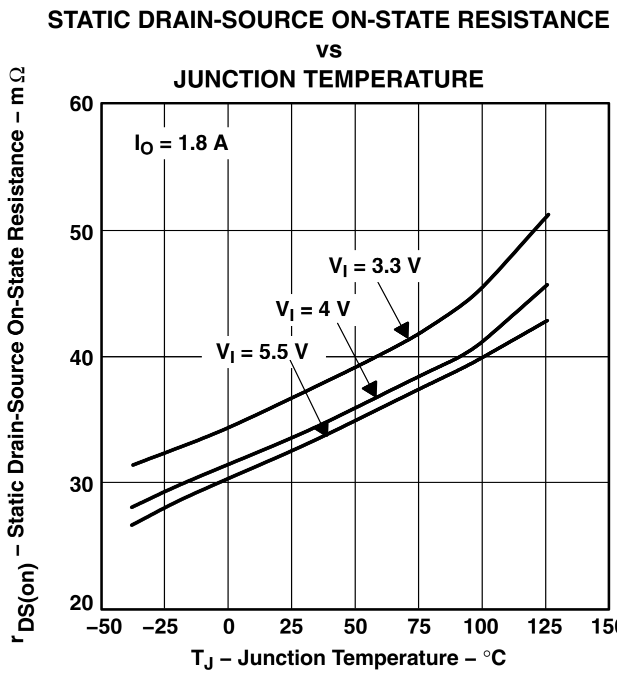

Figure 36

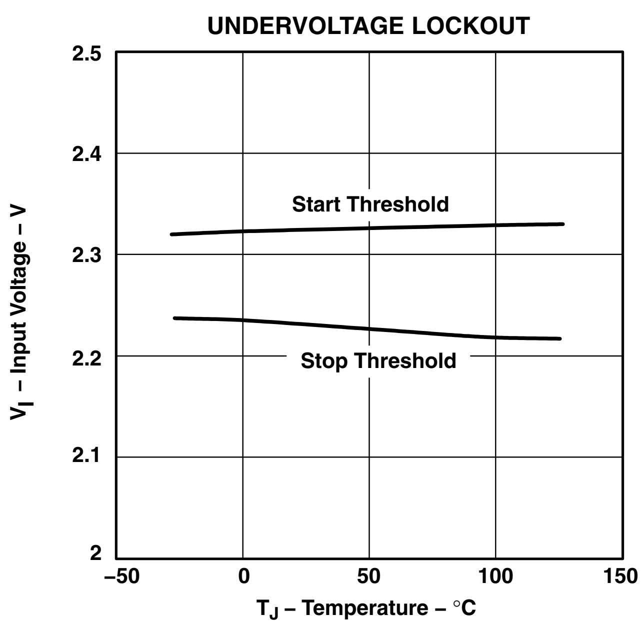

Figure 37

APPLICATION INFORMATION

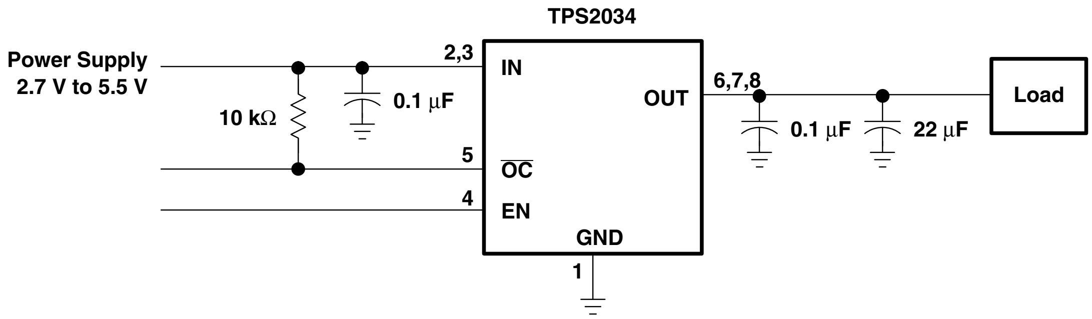

Figure 38. Typical Application

power supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This precaution reduces power supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS203x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, high currents may flow for a short time before the current-limit circuit can react (see Figure 13 through Figure 22). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7 through Figure 11). The TPS203x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the $\overline{\text{OC}}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

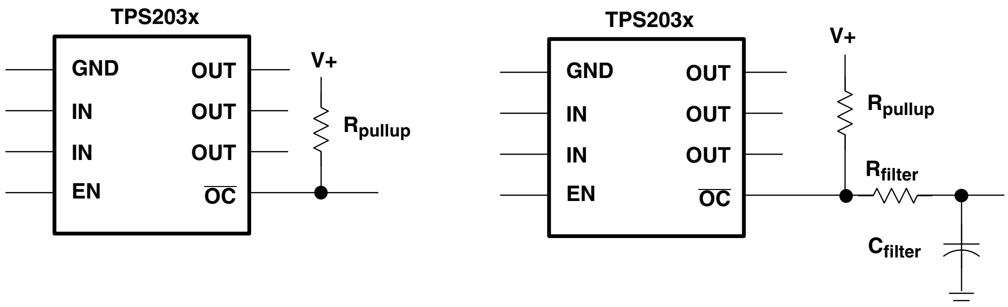

Figure 39. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 33 through Figure 36. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS203x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

generic hot-plug applications (see Figure 40)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS203x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS203x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature assures a soft start with a controlled rise time for every insertion of the card or module.

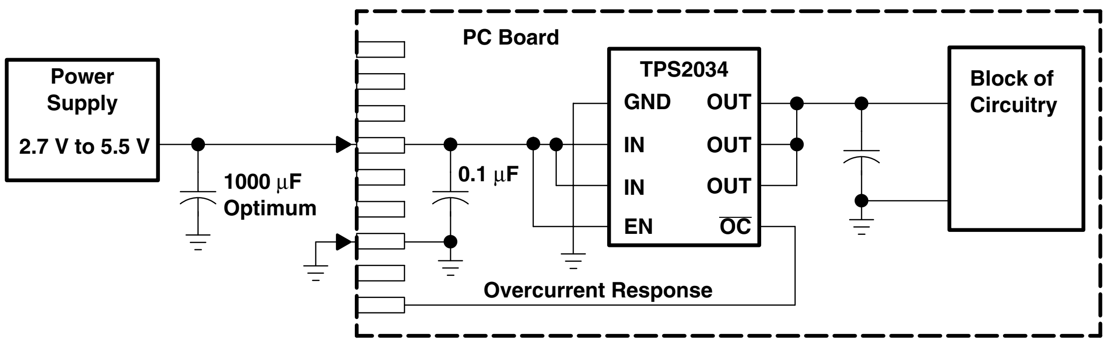

Figure 40. Typical Hot-Plug Implementation

By placing the TPS203x between the V_{CC} input and the rest of the circuitry, the input power reaches this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2030IDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2030Q1
TPS2030IDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2030Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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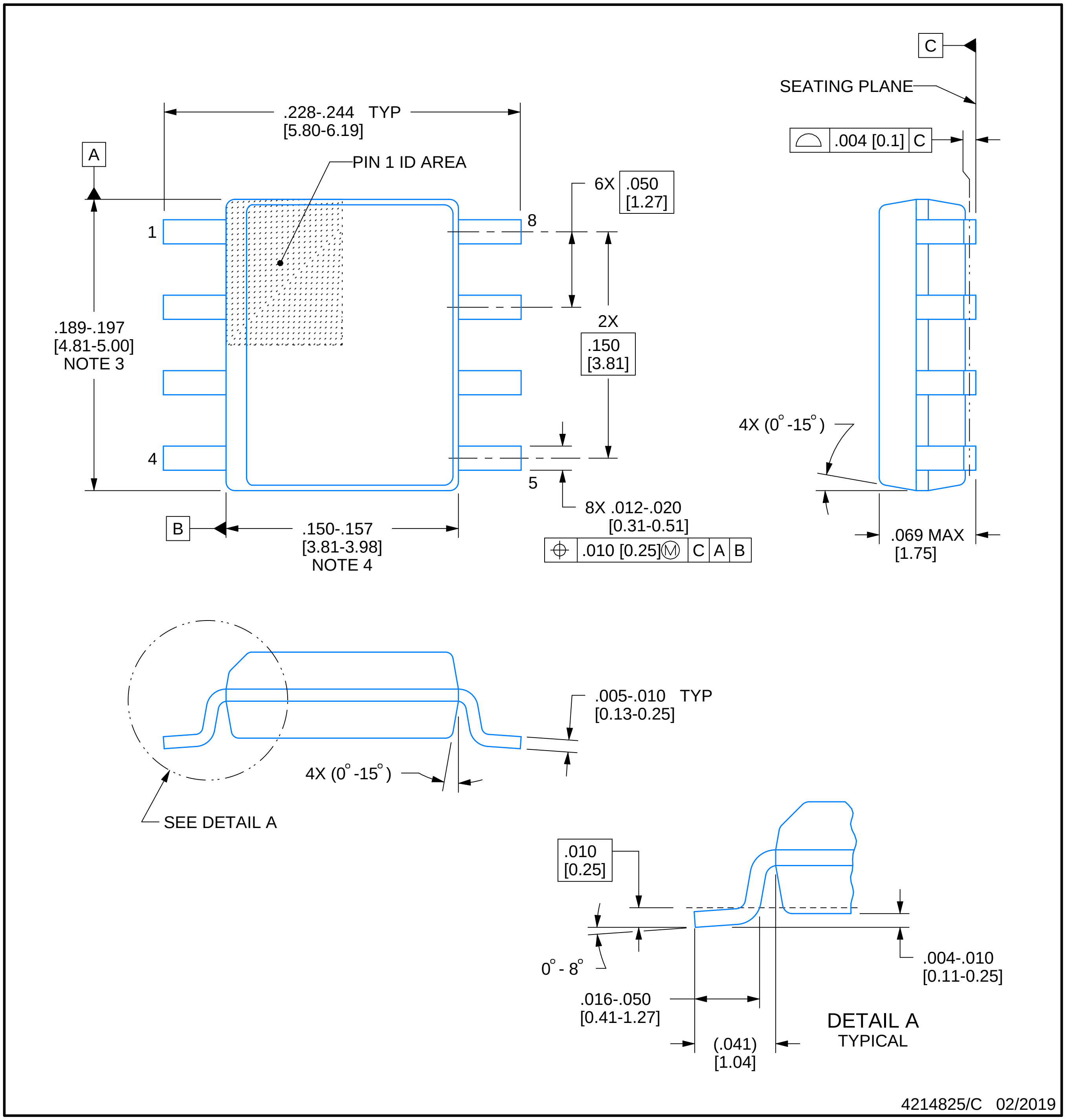
OTHER QUALIFIED VERSIONS OF TPS2030-Q1 :

- Catalog : TPS2030

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



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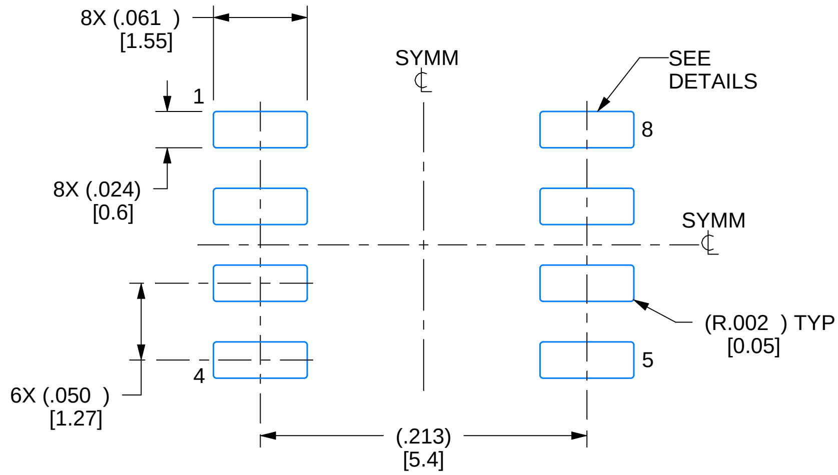
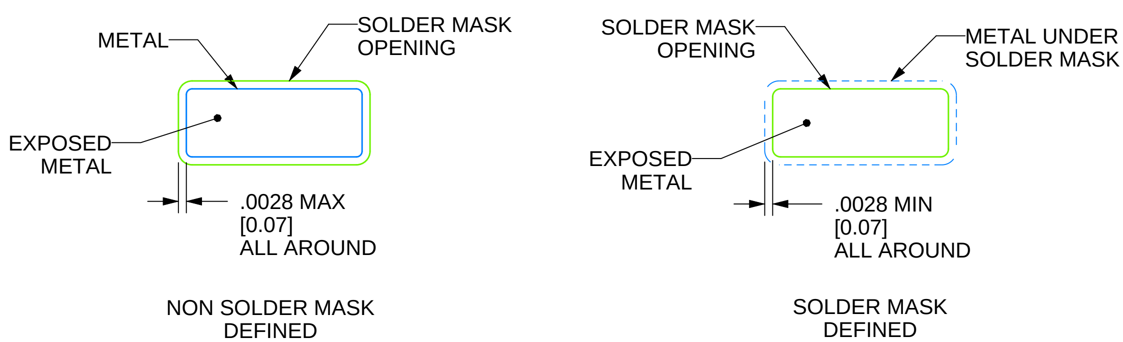
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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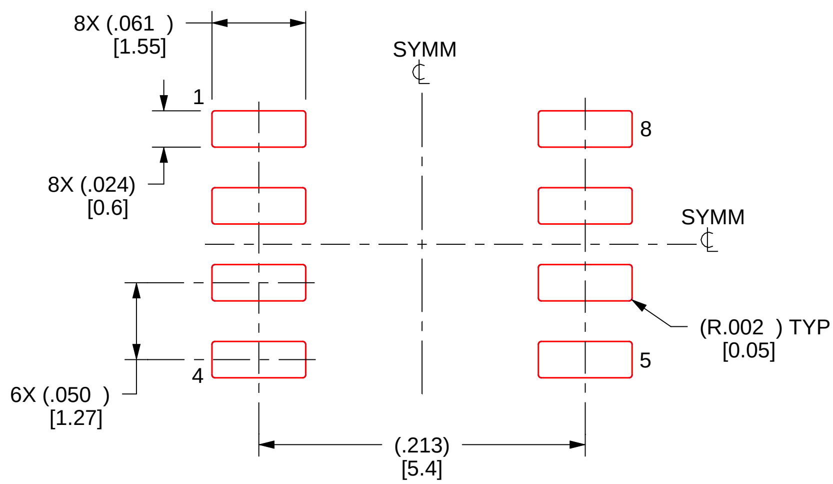
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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