TPS61376 $23V_{IN}$, $25V_{OUT}$, 4.5A, Boost Converter with up to ±2.5% Accuracy Input Average Current Limit and True Load Disconnection

1 Features

- Wide input voltage and output voltage range
  - Input voltage range: 2.9V to 23V
  - Output voltage range: 4.5V to 25V
- Peak inductor current limit up to 4.5A
- Programmable input average current limit range: 0.1A to 3A
- Switching frequency: 1.2MHz
- Integrated two MOSFETs
  - ISO FET: 40mΩ
  - Low-side FET: 50mΩ
- Safety and robust operation features
  - Output overvoltage protection
  - Cycle-by-cycle overcurrent protection
  - True disconnection between input and output during EN shutdown
  - Thermal shutdown
- Precise EN/UVLO threshold
- External loop compensation
- 2.5mm × 2.0mm HotRod™ Lite VQFN package

2 Applications

- ePOS retail automation and payment
- Barcode scanner
- Smart speaker
- Appliances

3 Description

The TPS61376 is a high voltage non-synchronous boost converter with input average current limit and true load disconnect functions. The input average current limit threshold can be programmed through the ILIM pin from 0.1A to 3.0A. The isolation FET between the VP and SW pin will completely cut off the path between input and output when the device is disabled. The TPS61376 has a wide input voltage range from 2.9V to 23V and output voltage covers up to 25V.

The TPS61376 implements the peak current mode with the adaptive off-time control topology. The device works in PWM mode at moderate to heavy loads. At the light load conditions, the device enters PFM mode to maintain high efficiency over the entire load current range.

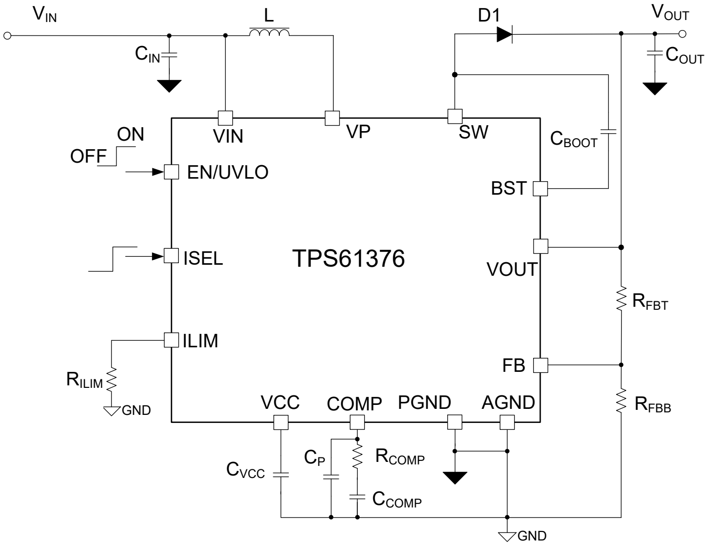
The TPS61376 also integrates robust protection features including output overvoltage protection, cycle-by-cycle overcurrent protection and thermal shutdown.

The TPS61376 offers a very small solution size with a 2.5mm × 2.0mm HotRod™ Lite VQFN package.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
TPS61376	VQFN (13)	2.5mm × 2.0mm

[1] For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

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4 Pin Configuration and Functions

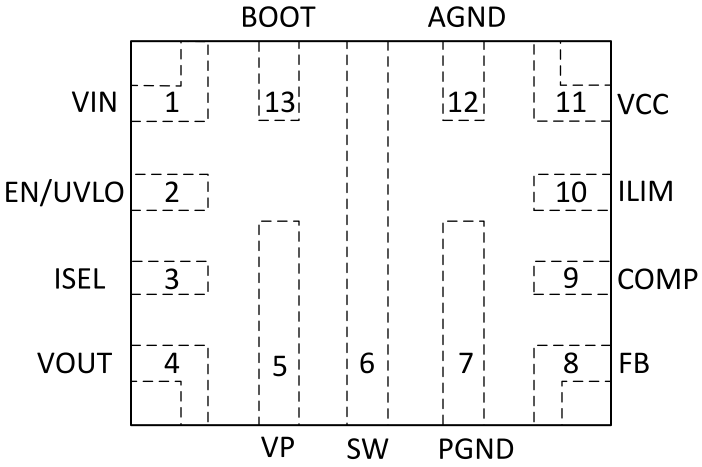


Figure 4-1. 13-Pin RYH VQFN Package (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VIN	1	I	IC power supply input
EN/UVLO	2	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider.
ISEL	3	I	Scale the ISO FET to improve input average current limit accuracy and adjust peak switching current limit value. ISEL = low when setting $I_{limit} \leq 750mA$ ISEL = high, when setting $I_{limit} > 750mA$
VOUT	4	PWR	Boost converter output
VP	5	PWR	Drain of the ISO MOSFET
SW	6	PWR	The switching node pin. It is connected to the drain of the internal low-side power MOSFET and the source of the internal ISO power MOSFET.
PGND	7	PWR	Power ground of the IC
FB	8	I	Output voltage feedback pin. Connect to the center tape of a resistor divider to program the output voltage.
COMP	9	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
ILIM	10	I	Input average current limit setting pin. Use a resistor between this pin and AGND to set the desired input average current limit threshold.
VCC	11	O	Output of the internal regulator. A ceramic capacitor of more than 1µF is required between this pin and AGND.
AGND	12	PWR	Analog ground of the IC
BOOT	13	O	Power supply for ISO MOSFET gate driver. A ceramic capacitor of more than 0.47µF must be connected between this pin and the SW pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range at terminals [2]	VIN, EN/UVLO	–0.3	25	V
	SW, VOUT, VP	–0.3	30	V
	BST	–0.3	SW + 6	V
	ISEL, FB, ILIM, VCC, COMP	–0.3	6	V
T_J [3]	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ [1]	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.9		23	V
V_{OUT}	Output voltage	4.5		25	V
L	Inductance, effective value	2.2	4.7	10	µH
C_I	Input capacitance, effective value		10		µF
C_O	Output capacitance, effective value	10		2000	µF
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS61376	UNIT
		VQFN	
		13 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

T_J = -40 to 125°C, L = 4.7 µH, V_{IN} = 5 V and V_{OUT} = 12 V. Typical values are at T_J = 25°C, (unless otherwise noted)

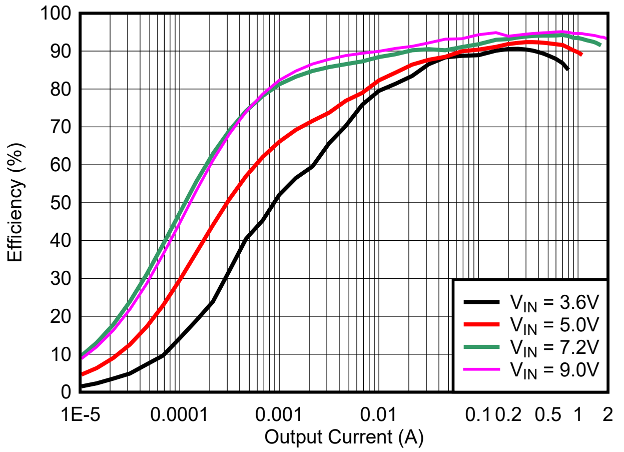
PARAMETER	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.9		23	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN} rising		2.8	2.9	V
		V_{IN} falling		2.6	2.7	V
V_{IN_HYS}	VIN UVLO hysteresis			200		mV
I_Q	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} = 2.9V to 5.25V, V_{OUT} = 25 V, V_{FB} = V_{REF} + 0.1V		80	110	µA
I_Q	Quiescent current into V_{OUT} pin	IC enabled, no load, no switching V_{IN} = 5.5V to 23V, V_{OUT} = 25 V, V_{FB} = V_{REF} + 0.1V		2	8	µA
	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} = 2.9V to 5.25V, V_{FB} = V_{REF} + 0.1V		1.5	2	µA
I_Q	Quiescent current into V_{IN} pin	IC enabled, no load, no switching V_{IN} = 5.5V to 23V, V_{FB} = V_{REF} + 0.1V		80	110	µA
V_{CC_UVLO}	VCC UVLO threshold	V_{CC} rising		2.75		V
V_{CC_HYS}	VCC UVLO hysteresis	V_{CC} hysteresis		160		mV
V_{CC}	VCC regulation	I_{VCC} = 4mA, V_{OUT} = 12V		4.80		V
I_{SD}	Shutdown current into V_{IN} pin	IC disabled, V_{IN} = 2.9V to 23V, EN = GND			1.25	µA
I_{SW_LKG}	Leakage current into SW	IC disabled, VP = 0V, SW = 25V,T_J up to 85°C			2	µA
I_{VP_LKG}	Leakage current into VP	IC disabled, VP = 25V, SW = 0V,T_J up to 85°C			2	µA
I_{FB_LKG}	Leakage current into FB	IC disabled, T_J up to 85°C			16	nA
OUTPUT VOLTAGE						
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 3.3V, V_{OUT} rising	26.5	27.5	28.6	V
V_{OVP_HYS}	Output over-voltage protection hysteresis	V_{IN} = 3.3V, OVP threshold		0.9		V
VOLTAGE REFERENCE						
V_{REF}	Reference Voltage at FB pin	T_J = –40 to 125°C	0.985	1	1.015	V
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{CC} = 4.85V,		50		mΩ
$R_{DS(on)}$	ISO MOSFET on resistance	V_{CC} = 4.85V, ISEL = high		40		mΩ
$R_{DS(on)}$	ISO MOSFET on resistance(scale)	V_{CC} = 4.85V, ISEL = low		160		mΩ
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit	R_{LIM} = 14.4kΩ, ISEL = high ,V_{IN} = 2.9V to 23V	3.76	4.5	5.35	A
I_{LIM_SW}	Peak switching current limit	R_{LIM} = 14.4kΩ, ISEL = low, V_{IN} = 2.9V to 23V	1.7	2.5	3.3	A
$I_{LIM\_DC\_Range}$	Input DC current limit range		0.1		3	A
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 1.5 A to 3.0 A	VIN = 5V, VOUT = 12V, T_J = 25°C	–2.5		2.5	%
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 0.75 A to 1.5 A	VIN = 5V, VOUT = 12V, T_J = 25°C	–5		5	%
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 0.1 A to 0.75 A	VIN = 5V, VOUT = 12V, T_J = 25°C	–10		10	%
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 0.75 A to 3.0 A	VIN = 2.9V to 23V, VOUT = 4.5V to 25 V, T_J = –40 to 125°C	–5		5	%
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 0.2 A to 0.75 A	VIN = 2.9V to 23V, VOUT = 4.5V to 25V, T_J = –40 to 125°C	–10		10	%
$I_{LIM\_DC\_Accuracy}$	Input DC current limit 0.1 A to 0.2 A	VIN = 2.9V to 23V, VOUT = 4.5V to 25V, T_J = –40 to 125°C	–20		20	%
SWITCHING FREQUENCY						
Fsw	Switching frequency	V_{IN} = 2.9V to 23V, V_{OUT} = 4.5V to 25V		1200		kHz

T_J = -40 to 125°C, L = 4.7 μH, V_{IN} = 5 V and V_{OUT} = 12 V. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SS}	Soft-start time			4		ms
t_{OFF_min}	Minimum off time			120		ns
t_{ON_min}	Minimum on time			65		ns
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current			20		µA
I_{SOURCE}	COMP pin source current			20		µA
V_{CCLPH}	COMP pin high clamp voltage			1.6		V
V_{CCLPL}	COMP pin low clamp voltage			0.5		V
G_{mEA}	Error amplifier trans conductance			240		µS
LOGIC INTERFACE						
V_{EN_H}	EN Logic high threshold				0.812	V
V_{EN_L}	EN Logic low threshold		0.36			V
V_{EN_L}	EN threshold hysteresis			120		mV
V_{UVLO}	UVLO rising threshold		0.790	0.813	0.835	V
I_{UVLO_HYS}	Sourcing current at the EN/UVLO pin		1.75	2	2.25	µA
VI_H	ISEL pins Logic high threshold				0.84	V
VI_L	ISEL pins Logic Low threshold		0.36			V
R_{DOWN}	ISEL pins internal pull down resistor			800		kΩ
THERMAL SHUTDOWN						
t_{SD_R}	Thermal shutdown rising threshold	T_J rising		150		°C
t_{SD_F}	Thermal shutdown falling threshold	T_J falling		130		°C

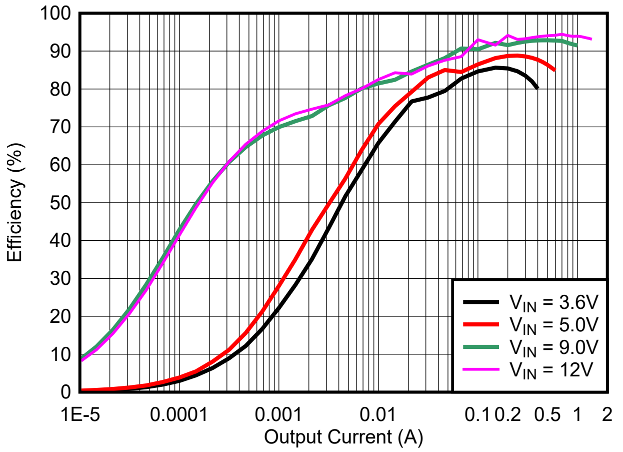
5.6 Typical Characteristics

TPS61376 Fsw = 1.2MHz, T_A = 25°C, unless otherwise noted.



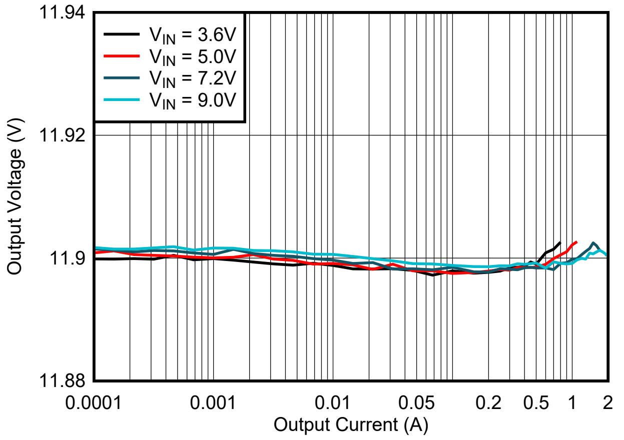
V_{IN} = 3.6V, 5.0V, 7.2V, 9.0V V_{OUT} = 12V

Figure 5-1. Efficiency vs Output Current, V_{OUT} = 12V



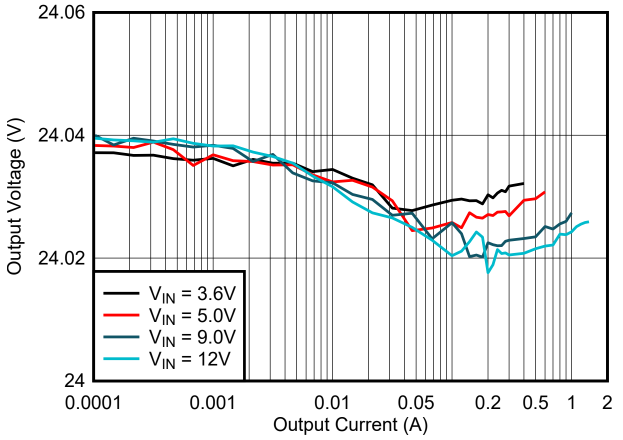
V_{IN} = 3.6V, 5.0V, 9.0V, 12V V_{OUT} = 24V

Figure 5-2. Efficiency vs Output Current, V_{OUT} = 24V



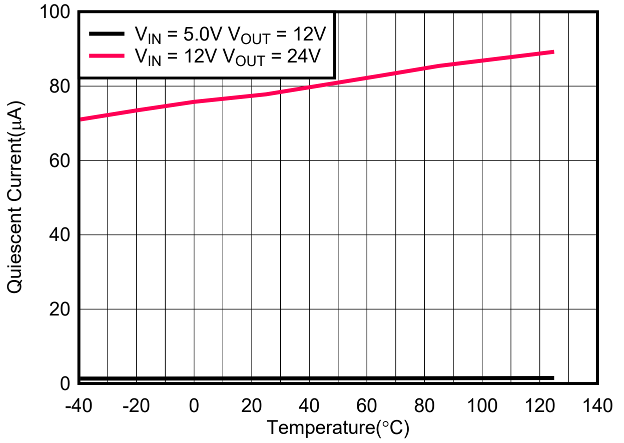
V_{IN} = 3.6V, 5.0V, 7.2V, 9.0V V_{OUT} = 12V

Figure 5-3. Load regulation, V_{OUT} = 12V



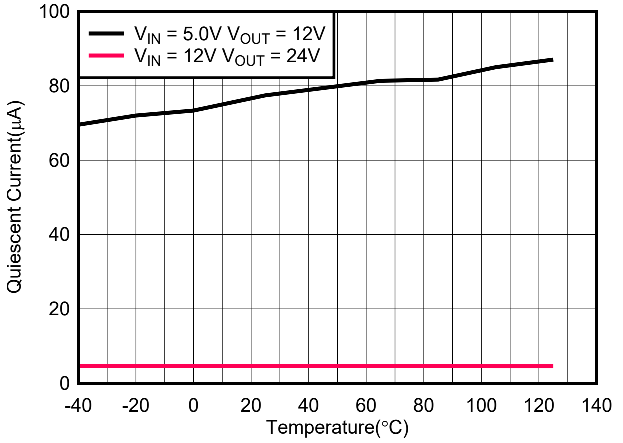
V_{IN} = 3.6V, 5.0V, 9.0V, 12V V_{OUT} = 24V

Figure 5-4. Load regulation, V_{OUT} = 24V



V_{IN} = 5.0V;12V V_{OUT} = 12V;24V

Figure 5-5. Quiescent Current into VIN vs Temperature



V_{IN} = 5.0V;12V V_{OUT} = 12V;24V

Figure 5-6. Quiescent Current into VOUT vs Temperature

5.6 Typical Characteristics (continued)

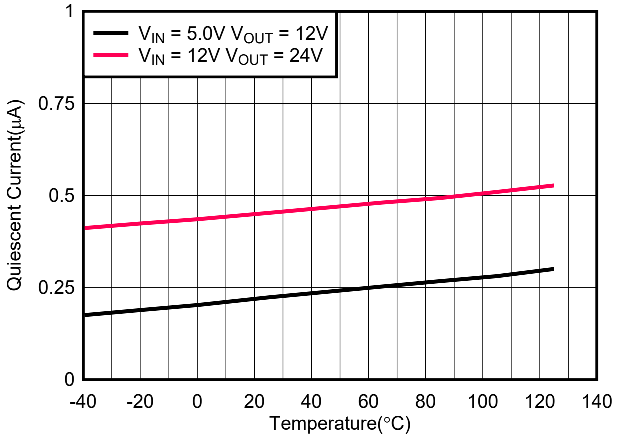


Figure 5-7. Shutdown Current vs Temperature

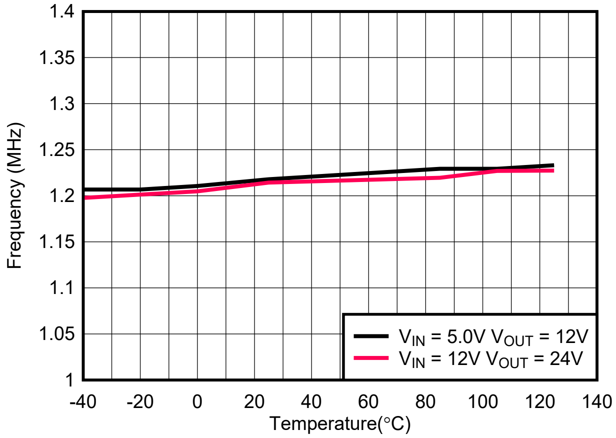


Figure 5-8. Switching Frequency vs Temperature

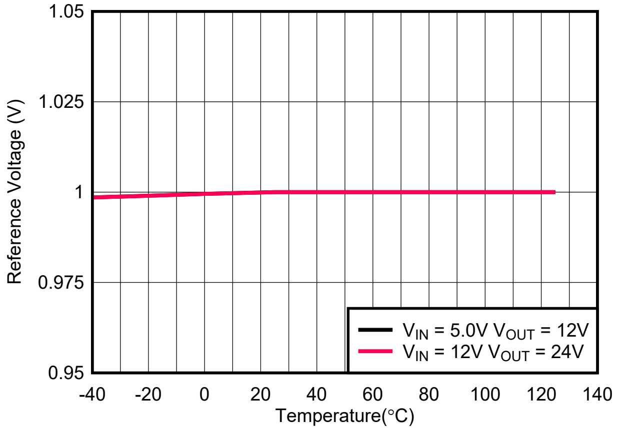


Figure 5-9. Reference Voltage vs Temperature

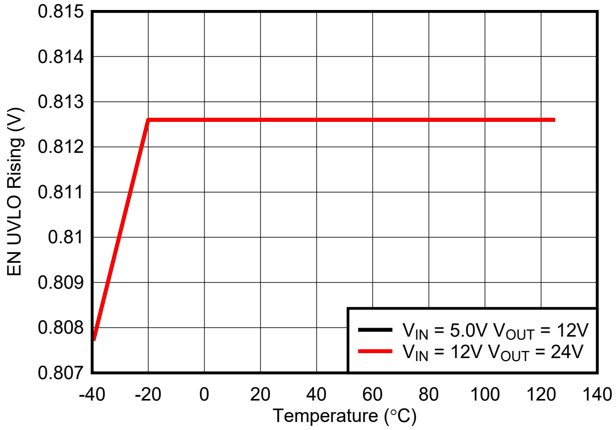


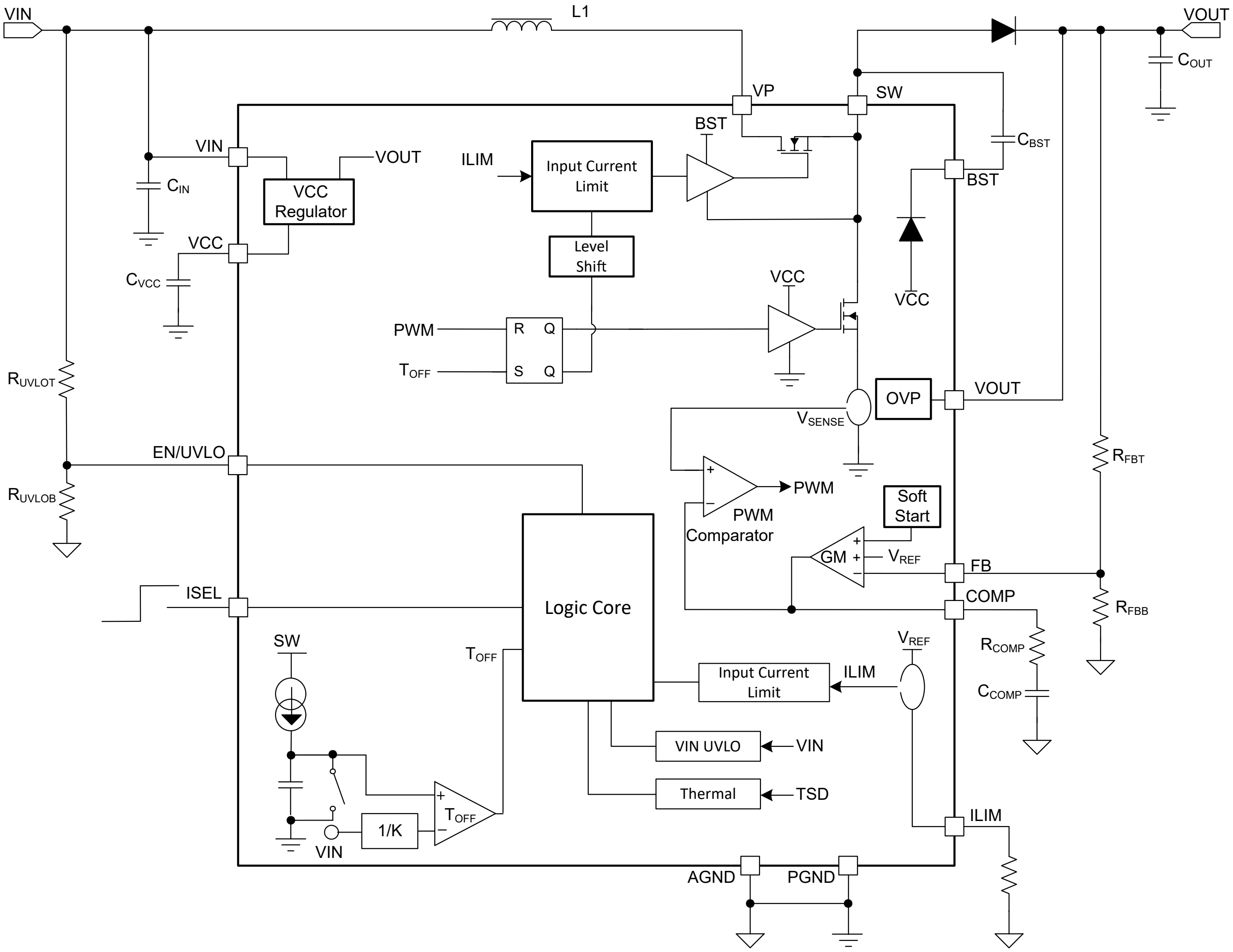
Figure 5-10. EN/UVLO rising Voltage vs Temperature

6 Detailed Description

6.1 Overview

The TPS61376 is a high voltage non-synchronous boost converter with input average current limit and load disconnect functions. The input average current limit threshold can be programmed through the ILIM pin from 0.1A to 3.0A. The isolation FET between the VP and SW pin will completely cut off the path between input and output when the device is disabled. The TPS61376 has a wide input voltage range from 2.9V to 23V and output voltage covers up to 25V. The TPS61376 implements the peak current mode with the adaptive off-time control topology. When the ISEL pin is logic high, the peak switching current limit is 4.5A(typ). When the ISEL pin is logic low, the peak switching current limit will change form 4.5A(typ) to 2.5A(typ). The device works in PWM mode at moderate to heavy load conditions. At the light load conditions, the device enters PFM mode to maintain high efficiency over the entire load current range. The TPS61376 also integrates robust protection features including output overvoltage protection, cycle-by-cycle overcurrent protection and thermal shutdown.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VCC Power Supply

The internal LDO of TPS61376 outputs a regulated voltage of 4.8V with 10-mA output current capability. When the input voltage at the VIN pin is below 5.25V, the internal LDO is powered by the VOUT pin, when the input voltage at the VIN pin is above 5.5V, the internal LDO is powered by the VIN pin. A ceramic capacitor is connected between the VCC pin and AGND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor should be above 1µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10V is recommended.

6.3.2 Enable and Programmable UVLO

The TPS61376 has a dual function enable and UVLO circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 2.8V and the EN/UVLO pin is pulled above rising threshold, the TPS61376 is enabled and starts switching. The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input under-voltage lockout with hysteresis. A hysteresis current I_{UVLO_HYS} is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of input voltage noise. By using resistor divider as shown in Figure 6-1 , the turn on threshold can be calculated by using Equation 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- V_{UVLO} is the UVLO threshold of 0.813V at the EN/UVLO pin

The hysteresis between the UVLO turn on threshold and turn off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by Equation 2

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

where

- I_{UVLO} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}

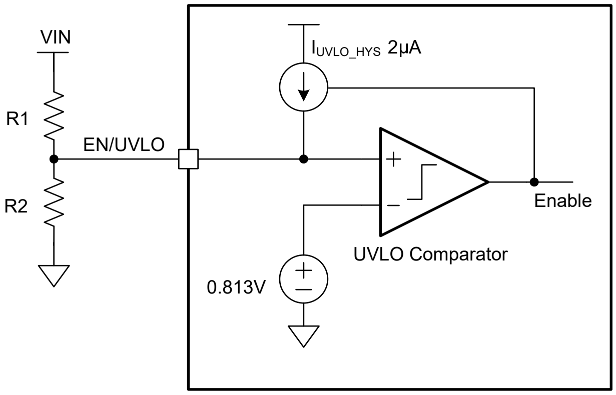


Figure 6-1. Programmable UVLO with Resistor Divider at EN/UVLO Pin

6.3.3 Soft Start and Inrush Current Control During Start-Up

The TPS61376 has a soft-start and input average current limit function to prevent high inrush current during start-up. When the EN pin is pulled high, the TPS61376 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to the reference voltage within typical 4ms. During start-up when V_{IN} is higher than V_{OUT}, the ISO FET between VP and SW pin will limit the current across the inductor. This current will increase linearly as the V_{IN} and V_{OUT} delta decreases. When V_{OUT} is higher than V_{IN}, TPS61376 will regulate the input average current programmed via ILIM pin.

6.3.4 Switching Frequency

The TPS61376 uses adaptive constant off-time peak current control topology to regulate the output voltage. In moderate to heavy load conditions, the TPS61376 works in pulse width modulation (PWM) mode. The switching frequency in PWM mode is 1.2MHz. At light load conditions, the TPS61376 works in power-save mode with pulse frequency modulation (PFM). The PFM mode brings high efficiency at the light load.

6.3.5 Adjustable input average Current Limit

The TPS61376 has integrated input average current limit function internally, the average current limit can be set by a resistor from the ILIM pin to AGND. The current limit can be programmed from 0.1A to 3.0A. It is recommended to set ISEL pin logic low when setting input average current limit below 750mA. With ISEL pin logic low, TPS61376 will scale the ISO FET to increase the on resistance to improve the input average current accuracy. Meanwhile with ISEL pin logic low, the peak switching current limit will change from 4.5A(typ) to 2.5A(typ). The relationship between the input average current limit and the resistor is shown in Equation 3 and Equation 4.

$$I_{LIM} = \frac{43.2K}{R_{LIM}} \text{ with ISEL pin logic high} \tag{3}$$

$$I_{LIM} = \frac{10.8K}{R_{LIM}} \text{ with ISEL pin logic low} \tag{4}$$

where

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{LIM} is the input average current limit.

For instance, the input average current limit is 3.0A if the R_{LIM} is 14.4kΩ with ISEL pin logic high. The ILIM pin cannot be left floating or connected to VCC.

6.3.6 Shut Down and Load Disconnect

When the input voltage is below the UVLO threshold or the EN pin is pulled low, The TPS61376 is in shutdown mode and all the functions are disabled. The TPS61376 integrates a load disconnect function, the ISO FET between the VP and SW pin will completely cut off the path between input and output when the device is disabled.

6.3.7 Overvoltage Protection

If the output voltage at the VOUT pin is detected above 27.5V (typ), the TPS61376 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

6.3.8 Output Short Protection

The TPS61376 has output short protection. If the output voltage falls below $V_{IN} \times 1.05 + 0.2V$ (typical), or even to ground during a fault condition, the device enters into down mode. During this mode, the VP pin is regulated to approximately 3.5V above V_{IN} to control the current across the inductor at a relatively low level and protect the device from damage. When the short condition disappears and the V_{OUT} rises above $V_{IN} \times 1.05 + 0.2V$ (typical), the device automatically returns to normal work mode.

6.3.9 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

6.4 Device Functional Modes

6.4.1 PWM Mode

The TPS61376 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate to heavy load condition before trigger the input average current limit. Based on the VIN to VOUT ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch, shown in Functional Block Diagram, is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, then it turns off the low-side N-MOSFET switch and the inductor current goes through the schottky diode. Because the output voltage is higher than the input voltage, the inductor current decreases. Until the calculated off-time is reached the low-side switch turns on again and the switching cycle is repeated.

6.4.2 Auto PFM Mode

The TPS61376 provides a seamless transition from PWM to PFM operation with smooth on-time/off-time (SOO) mode and enables automatic pulse-skipping mode that provides excellent efficiency over a wide load range. As load current decreasing or VIN rising, the output of the internal error amplifier decreases to lower the inductor peak current, delivering less power to the load. When the output of the error amplifier goes down and reaches a threshold of about 350-mA peak current, the output of the error amplifier is clamped at this value and does not decrease any more, the TPS61376 extends its off-time of the switching period to deliver less energy to the output and regulate the output voltage to the target.

With SOO mode, the TPS61376 keeps the output voltage equal to the setting voltage in PFM mode. In addition, the output voltage ripple is much smaller at light load due to low peak current. Refer to Figure 6-2.

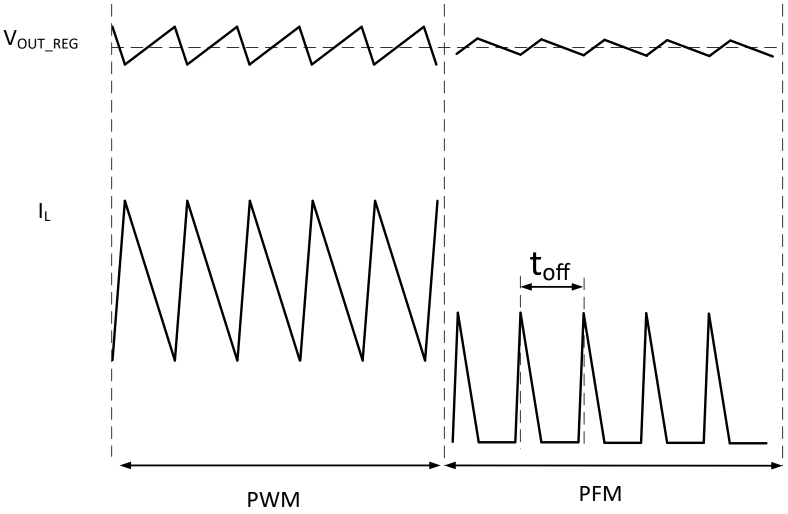


Figure 6-2. Auto PFM Mode Diagram

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS61376 is designed for output voltage up to 25V with up to 3A input average current limit. The TPS61376 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate to heavy load condition. In light load condition, the converter operates in PFM mode. The PFM mode brings high efficiency over the entire load range. The converter uses the adaptive constant off-time peak current control scheme, which provides excellent line and load transient response with minimal output capacitance. The TPS61376 can work with different inductor and output capacitor combinations by adjusting external loop compensation.

7.2 Typical Application

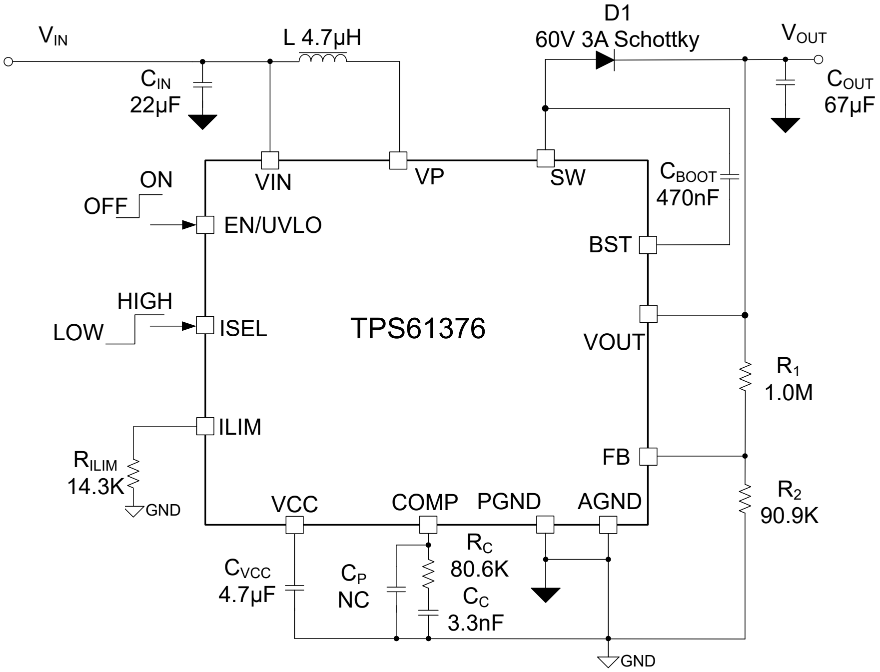


Figure 7-1. TPS61376 3.3V to 8.4V V_{IN} ;12V V_{OUT} 0.5A Output Converter

7.2.1 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3.3V to 8.4V
Output voltage	12V
Output voltage ripple	100mV peak to peak
Output current rating	0.5A

7.2.2 Detailed Design Procedure

7.2.2.1 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in the Figure 7-1 circuit diagram). For the best accuracy, R2 should be smaller than 500kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 to lower value increases the immunity against noise injection. Changing R2 to higher values reduces the quiescent current to achieve higher efficiency at light load.

The value of R1 is then calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \tag{5}$$

7.2.2.2 Inductor Selection

The selection of the inductor affects the steady state of the power supply operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. The three most important specifications to the performance of the inductor are the inductance value, DC resistance, and saturation current.

The TPS61376 is designed to work with inductor values between 2.2µH and 10µH. A 2.2µH inductor is typically available in a smaller or lower-profile package, while a 10µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a bigger inductance can maximize the output current capability of the converter.

Inductor values can have ±20% or even ±30% tolerance with 0A bias current. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A bias current, depending on how the inductor vendor defines saturation current. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than boost converter peak current under all operating conditions.

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. Follow Equation 6 to Equation 8 to calculate the average, peak and ripple current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 6.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{6}$$

where

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 7.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \tag{7}$$

where

- I_{PP} is the inductor peak-to-peak ripple.

- L is the inductor value.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with Equation 8.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \tag{8}$$

With ISEL pin logic high, the peak switching current limit is 4.5A(typ), when the ISEL pin logic low, the peak switching current limit will change from 4.5A(typ) to 2.5A(typ). It is important that the peak current does not exceed the inductor saturation current.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. Usually, a data sheet of an inductor does not provide the core loss information. If needed, consult the inductor vendor for detailed information. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. The table below lists some recommended inductors.

Table 7-2. Recommended Inductors

PART NUMBER	L (µH)	DCR TYP (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR(1)
XGL5050-222ME	2.2	6.8	10.7	5.28 x 5.48 x 5.1	Coilcraft
XGL5050-472ME	4.7	13.9	7.0	5.28 x 5.48 x 5.1	Coilcraft
XGL6060-103ME	10	18.5	7.3	6.51 x 6.71 x 6.1	Coilcraft
XGL4020-222ME	2.2	19.5	6.2	4.0 x 4.0 x 2.1	Coilcraft
XGL4020-472ME	4.7	43	4.1	4.0 x 4.0 x 2.1	Coilcraft
XGL4020-822ME	8.2	71	3.2	4.0 x 4.0 x 2.1	Coilcraft

(1) See the *Third-party Products Disclaimer*.

7.2.2.3 Bootstrap Capacitor Selection

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the ISO FET device gate during the turn on of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.47µF to 1µF. C_{BST} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.47µF was selected for this design example.

7.2.2.4 Input Capacitor Selection

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, must be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

7.2.2.5 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 9:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \tag{9}$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by Equation 10:

$$\Delta V_{ESR} = I_{Lpeak} \times R_{ESR} \tag{10}$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 11:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \tag{11}$$

where

- ΔI_{STEP} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the respective rated voltage. Therefore, enough margins on the voltage rating must be considered to ensure adequate capacitance at the required output voltage.

7.2.2.6 Diode Selection

A Schottky diode is the preferred type for D1 due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current.

7.2.2.7 Loop Stability

The TPS61376 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R_C, and ceramic capacitors C_C and C_P, is connected to the COMP pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by Equation 12.

$$G_{PS}(S)=K_{COMP}\times\frac{R_O\times(1\text{-}D)}{2}\times\frac{\left(1+\frac{S}{2\pi f_{ESRZ}}\right)\times\left(1-\frac{S}{2\pi f_{RHPZ}}\right)}{1+\frac{S}{2\pi f_P}} \tag{12}$$

where

- D is the switching duty cycle.
- R_O is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current / comp voltage), which is 6.5A/V.

$$f_P=\frac{2}{2\pi\times R_O\times C_O} \tag{13}$$

where

- C_O is effective output capacitance.

$$f_{ESRZ}=\frac{1}{2\pi\times R_{ESR}\times C_O} \tag{14}$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ}=\frac{R_O\times(1-D)^2}{2\pi\times L} \tag{15}$$

The COMP pin is the output of the internal transconductance amplifier. Equation 16 shows the small signal transfer function of compensation network.

$$Gc(S)=\frac{G_{EA}\times R_{EA}\times V_{REF}}{V_{OUT}}\times\frac{\left(1+\frac{S}{2\times\pi\times f_{COMZ}}\right)}{\left(1+\frac{S}{2\times\pi\times f_{COMP1}}\right)\left(1+\frac{S}{2\times\pi\times f_{COMP2}}\right)} \tag{16}$$

where

- G_{EA} is the transconductance of the amplifier, which is 240uS.
- R_{EA} is the output resistance of the amplifier, which is 100MΩ.
- V_{REF} is the reference voltage at the FB pin.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R_C, C_C, and C_P (in Figure 7-1) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1\text{-}D) \times V_{REF} \times G_{EA} \times K_{COMP}} \tag{17}$$

where

- f_C is the selected crossover frequency.

The value of C_C can be set by Equation 18.

$$C_C = \frac{R_O \times C_O}{2R_C} \tag{18}$$

The value of C_P can be set by Equation 19.

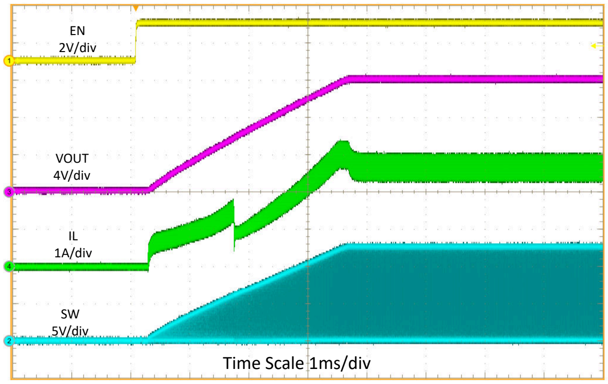
$$C_P = \frac{R_{ESR} \times C_O}{R_C} \tag{19}$$

If the calculated value of C_P is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

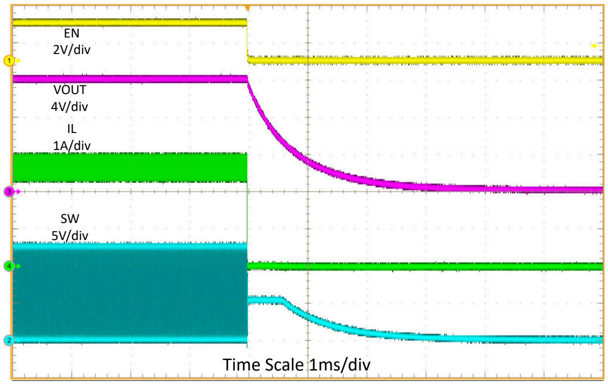
7.2.3 Application Curves

T_A = 25°C, C_{OUT} = 67µF, ICL = 3.0A, unless otherwise noted.



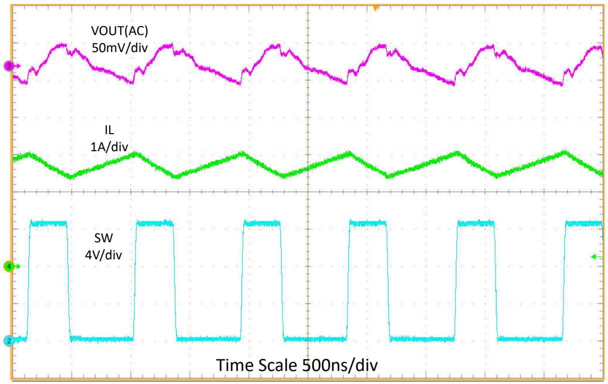
V_{IN} = 5V V_{OUT} = 12V R_{LOAD} = 12Ω

Figure 7-2. Start-Up Waveforms



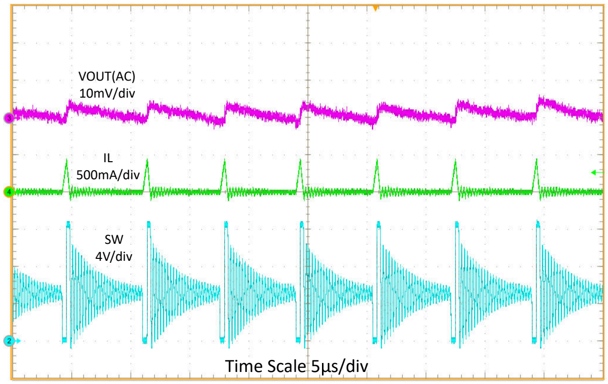
V_{IN} = 5V V_{OUT} = 12V R_{LOAD} = 12Ω

Figure 7-3. Shutdown Waveforms



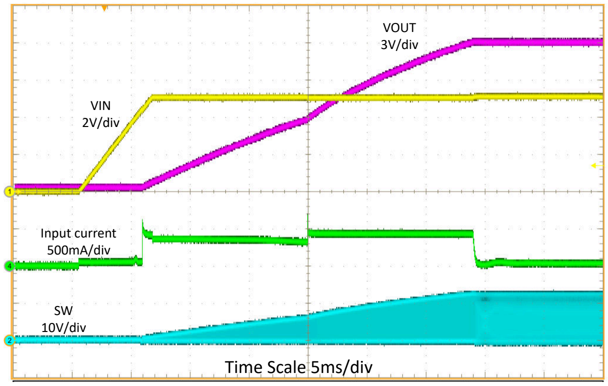
V_{IN} = 5V V_{OUT} = 12V I_{OUT} = 1.0A

Figure 7-4. Switching Waveforms in CCM



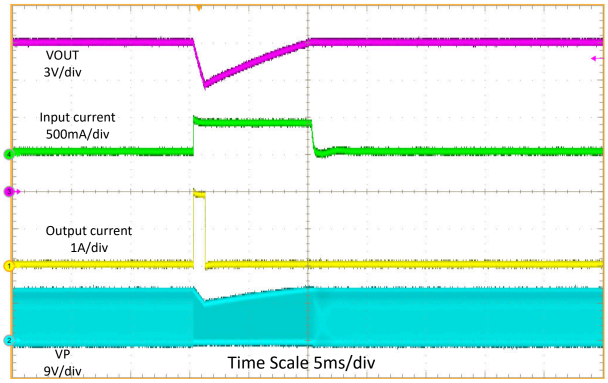
V_{IN} = 5V V_{OUT} = 12V I_{OUT} = 50mA

Figure 7-5. Switching Waveforms in 50mA Load



V_{IN} = 5.0V V_{OUT} = 12V I_{OUT} = 0A, C_{OUT} = 540µF

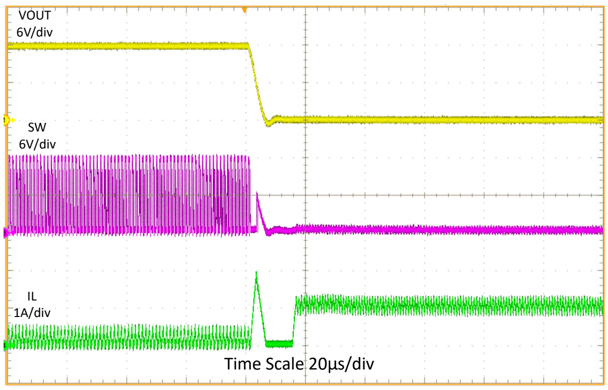
Figure 7-6. Start-Up with ICL 500mA



V_{IN} = 5.0V V_{OUT} = 12V Load = 0A to 2A, C_{OUT} = 540µF

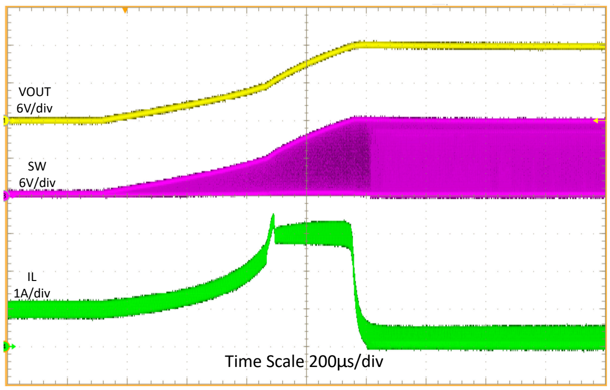
Figure 7-7. 2A Load Pulse with ICL 500mA

7.2.3 Application Curves (continued)



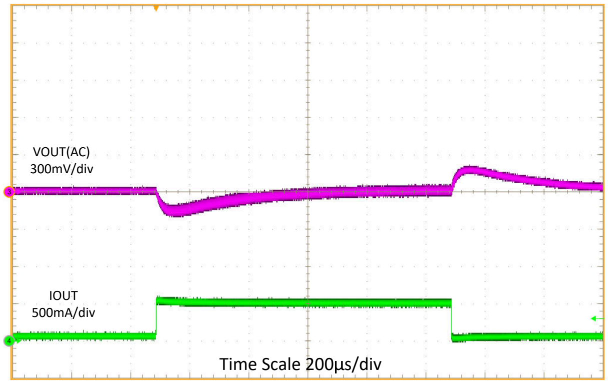
V_{IN} = 3.3V V_{OUT} = 12V

Figure 7-8. Short Circuit Protection (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 50mA, R_{LIM} = 14.3kΩ, ISEL = high)



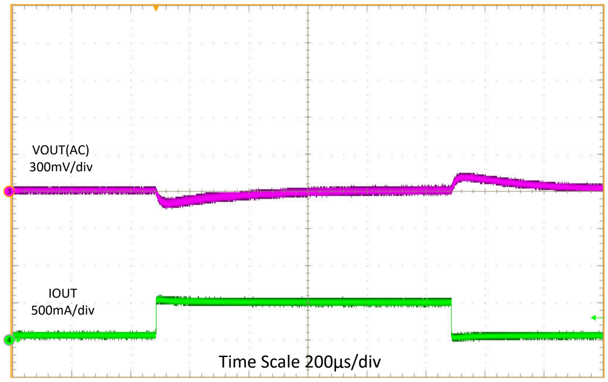
V_{IN} = 3.3V V_{OUT} = 12V

Figure 7-9. Short Circuit Recovery (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 50mA, R_{LIM} = 14.3kΩ, ISEL = high)



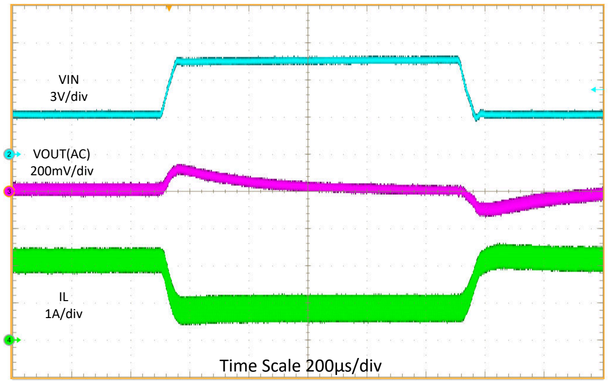
V_{IN} = 3.3V V_{OUT} = 12V

Figure 7-10. Load Transient (I_{OUT} = 0.1A to 0.5A)



V_{IN} = 8.4V V_{OUT} = 12V

Figure 7-11. Load Transient (I_{OUT} = 0.1A to 0.5A)



V_{OUT} = 12V I_{OUT} = 0.5A

Figure 7-12. Line Transient (V_{IN} = 3.3V to 8.4V)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9V to 23V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47μF.

7.4 Layout

7.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high current, layout is an important design step. If the layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

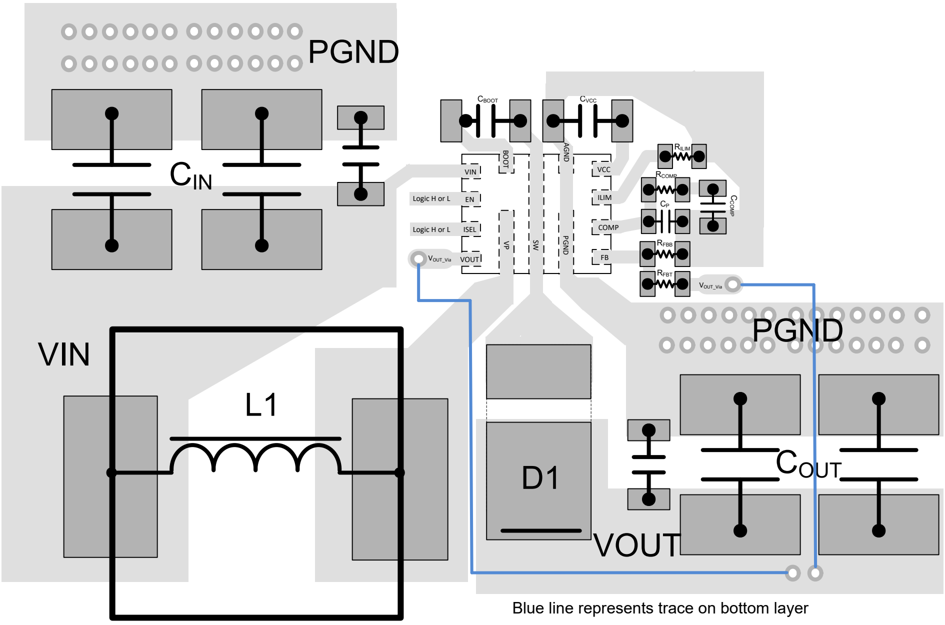
The input capacitor needs to be close to the VIN pin and PGND pin in order to reduce the I_{input} supply ripple.

The power paths of SW, D1,output capacitor and PGND should be as small as possible, in order to reduce parasitic inductance.

The layout should also be done with well consideration of the thermal as this is a high power density device. The VP, SW, VOUT and PGND pins that improves the thermal capabilities of the package should be soldered with the large polygon, using thermal vias underneath the SW pin could improve thermal performance.

7.4.2 Layout Example

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.



Blue line represents trace on bottom layer

Figure 7-13. Layout Example

7.4.2.1 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 20.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{20}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS61376 comes in a thermally-enhanced VQFN package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2022) to Revision B (August 2023)	Page
• Updated Output Short Protection section	11

Changes from Revision * (January 2022) to Revision A (September 2022)	Page
• Changed device status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61376RYHR	Active	Production	VQFN-HR (RYH) | 13	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1376
TPS61376RYHR.A	Active	Production	VQFN-HR (RYH) | 13	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1376

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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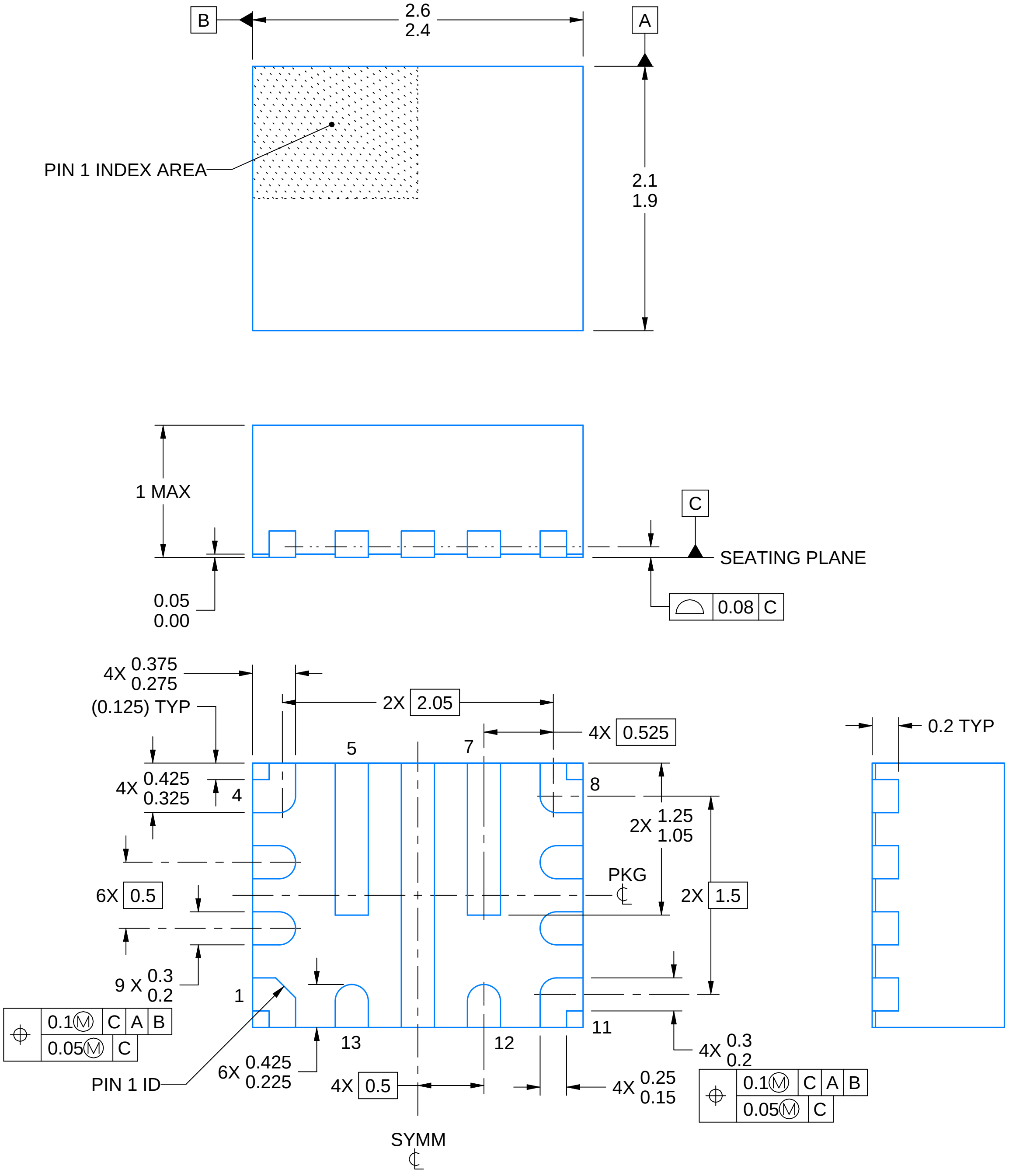

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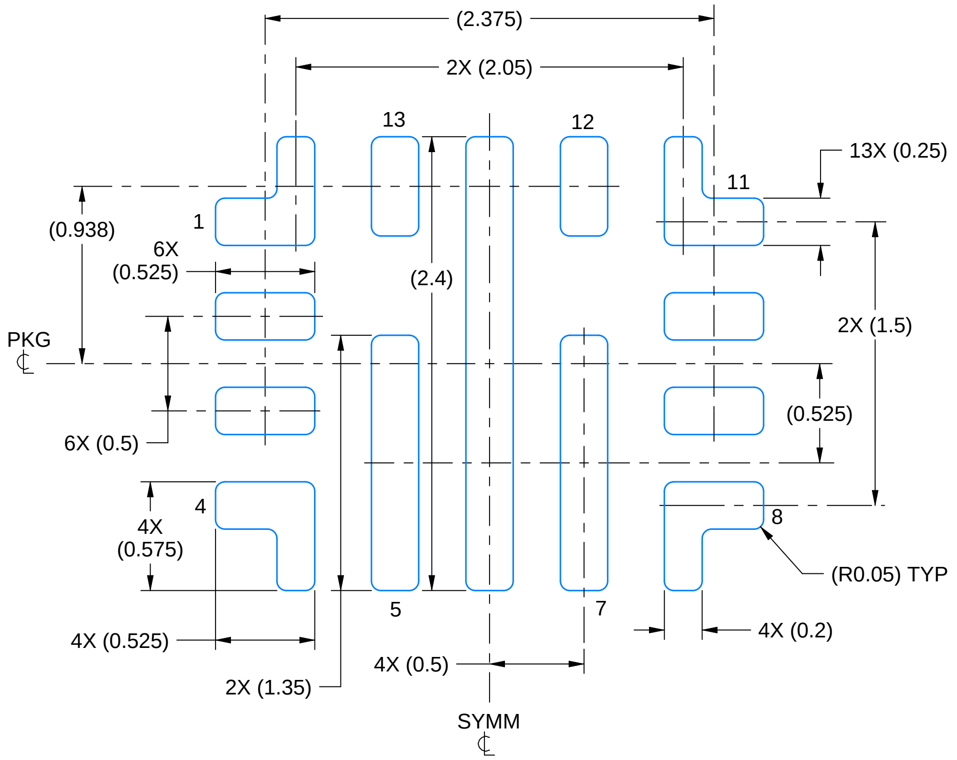
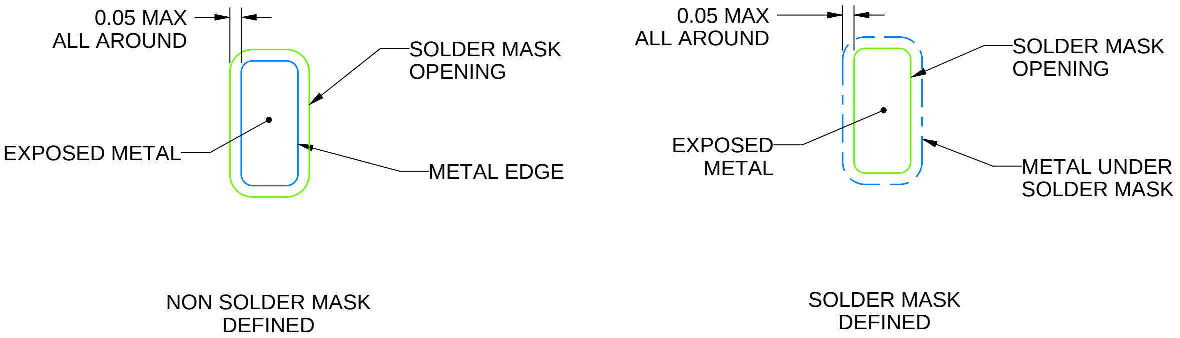
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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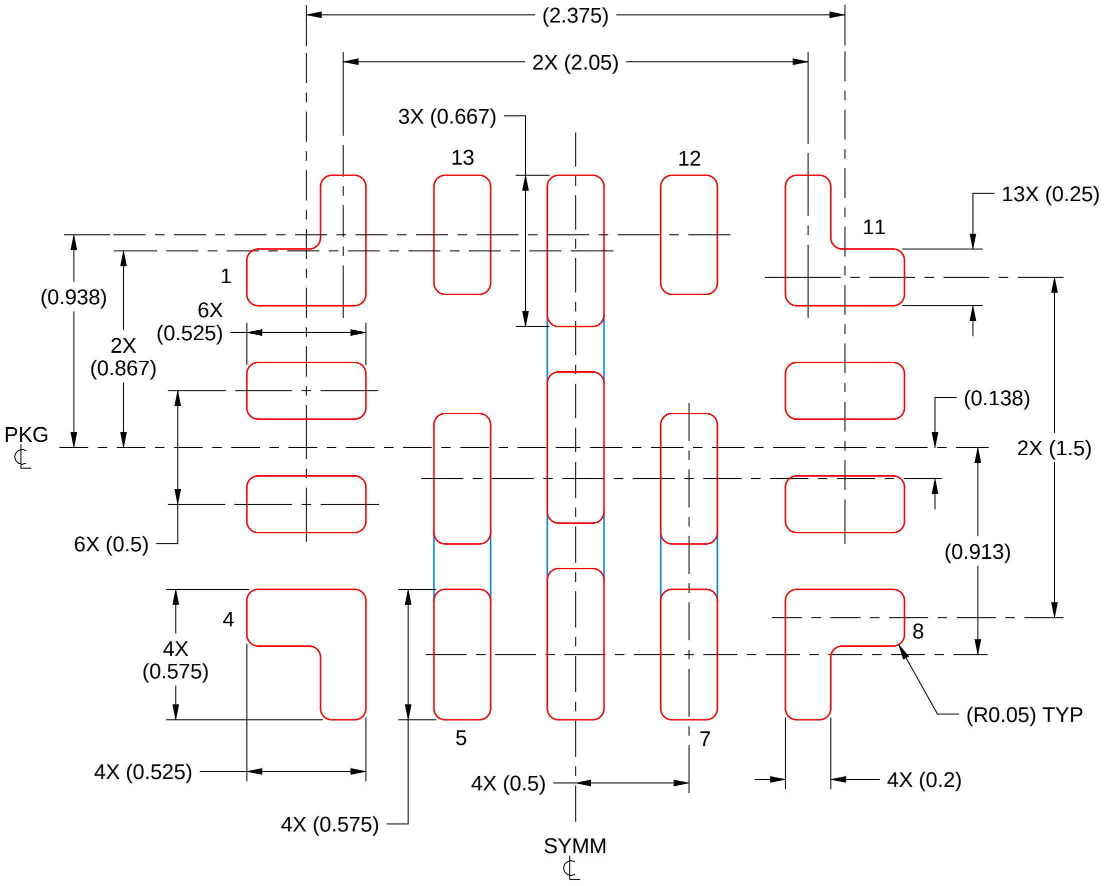
NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PIN 5 & 7 SOLDER COVERAGE = 85%
PIN 6 SOLDER COVERAGE = 83%
SCALE : 25X

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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