

The μ A733M is obsolete
and no longer supplied.

μ A733C, μ A733M DIFFERENTIAL VIDEO AMPLIFIERS

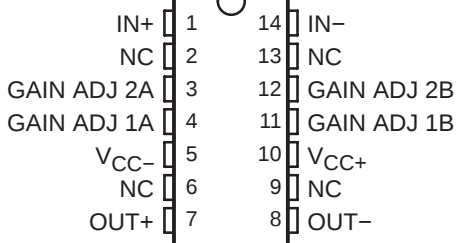
SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

- 200-MHz Bandwidth
- 250-k Ω Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required

μ A733C . . . D, N, OR NS PACKAGE

μ A733M . . . J PACKAGE

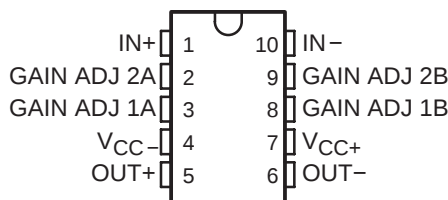
(TOP VIEW)



NC — No internal connection

μ A733M . . . U PACKAGE

(TOP VIEW)



description/ordering information

The μ A733 is a monolithic two-stage video amplifier with differential inputs and differential outputs. Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10 V/V, 100 V/V, or 400 V/V may be selected without external components, or amplification may be adjusted from 10 V/V to 400 V/V by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The μ A733C is characterized for operation from 0°C to 70°C; the μ A733M is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	P-DIP (N)	Tube of 25	UA733CN	UA733CN
	SOIC (D)	Tube of 50	UA733CD	UA733C
		Reel of 2500	UA733CDR	
	SOP (NS)	Reel of 2000	UA733CNSR	UA733

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

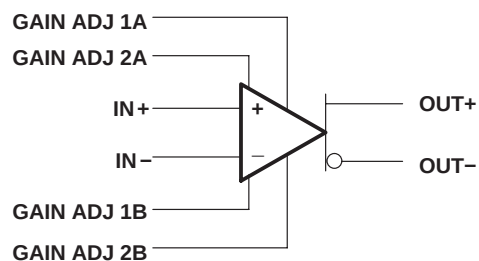
Copyright © 2004, Texas Instruments Incorporated

μA733C, μA733M **DIFFERENTIAL VIDEO AMPLIFIERS**

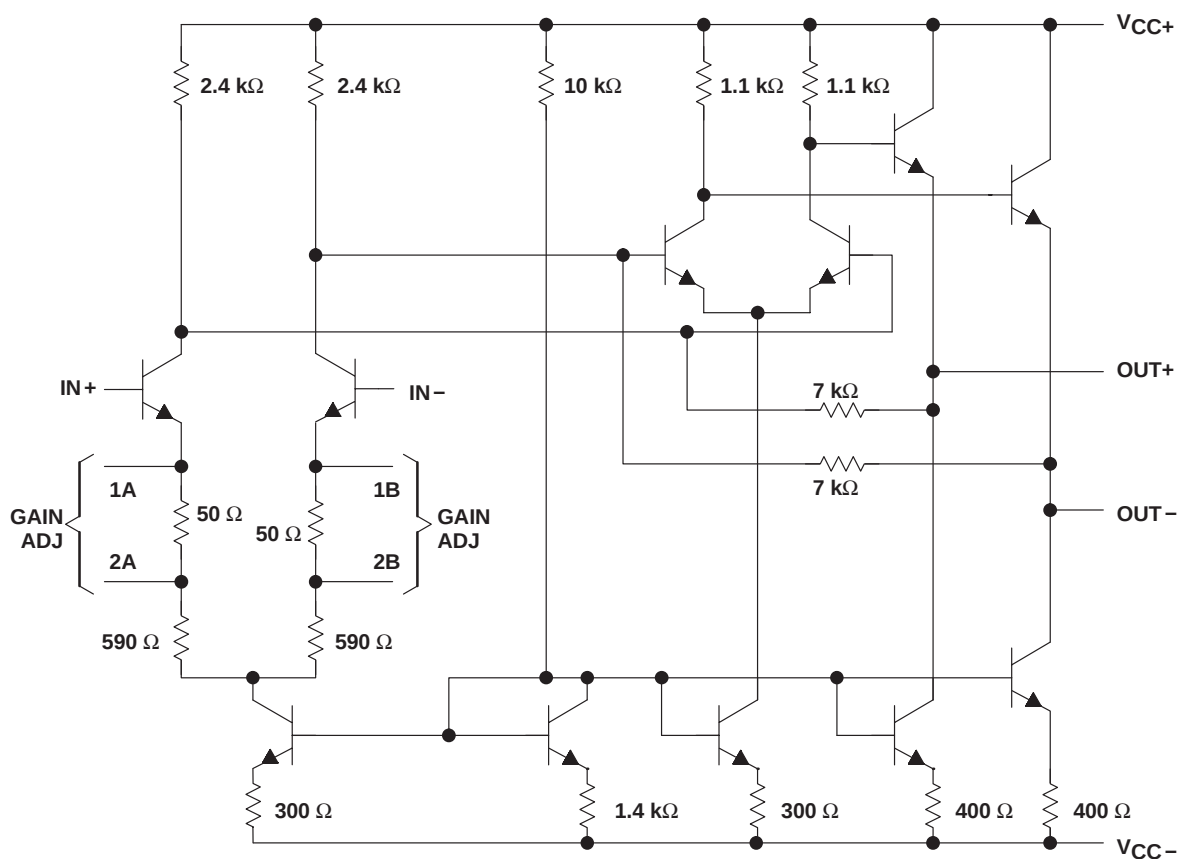
SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

The μA733M is obsolete
 and no longer supplied.

symbol



schematic



Component values shown are nominal.

The μ A733M is obsolete
and no longer supplied.

μ A733C, μ A733M DIFFERENTIAL VIDEO AMPLIFIERS

SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

	μ A733C	μ A733M	UNIT
Supply voltage V_{CC+} (see Note 1)	8	8	V
Supply voltage V_{CC-} (see Note 1)	– 8	– 8	V
Differential input voltage	± 5	± 5	V
Common-mode input voltage	± 6	± 6	V
Output current	10	10	mA
Continuous total power dissipation	See Dissipation Rating Table		
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	D package	86	$^{\circ}\text{C/W}$
	N package	80	
	NS package	76	
Maximum junction temperature, T_J	150		$^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package	300	$^{\circ}\text{C}$
Storage temperature range, T_{Stg}	– 65 to 150	– 65 to 150	$^{\circ}\text{C}$

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 125^{\circ}\text{C}$ POWER RATING
J (μ A733M)	500 mW	11.0 mW/ $^{\circ}\text{C}$	104°C	500 mW	269 mW



μA733C, μA733M **DIFFERENTIAL VIDEO AMPLIFIERS**

The μA733M is obsolete
and no longer supplied.

SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

electrical characteristics, $V_{CC\pm} = \pm 6\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		FIGURE	TEST CONDITIONS	GAIN OPTION†	μA733C			μA733M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A _{VD}	Large-signal differential voltage amplification	1	V _{OD} = 1 V	1	250	400	600	300	400	500	V/V
				2	80	100	120	90	100	110	
				3	8	10	12	9	10	11	
BW	Bandwidth	2	R _S = 50 Ω	1	50			50			MHz
				2	90			90			
				3	200			200			
I _{IO}	Input offset current			Any	0.4 5			0.4 3			μA
I _{IB}	Input bias current			Any	9 30			9 20			μA
V _{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V _{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V _{OO}	Output offset voltage	1		1	0.6 1.5			0.6 1.5			V
				2 & 3	0.35 1.5			0.35 1			
V _{OPP}	Maximum peak- to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r _i	Input resistance	3	V _{OD} ≤ 1 V	1	4			4			kΩ
				2	10	24		20	24		
				3	250			250			
r _o	Output resistance				20			20			Ω
C _i	Input capacitance	3	V _{OD} ≤ 1 V	2	2			2			pF
CMRR	Common-mode rejection ration	4	V _{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V _{IC} = ±1 V, f = 5 MHz	2	70			70			
k _{SVR}	Supply voltage rejection ratio (ΔV _{CC} /ΔV _{IO})	1	ΔV _{CC} ± = ±0.5 V	2	50	70		50	70		dB
V _n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any	12			12			μV
t _{pd}	Propagation delay time	2	R _S = 50 Ω, Output voltage step = 1 V	1	7.5			7.5			ns
				2	6.0 10			6.0 10			
				3	3.6			3.6			
t _r	Rise time	2	R _S = 50 Ω, Output voltage step = 1 V	1	10.5			10.5			ns
				2	4.5 12			4.5 10			
				3	2.5			2.5			
I _{sink(max)}	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I _{CC}	Supply current		No load, No signal	Any	16 24			16 24			mA

† The gain option is selected as follows:

Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.

Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.

Gain Option 3: All four gain-adjust pins are open.



The μ A733M is obsolete
and no longer supplied.

μ A733C, μ A733M DIFFERENTIAL VIDEO AMPLIFIERS

SLFS027B – NOVEMBER 1970 – REVISED MAY 2004

electrical characteristics, $V_{CC\pm} = \pm 6$ V, $T_A = 0^\circ\text{C}$ to 70°C for μ A733C, -55°C to 125°C for μ A733M

PARAMETER	FIGURE	TEST CONDITIONS	GAIN OPTION†	μ A733C		μ A733M		UNIT
				MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	$V_{OD} = 1$ V	1	250 600	200 600		V/V
				2	80 120	80 120		
				3	8 12	8 12		
I_{IO}	Input offset current		Any		6		5	μ A
I_{IB}	Input bias current		Any		40		40	μ A
V_{ICR}	Common-mode input voltage range	1		Any	± 1	± 1		V
V_{OO}	Output offset voltage	1	1		1.5		1.5	V
			2 & 3		1.5		1.2	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	Any		2.8		2.5	V
r_i	Input resistance	3	$V_{OD} \leq 1$ V	2	8		8	k Ω
CMRR	Common-mode rejection ratio	4	$V_{IC} = +1$ V, $f \leq 100$ kHz	2	50		50	dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	$\Delta V_{CC\pm} = \pm 0.5$ V	2	50		50	dB
$I_{sink(max)}$	Maximum output sink current			Any	2.5		2.2	mA
I_{CC}	Supply current		No load, No signal	Any		27		27 mA

† The gain option is selected as follows:

Gain Option 1: Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.

Gain Option 2: Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.

Gain Option 3: All four gain-adjust pins are open.



PARAMETER MEASUREMENT INFORMATION

test circuits

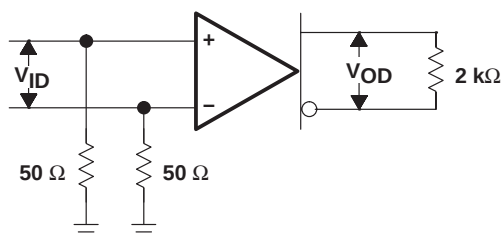


Figure 1

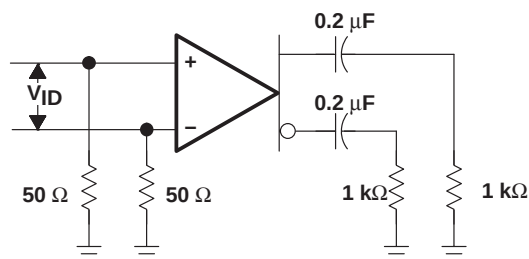


Figure 2

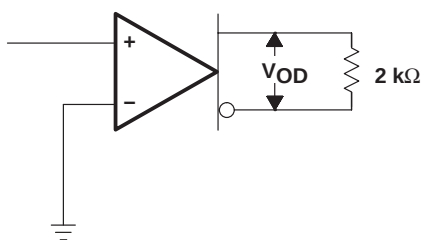


Figure 3

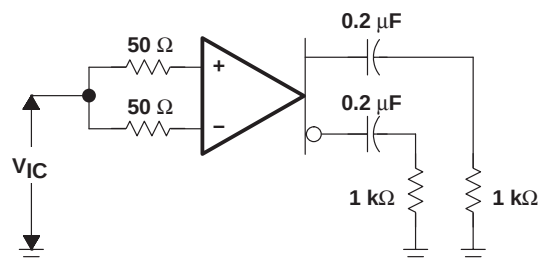


Figure 4

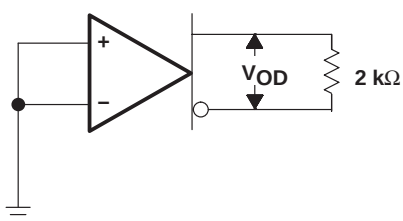
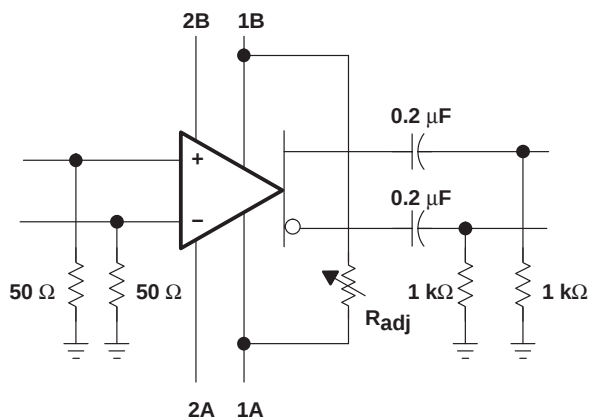


Figure 5



VOLTAGE AMPLIFICATION ADJUSTMENT

Figure 6

TYPICAL CHARACTERISTICS

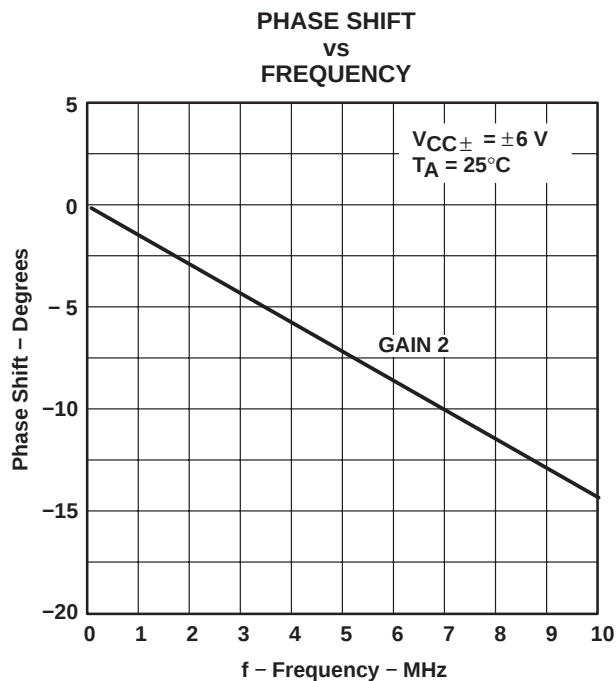


Figure 7

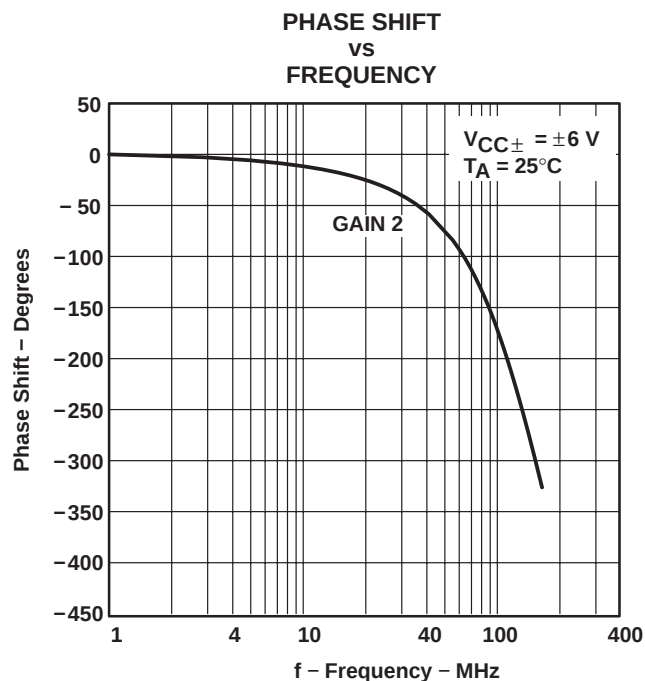


Figure 8

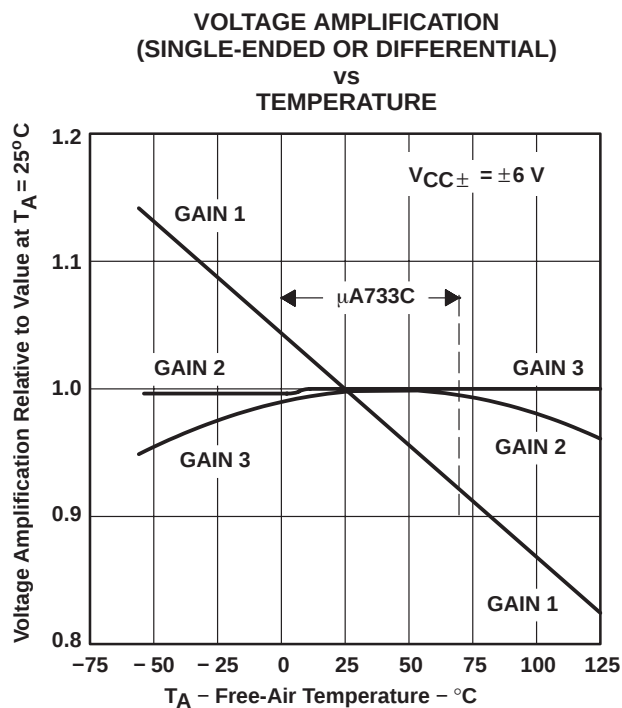


Figure 9

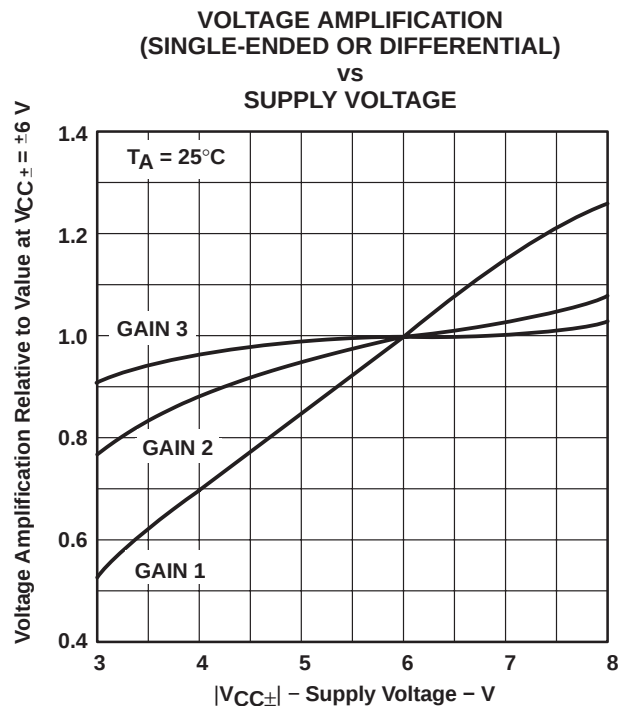


Figure 10

TYPICAL CHARACTERISTICS

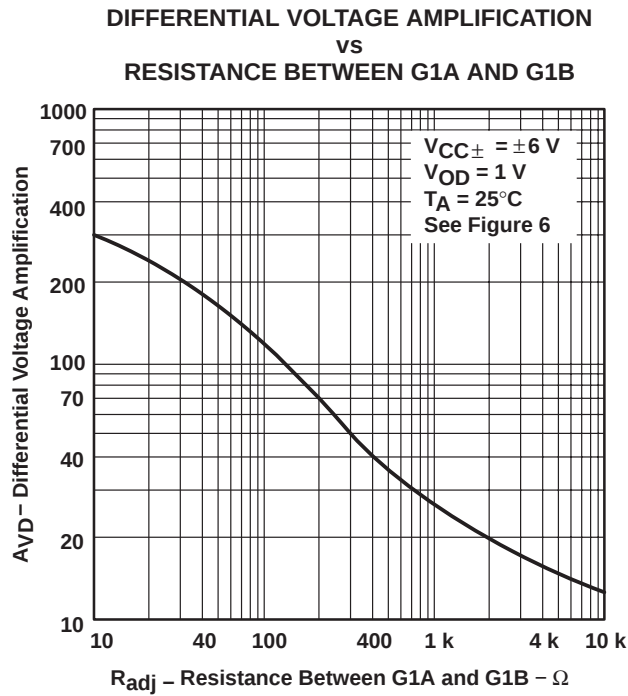


Figure 11

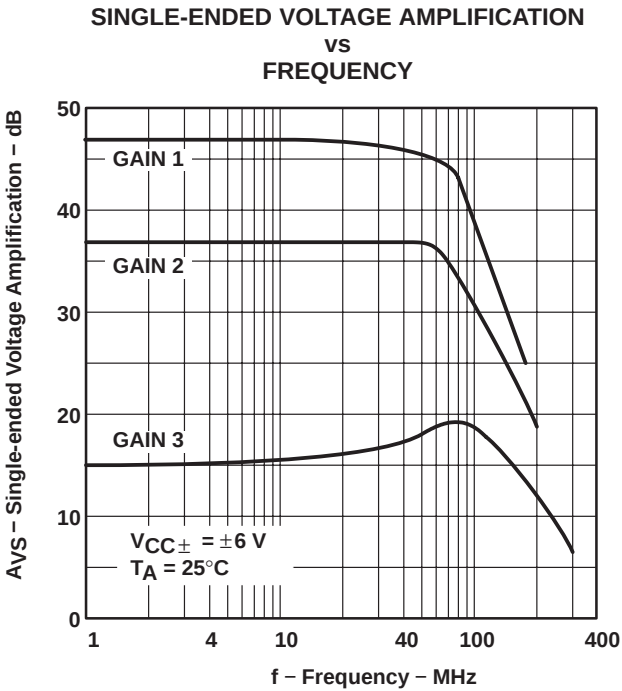


Figure 12

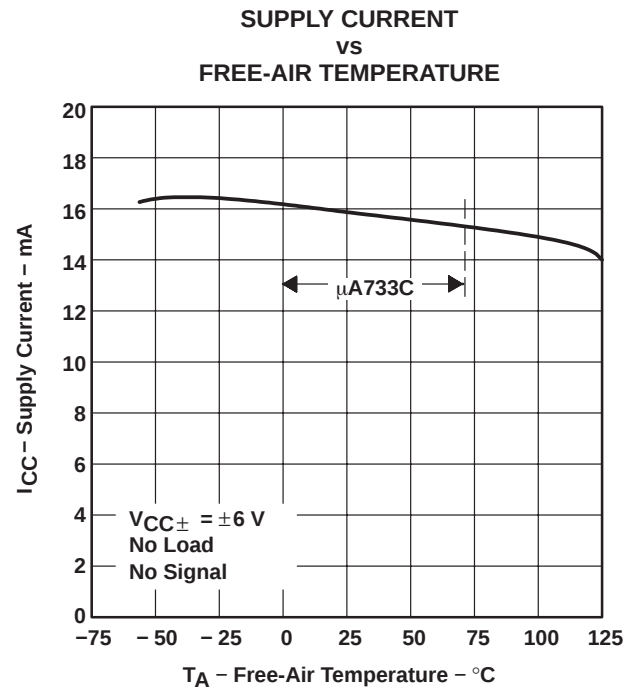


Figure 13

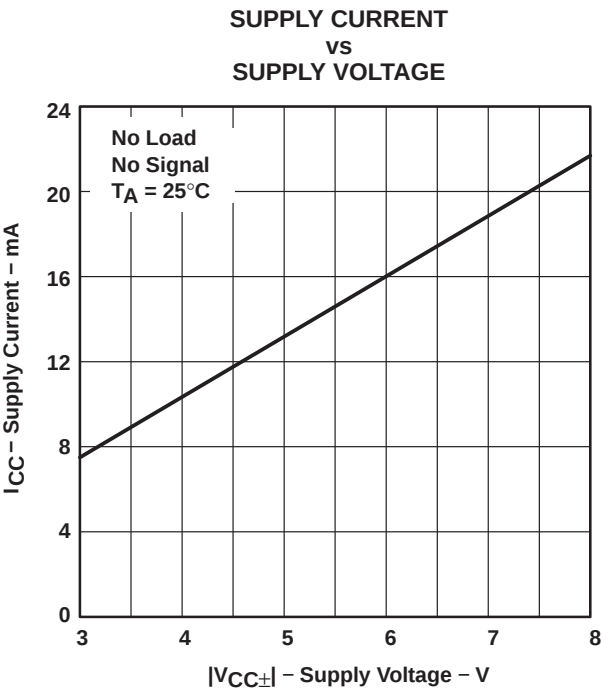


Figure 14

TYPICAL CHARACTERISTICS

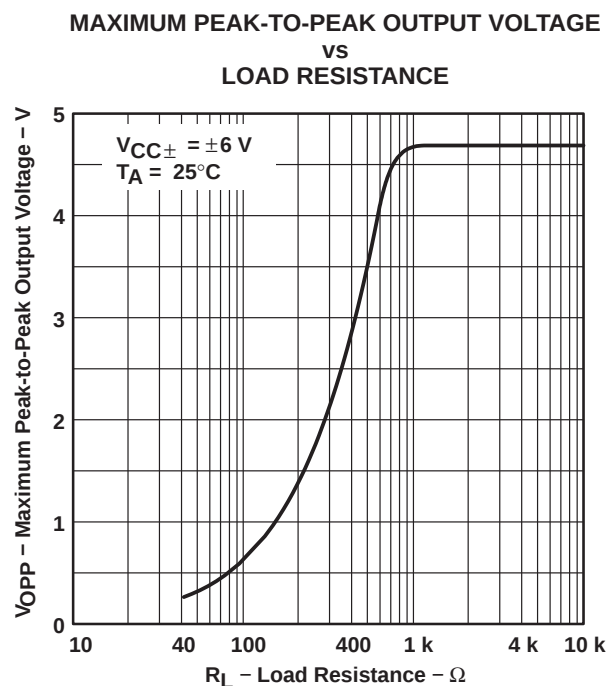


Figure 15

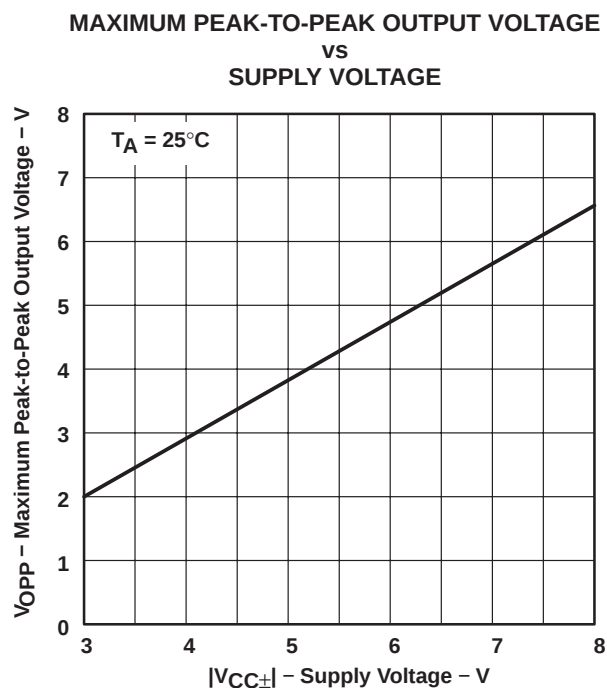


Figure 16

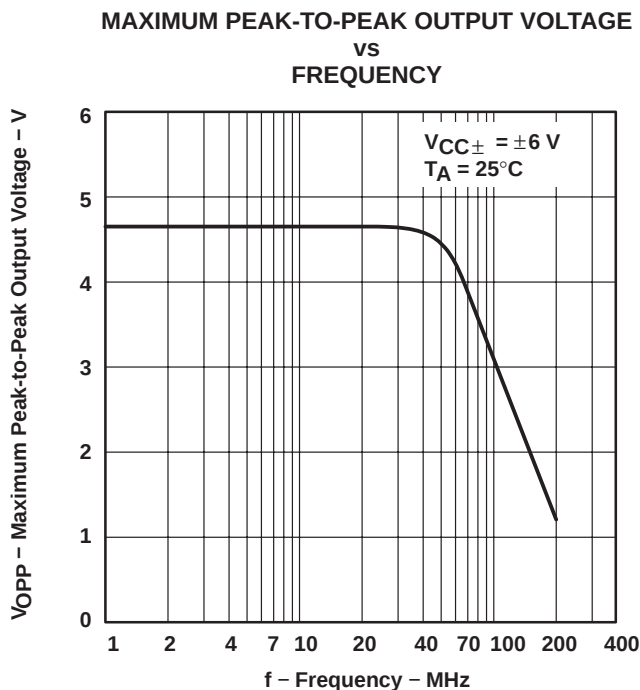


Figure 17

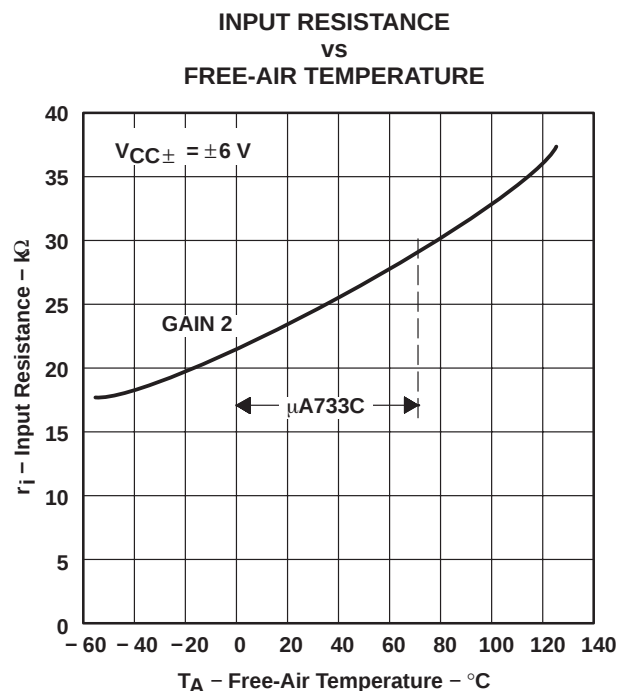


Figure 18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA733CD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C
UA733CD.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C
UA733CDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C
UA733CDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733C
UA733CN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA733CN
UA733CN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA733CN
UA733CNSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733
UA733CNSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA733

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

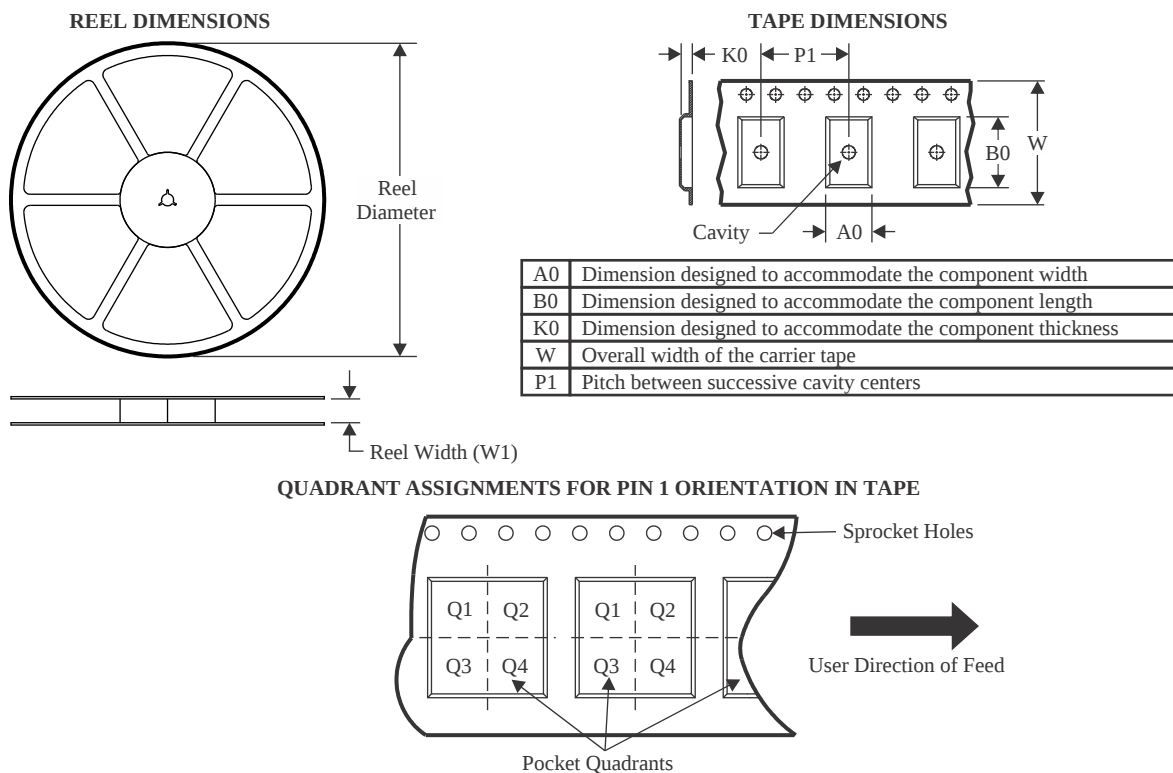
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

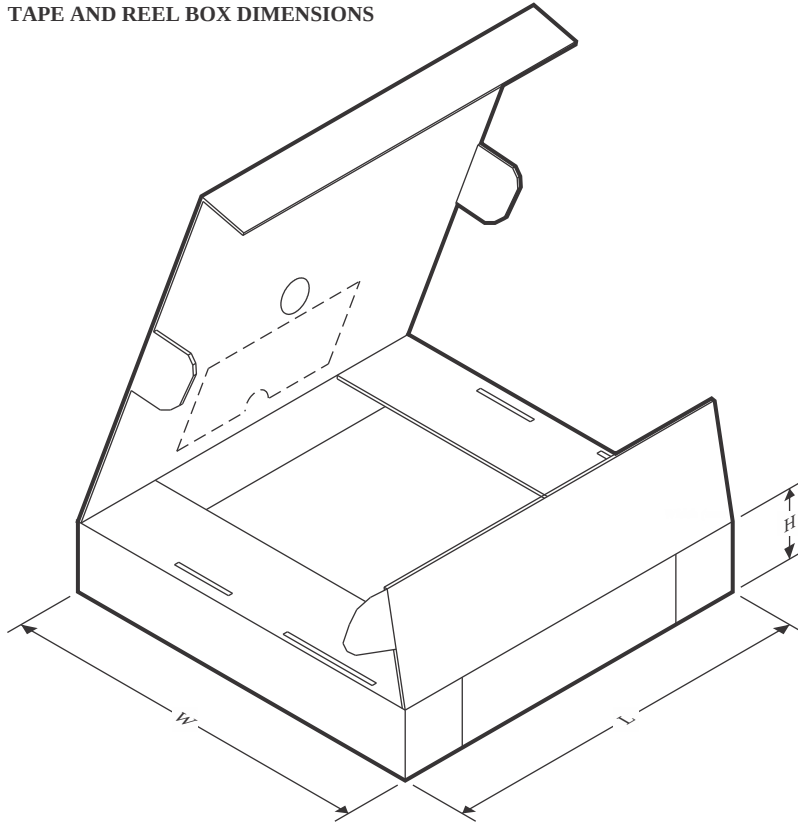
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA733CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UA733CNSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA733CDR	SOIC	D	14	2500	356.0	356.0	35.0
UA733CNSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE

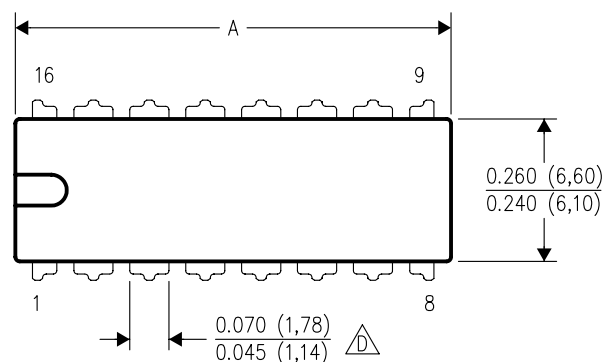

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UA733CD	D	SOIC	14	50	506.6	8	3940	4.32
UA733CD.A	D	SOIC	14	50	506.6	8	3940	4.32
UA733CN	N	PDIP	14	25	506	13.97	11230	4.32
UA733CN.A	N	PDIP	14	25	506	13.97	11230	4.32

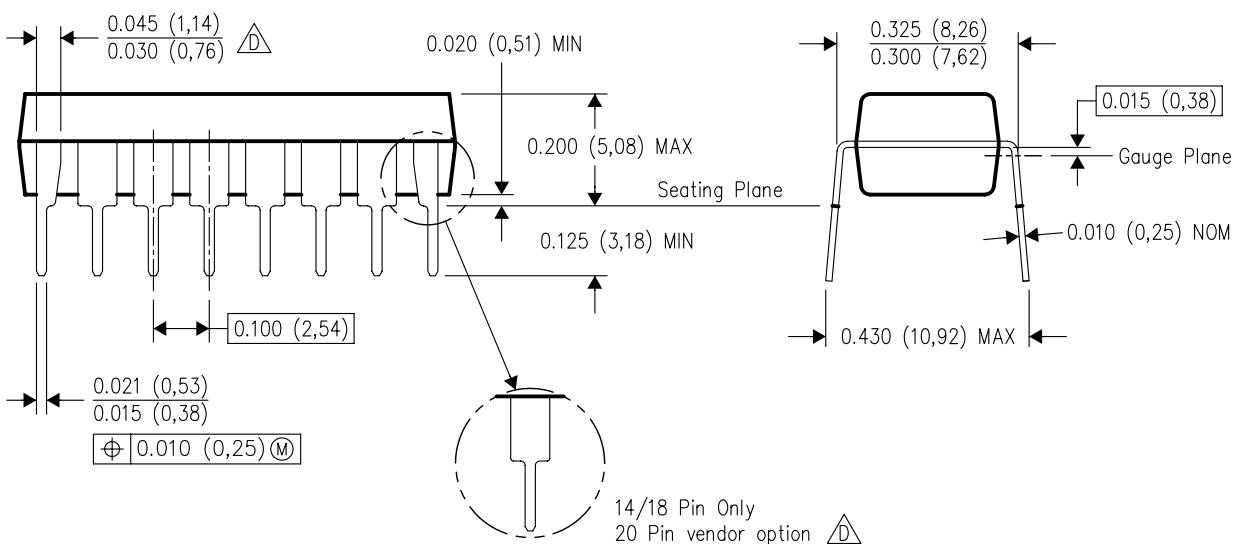
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

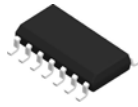


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

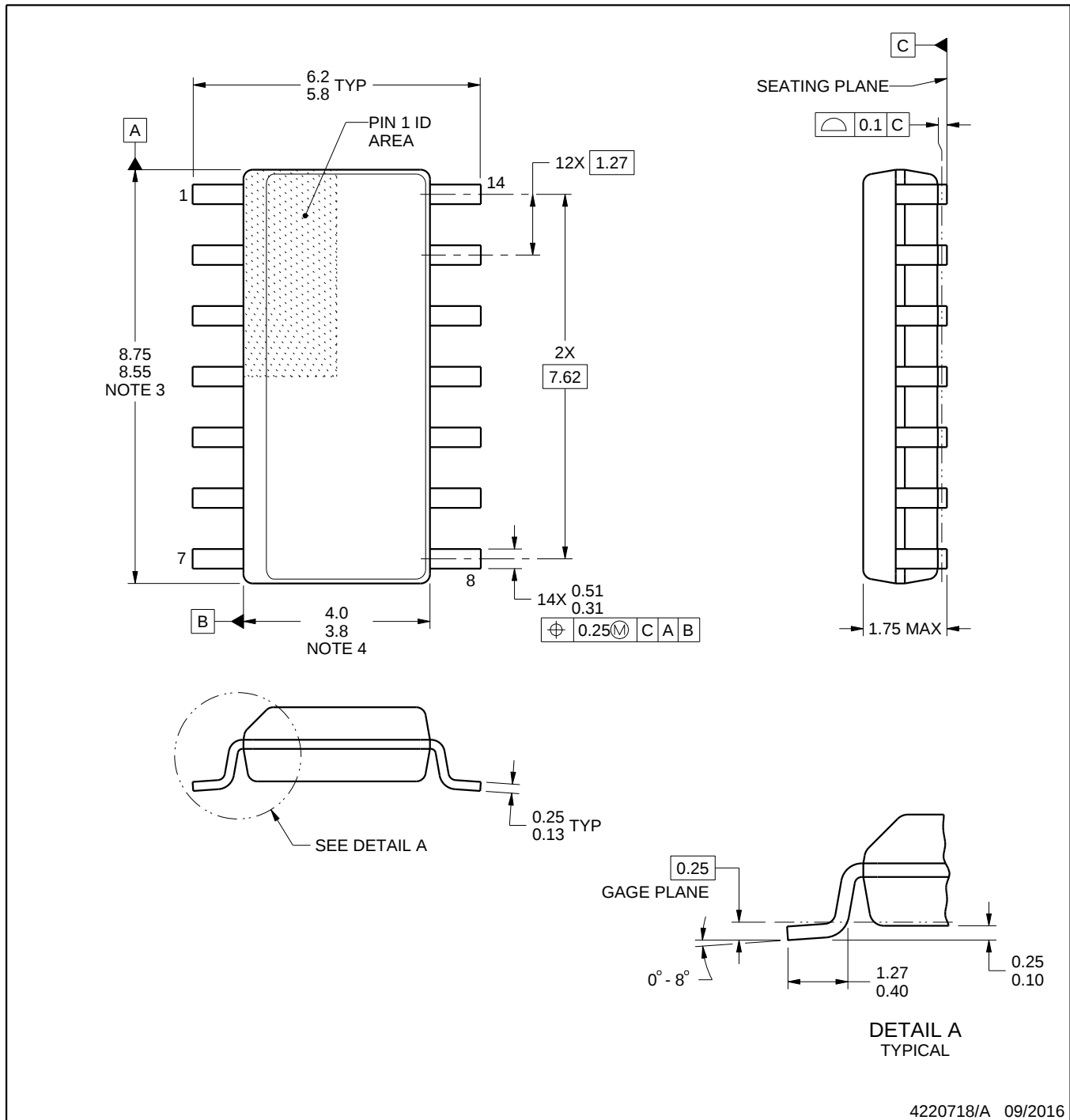


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

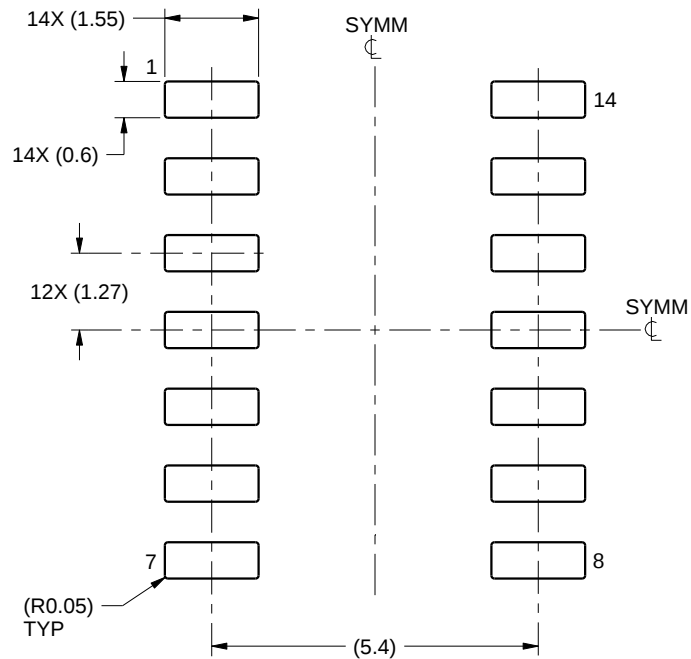
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

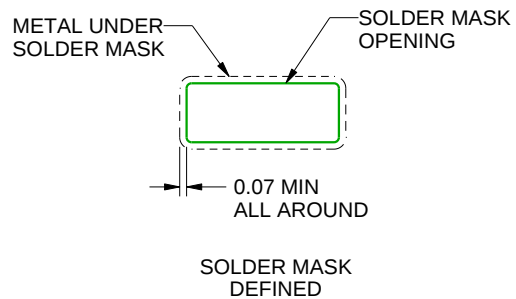
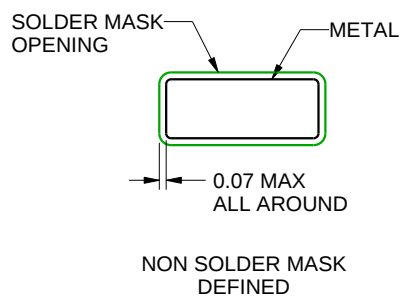
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

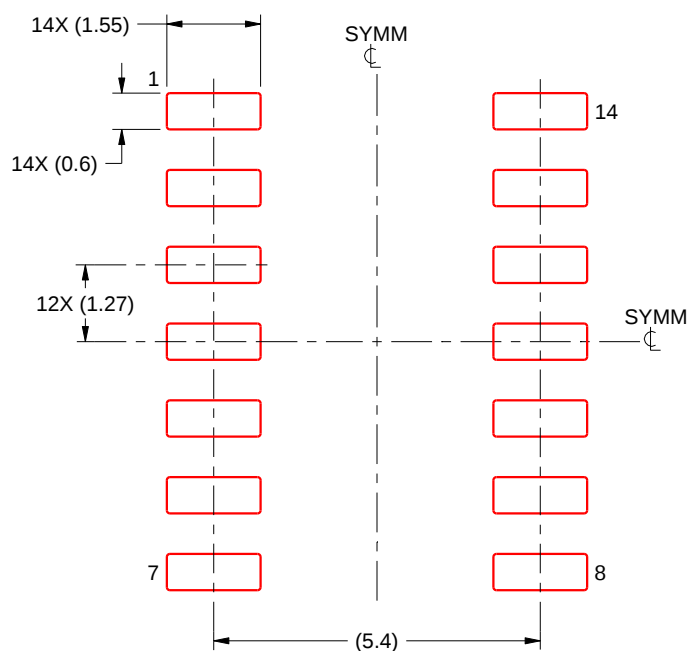
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

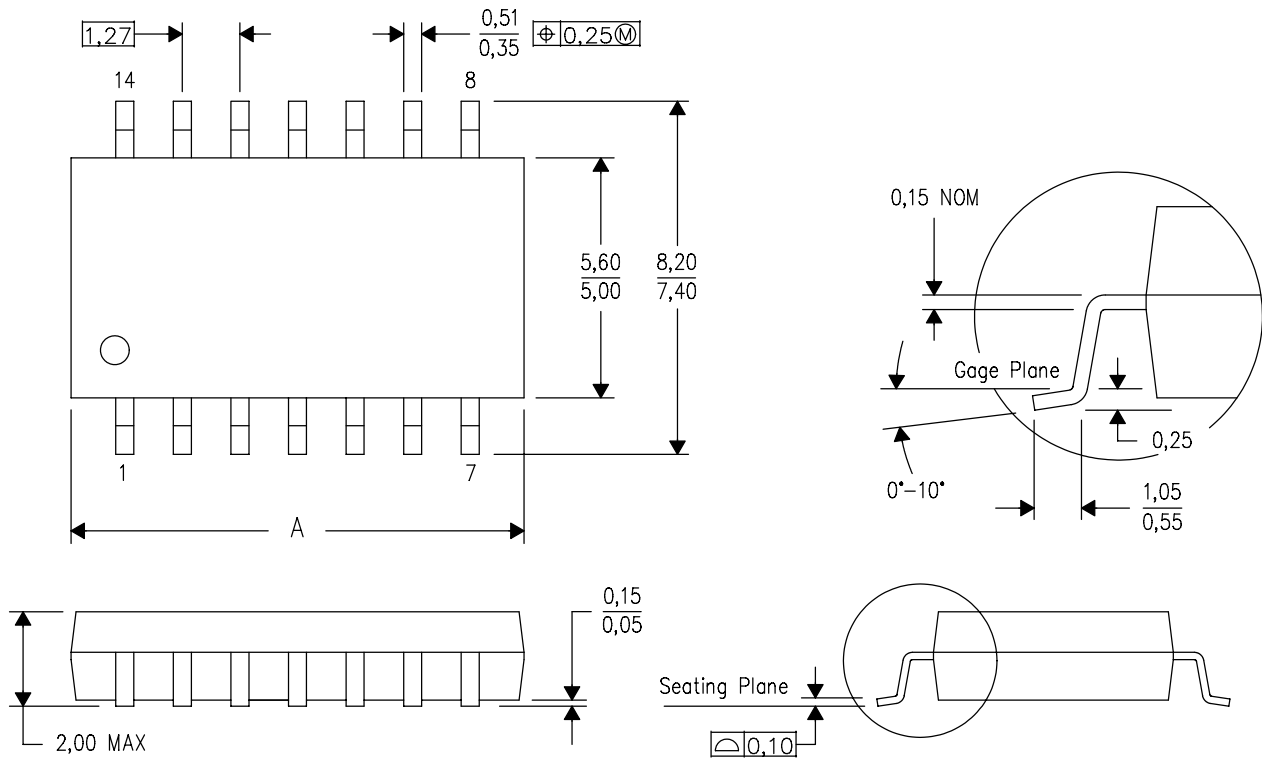
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated