TPS650830 Simple and Flexible Wide Input Voltage PMU for Mobile Computers

1 Device Overview

1.1 Features

- 5 Reconfigurable Voltage Regulators:
  - High Efficiency over a Wide Input Voltage and Wide Output Current Range
  - Voltage, Current, and Sequence can be Changed to Optimize the System
  - 4 Variable Output Voltage Step-Down Controllers using External Power MOSFETs:
    - VR1 = 1 V; VR3 = 3.3 V , VR4 = 1.2 V/1.35 V/1.1 V for DDRx VDDQ , VR5 = 5 V
    - V_{IN} Range from 5.4 V to 24 V
  - 1 Variable Output Voltage Step-Down Converter with Internal Power MOSFETs:
    - VR2 = 1.8 V
    - V_{IN} Range from 3 V to 3.6 V
    - Up to 2 A of Continuous Output Current
  - Output Voltage DC Accuracy ±1%; with Differential Output Voltage Sensing
  - Ultra Low Quiescent Current Mode, Typical 30-µA Quiescent Current per Controller or Converter
- 3 Fixed LDO Voltage Regulators:
  - LDO1: Fixed Output Voltage LDO for DDRx VTT (Vout = VDDQ/2)
    - Up to 1 A of Continuous Output Current, DC+AC Accuracy ±5%, 2 A Peak
  - LDO3: 3.3-V Fixed Output Voltage LDO, DC Accuracy ±1%, < 40 mA
    - High Precision Reference Supply for External ADC
    - 3.3-V Load Switch for EC_VCC Rail
  - LDO5: 5-V Fixed Output Voltage LDO, DC Accuracy ±1%, < 100 mA
    - Automatic Switch to 5-V Regulator for Higher Efficiency
- 7 Powergood Comparators and Sequence Logic for External Voltage Regulators, Load Switches, or LDOs
- Power-Button Logic Supported with Programmable Response Time
- 3 General Purpose Level Shifters
- Backup Battery / 3.1-V LDO Selector Output for RTC
- Power Source Detection and Monitoring: Adapter, Battery1, Battery2
- Board Temperature Monitoring
- 1-Hz EC-Wake Clock Output
- Advanced System Reset Control
- I^2C Interface: Standard-Mode (100 kHz), Fast-Mode (400 kHz), Fast-Mode Plus (1000 kHz)

1.2 Applications

- NVDC or Non-NVDC
  2, 3, or 4 Series-Cell Li Battery Powered Products
- Tablet, Ultrabook, 2in1, and Notebook Computers
- Mobile PC's, All-in-Ones, Mobile Internet Devices

1.3 Description

The TPS650830 is a single-chip solution Power Management IC designed specifically for the latest Intel Processors targeted for Tablets, Ultrabooks, and Notebooks with NVDC or non-NVDC power architectures, using 2S, 3S, or 4S Lithium-Ion battery packs.

The TPS650830 is used for Volume systems with the low voltage rails merged for the smallest footprint and lowest cost system power solution.

The TPS650830 can provide the complete power solution based on the Intel Reference Designs. Five highly efficient step-down voltage regulators (VRs) and a sink/source LDO, are used along with power-up sequence logic managing external load switches to provide the proper power rails, sequencing, and protection - including DDR3 and DDR4 memory power. The regulators support dynamic voltage scaling (DVS) for maximum efficiency including Connected Standby. The high frequency voltage regulators use small inductors and capacitors to achieve a small solution size. Output power is adjustable on four VR controllers. An I^2C interface allows simple control by the embedded controller (EC). Each version is available in a 7x7 NFBGA package and a 9x9 NFBGA package. The 7x7 NFBGA package can be used in Type 4 PCB boards for the smallest area implementation. The 9x9 NFBGA package can be used in Type 3 and Type 4 PCB boards allowing to minimize cost and area.

For the Skylake and Kabylake Power Map implementation, the five PMIC voltage regulators and LDO1 are assigned with the low-voltage rails merged or split according to the configuration. For the Volume (merged low voltage rails) configuration six external load switches are controlled and monitored by using six powergood comparator logic blocs.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS650830	NFBGA (168)	7.00 mm x 7.00 mm
	NFBGA (159)	9.00 mm x 9.00 mm

(1) For more information, see Section 11, *Mechanical Packaging and Orderable Information*.

1.4 Simplified System Diagram

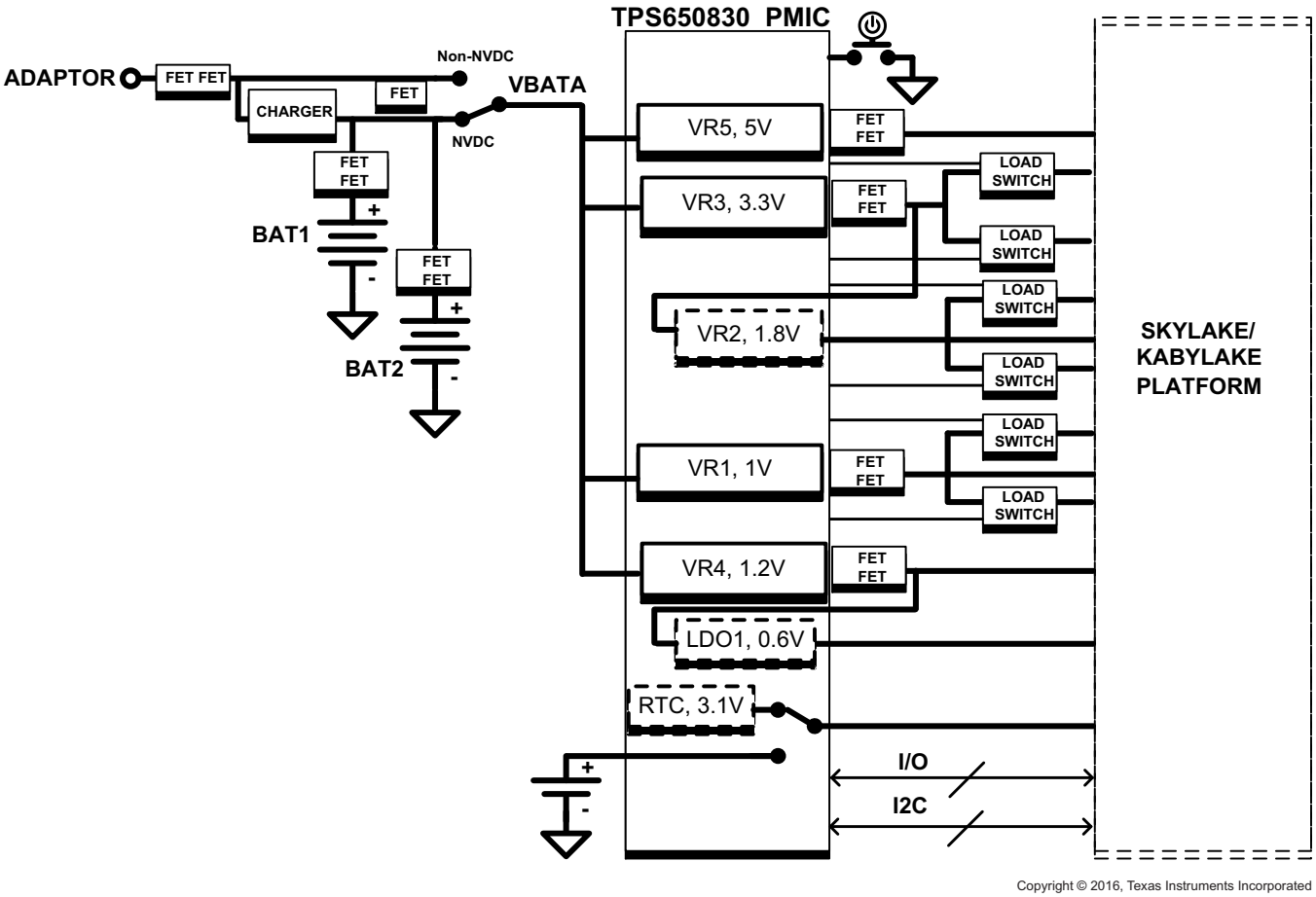


Figure 1-1. Simplified System Diagram

Table of Contents

2 Revision History

Changes from Original (December 2014) to Revision A **Page**

- Changed from data sheet format to data manual format 1
- Changed Applications 1
- Changed Skylake to Skylake and Kabylake throughout data manual 2
- Added Device Options section 6
- Changed pinout diagrams 7
- Added TYPE column to pin functions tables 9
- Added Switch pins - controllers (transient <10 ns) to Absolute Maximum Ratings 14
- Added Switch pins - converter (transient <10 ns) to Absolute Maximum Ratings 14
- Changed Output alert pin to Output interrupt pin in Absolute Maximum Ratings 15
- Changed Output alert pin to Output interrupt pin in Recommended Operating Conditions 17
- Separated the VDD domains 19
- Changed Critical supply voltage (VDCSNS) falling threshold 22
- Added Critical supply voltage (VDCSNS) input current 22
- Added Internal Ramp Comparator 22
- Added Emergency Reset Shutdown 22
- Deleted Low-side output valley current limit 23
- Added Current limit (Vsw - PGND) voltage specifications 23
- Added Negative current limit (Vsw - PGND) voltage specifications 23
- Added VR1 Soft-Start specifications 24
- Added VR1 DVS specifications 24
- Added VR1 Decay exit specifications 24
- Added VR1_Powergood deglitch time 25
- Added VR1_Powergood Mask specifications 25
- Added VR1_Force PWM specifications 26
- Changed VR2 Low side valley cycle by cycle positive current limit min value from 2000 mA to 2260 mA 26
- Changed VR2 Low side valley cycle by cycle positive current limit max value from 2450 mA to 3360 mA 26
- Added VR2 Soft-Start specifications 27

- Added VR2 DVS specifications 27
- Added VR2_Powergood Mask specifications 28
- Added VR2_Force PWM specifications 29
- Deleted High-side output peak current limit 29
- Added Current limit (Vsw - PGND) voltage specifications 29
- Added Negative current limit (Vsw - PGND) voltage specifications 30
- Deleted VR3 Controller Power Low-side output valley current limit 30
- Deleted VR3 Controller Power Soft-Start total turn-on time 30
- Added VR3 Soft-Start specifications 30
- Changed VR3 Controller Power Soft-Start delay time values 30
- Added VR3 DVS specifications 30
- Added VR3 Decay exit specifications 31
- Added VR3_Powergood deglitch 32
- Added VR3_Powergood Mask specifications 32
- Added VR3_Force PWM specifications 32
- Deleted VR3 Controller Control VR3 delay time from enable to switching 33
- Deleted Low-side output valley current limit 34
- Added Current limit (Vsw - PGND) voltage specifications 34
- Added Negative current limit (Vsw - PGND) voltage specifications 34
- Deleted VR4 Controller Power Soft-Start total turn-on time 35
- Added VR4 Soft-Start specifications 35
- Changed VR4 Controller Power Soft-Start delay time values 35
- Added VR4 DVS specifications 35
- Added VR4_Powergood deglitch 36
- Added VR4_Powergood Mask specifications 36
- Added VR4_Force PWM specifications 37
- Added LDO1_Powergood deglitch 38
- Deleted High-side output peak current limit 39
- Added Current limit (Vsw - PGND) voltage specifications 39
- Added Negative current limit (Vsw - PGND) voltage specifications 39
- Deleted VR5 Controller Power Low-side output valley current limit 39
- Added VR5 Soft-Start specifications 40
- Added VR5 DVS specifications 40
- Added VR5_Powergood deglitch 41
- Added VR5_Powergood Mask specifications 41
- Added VR5_Force PWM specifications 42
- Added 16 ms delay from ENVR3 to start switching of VR3 in Figure 5-1 45
- Changed Table 6-1 52
- Added Section 6.3.2 53
- Added Section 6.3.3 54
- Added Section 6.3.4 55
- Added Section 6.3.5 56
- Added Section 6.3.6 57
- Added Section 6.3.7 57
- Added Section 6.3.8 58
- Added Section 6.3.9 60
- Added Section 6.3.10 61
- Added Section 6.3.11 63
- Added Section 6.3.12 64
- Added Figure 6-15 and following paragraph 66
- Deleted last paragraph and equation from Section 6.3.13.4 68
- Changed and moved Section 6.4 70
- Moved Section 6.5.1 to Section 6.5 72
- Added Table 6-3 75
- Changed register formatting, reordered registers, and deleted Default from field descriptions 77
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-47 110
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-48 111
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-49 112
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-50 113
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-51 114

- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-52 115
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-53 116
- Changed O to Ω in bit 7 description in Table 6-54 117
- Changed ? 1V to >1.05V in bit 6:3 description in Table 6-54 117
- Changed O to Ω in bit 0 description in Table 6-59 122
- Deleted last two paragraphs and equation from Section 7.2.2.1.2 130

3 Device Options

Table 3-1. Voltage Regulator and Powergood Comparator Logic Assignment for Skylake and Kabylake Platforms

TPS650830	Skylake and Kabylake PLATFORM POWER SYSTEM VOLTAGE RAIL VOLUME (Merged Low Voltage Rails)	OUTPUT VOLTAGE, V_{out} DEFAULT, or COMPARATOR INPUT	SWITCHING FREQUENCY, F_{sw} NVDCZ = 1 / 0	LPM VOLTAGE, V_{out} Default	POWER GOOD OUTPUT SETTING, (PGVRx or PGx is PP or OD)
VR1	V1.00A / V 0.85A	1.00 V	500 kHz / 800 kHz	LPM = 1.00 V	PP
VR2	V1.8A	1.8 V	2 MHz / 2 MHz	LPM = 1.8 V	PP
VR3	V3.3A_DSW	3.3 V	800 kHz / 800 kHz	LPM = 3.3 V	PP
VR4	V1.2U	1.2 V,1.35 V,1.1 V	500 kHz / 800 kHz	LPM = 1.2 V,1.35 V,1.1 V	OD
VR5	V5A_DS3	5 V	800 kHz / 800 kHz	LPM = 5.0 V	PP
LDO1	V0.6Dx	0.6 V, 0.675 V, 0.55 V	-	LPM = DDR_VTT_CTRL = Off	NA
External VR_a	none	-	-	-	--
External VR_b	none	-	-	-	--
Powergood Comparator Logic a	V3.3A_PCH Enable/Sense External Load Switch	3.3 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic b	V1.8U_2.5U Enable/Sense External Load Switch	1.8 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic c	Generic Comparator	- Comparator Disabled	–	–	-
Powergood Comparator Logic d	VCCIO Enable/Sense External Load Switch	1.00 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic e	V3.3S Sense External Load Switch	3.3 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic f	V1.8S Sense External Load Switch	1.8 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic g	V1.0S Sense External Load Switch	1.00 V, Comparator Analog Input	–	–	OD

4 Pin Configuration and Functions

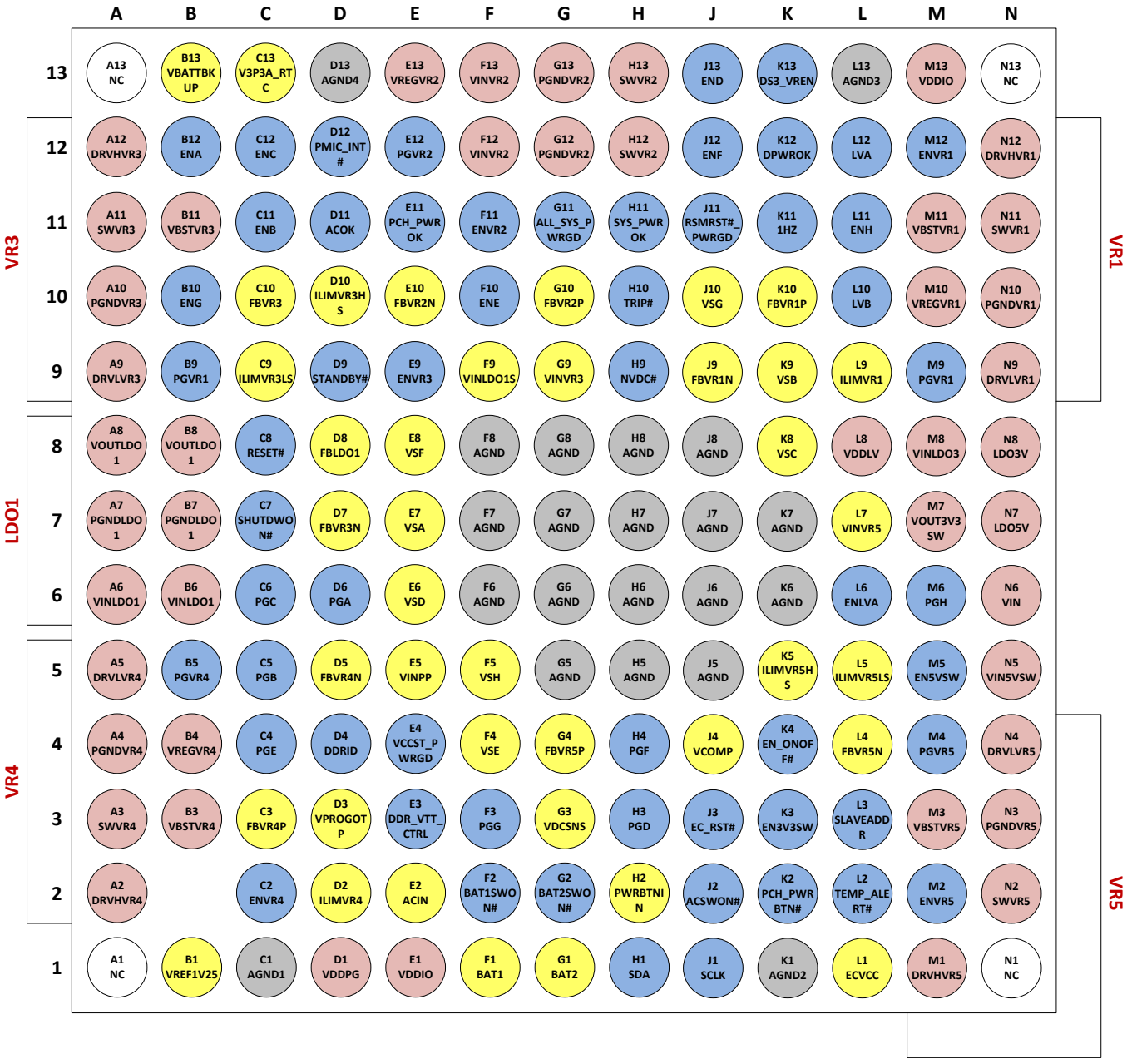


Figure 4-1. 168-Pin 7x7 ZAJ NFBGA (Top View)

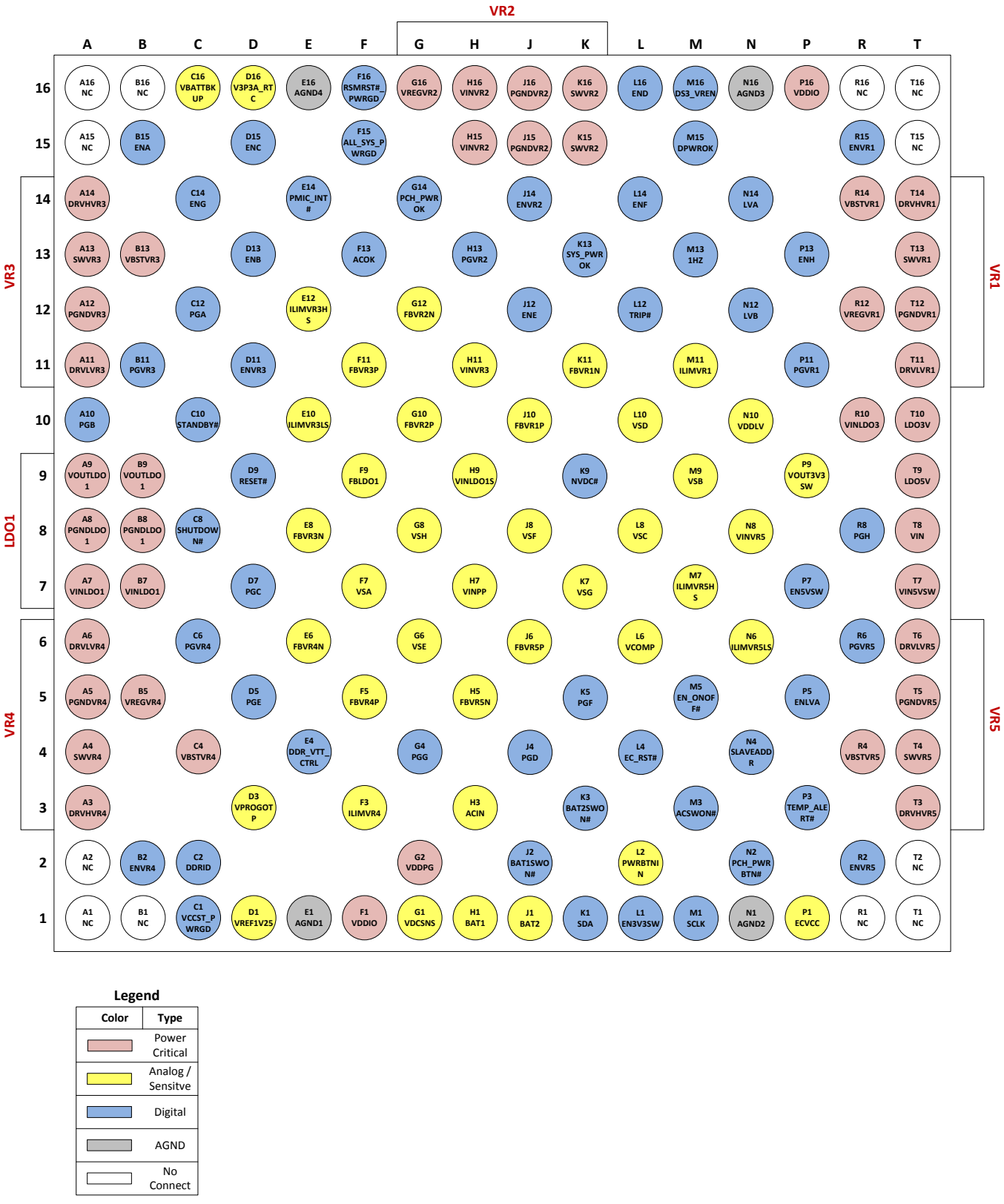


Figure 4-2. 159-Pin 9x9 ZCG NFBGA (Top View)

4.1 Pin Functions

Table 4-1. Pin Functions

PIN			I/O	TYPE(1)	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER			
ACIN	E2	H3	I	AS	AC Adaptor voltage sense
ACOK	D11	F13	I	D	ACOK input
ACSWONZ	J2	M3	O	D	AC adaptor switch ON power-path (Open-drain output) (active low)
AGND	F8, G8, H8, J8, F7, G7, H7, J7, K7, F6, G6, H6, J6, K6, G5, H5, J5	-	-	A	Analog GND - tie directly to the ground plane
AGND1	C1	E1	-	A	Analog GND1 - tie directly to the ground plane
AGND2	K1	N1	-	A	Analog GND2 - tie directly to the ground plane
AGND3	L13	N16	-	A	Analog GND3 - tie directly to the ground plane
AGND4	D13	E16	-	A	Analog GND4 - tie directly to the ground plane
ALL_SYS_PWRGD	G11	F15	O	D	Non-core rails powergood, All PMIC and specified monitored VRs power good (Open-drain output)
BAT1	F1	H1	I	AS	Battery 1 voltage sense input
BAT2	G1	J1	I	AS	Battery 2 voltage sense input
BAT1SWONZ	F2	J2	O	D	Battery 1 switch ON power-path (Open-drain output) (active low)
BAT2SWONZ	G2	K3	O	D	Battery 2 switch ON power-path (Open-drain output) (active low)
DDRID	D4	C2	I	D	VR4 Output voltage selection. Low = 1.2 V, High = 1.35 V, Float = 1.1 V.
DDR_VTT_CTRL	E3	E4	I	D	LDO1 Enable, and DVS control of VR4
DPWROK	K12	M15	O	D	Delayed version of V3.3A_DSW_PG (Open-drain output)
DRVHVR1	N12	T14	O	VR	VR1 High side gate drive output (external power FET)
DRVHVR3	A12	A14	O	VR	VR3 High side gate drive output (external power FET)
DRVHVR4	A2	A3	O	VR	VR4 High side gate drive output (external power FET)
DRVHVR5	M1	T3	O	VR	VR5 High side gate drive output (external power FET)
DRVLVR1	N9	T11	O	VR	VR1 Low side gate drive output (external power FET)
DRVLVR3	A9	A11	O	VR	VR3 Low side gate drive output (external power FET)
DRVLVR4	A5	A6	O	VR	VR4 Low side gate drive output (external power FET)
DRVLVR5	N4	T6	O	VR	VR5 Low side gate drive output (external power FET)
DS3_VREN	K13	M16	O	D	DS3 VR enable (enables external power switches) (Push-pull output)
ECVCC	L1	P1	I	AS	EC VCC supply
EC_ONOFFZ	K4	M5	O	D	Debounced version of PWRBTNIN (Open-drain output) (active low)
EC_RSTZ	J3	L4	O	D	EC reset (Open-drain output) (active low)
ENA	B12	B15	I	D	Enable for VSA powergood comparator
ENB	C11	D13	I	D	Enable for VSB powergood comparator
ENC	C12	D15	I	D	Enable for VSC powergood comparator
END	J13	L16	I	D	Enable for VSD powergood comparator
ENE	F10	J12	I	D	Enable for VSE powergood comparator
ENG	B10	C14	I	D	Enable for VSG powergood comparator
ENF	J12	L14	I	D	Enable for VSF powergood comparator
ENH	L11	P13	I	D	Input to Level Shifter B general purpose level shifter.
ENLVA	L6	P5	I	D	Enable level shifter A. Pin not used for TPS650830. Connect to ground if unused. (Level Shifter A input is ACOK pin)

(1) VR – VR Critical, AS – Analog Sensitive, D – Digital, A - AGND

Table 4-1. Pin Functions (continued)

PIN			I/O	TYPE[1]	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER			
ENVR1	M12	R15	I	D	VR1 Enable
ENVR2	F11	J14	I	D	VR2 Enable
ENVR3	E9	D11	I	D	VR3 Enable
ENVR4	C2	B2	I	D	VR4 Enable
ENVR5	M2	R2	I	D	VR5 Enable
EN3V3SW	K3	L1	I	D	Enable for load switch from LDO3V pin to VOUT3V3SW output pin
EN5VSW	M5	P7	I	D	Enable Internal load switch from 5-V switching regulator to LDO5V output through VIN5VSW. Connect to powergood of 5-V switching regulator.
FBLDO1	D8	F9	I	AS	LDO1 Feedback voltage kelvin sense, (Connect to vout of LDO1 at output load capacitor)
FBVR1N	J9	K11	I	AS	VR1 Negative feedback remote sense (Connect to GND of VR1 at output load capacitor)
FBVR1P	K10	J10	I	AS	VR1 Positive feedback remote sense (Connect to vout of VR1 at output load capacitor)
FBVR2N	E10	G12	I	AS	VR2 Negative feedback remote sense (Connect to GND of VR2 at output load capacitor)
FBVR2P	G10	G10	I	AS	VR2 Positive feedback remote sense (Connect to vout of VR2 at output load capacitor)
FBVR3N	D7	E8	I	AS	VR3 Negative feedback remote sense (Connect to GND of VR3 at output load capacitor)
FBVR3P	C10	F11	I	AS	VR3 Positive feedback remote sense (Connect to vout of VR3 at output load capacitor)
FBVR4N	D5	E6	I	AS	VR4 Negative feedback remote sense (Connect to GND of VR4 at output load capacitor)
FBVR4P	C3	F5	I	AS	VR4 Positive feedback remote sense (Connect to vout of VR4 at output load capacitor)
FBVR5N	L4	H5	I	AS	VR5 Negative feedback remote sense (Connect to GND of VR5 at output load capacitor)
FBVR5P	G4	J6	I	AS	VR5 Positive feedback remote sense (Connect to vout of VR5 at output load capacitor)
ILIMVR1	L9	M11	I	AS	VR1 Current limit setting, low-side FET valley current limit
ILIMVR3HS	D10	E12	I	AS	VR3 Current limit setting, high-side FET peak current limit
ILIMVR3LS	C9	E10	I	AS	VR3 Current limit setting, low-side FET valley current limit
ILIMVR4	D2	F3	I	AS	VR4 Current limit setting, low-side FET valley current limit
ILIMVR5HS	K5	M7	I	AS	VR5 Current limit setting, high-side FET peak current limit
ILIMVR5LS	L5	N6	I	AS	VR5 Current limit setting, low-side FET valley current limit
LDO3V	N8	T10	O	AS	3.3-V LDO used as a reference voltage, and as a pull-up supply.
LDO5V	N7	T9	O	AS	5-V internal supply used primarily for the gate drives
LVA	L12	N14	O	D	Level shifter A open-drain output, used for BC_ACOK output level shifted to EC_VCC. Input is from ACOK pin
LVB	L10	N12	O	D	Level shifter B push-pull output, level shifted to VDDLV. Input is from ENH pin
NVDC#	H9	K9	I	D	NVDC select [two-level: Low = NVDC, High = non-NVDC]. Connect NVDC# to GND for NVDC, Connect NVDC# to LDO3V for non-NVDC
PCH_PWRBTNZ	K2	N2	O	D	Power button signal to PCH (Open-drain output) (active low)
PCH_PWROK	E11	G14	O	D	Core and Non Core powergood, Delayed version of ALL_SYS_PWRGD, (Open-drain output)
PGA	D6	C12	O	D	Powergood comparator output, push-pull to VDDPG
PGB	C5	A10	O	D	Powergood comparator output, push-pull to VDDPG

Table 4-1. Pin Functions (continued)

PIN			I/O	TYPE[1]	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER			
PGC	C6	D7	O	D	Powergood comparator output, push-pull to VDDPG
PGD	H3	J4	O	D	Powergood comparator output, push-pull to VDDPG
PGE	C4	D5	O	D	Powergood comparator output, push-pull to VDDPG
PGF	H4	K5	O	D	Powergood comparator output, push-pull to VDDPG
PGG	F3	G4	O	D	Powergood comparator output, open-drain output
PGH	M6	R8	O	D	Powergood comparator output, open-drain output
PGNDLDO1	A7, B7	A8, B8	-	VR	LDO1 Power GND
PGNDVR1	N10	T12	-	VR	VR1 Power GND
PGNDVR2	G12, G13	J15, J16	-	VR	VR2 Power GND
PGNDVR3	A10	A12	-	VR	VR3 Power GND
PGNDVR4	A4	A5	-	VR	VR4 Power GND
PGNDVR5	N3	T5	-	VR	VR5 Power GND
PGVR1	M9	P11	O	D	VR1 powergood comparator output (Push-pull output)
PGVR2	E12	H13	O	D	VR2 powergood comparator output (Push-pull output)
PGVR3	B9	B11	O	D	VR3 powergood comparator output (Push-pull output)
PGVR4	B5	C6	O	D	VR4 powergood comparator output (Open-drain output)
PGVR5	M4	R6	O	D	VR5 powergood comparator output (Push-pull output)
PMIC_INTZ	D12	E14	O	D	PMIC to EC interrupt (Open-drain output) (active low)
PWRBTNIN	H2	L2	I	AS	Power button input (internal pull-up to LDO3V) (active low)
RESETZ	C8	D9	O	D	Global disable output for external converters/power tree (active low)
RSMRSTZ_PWRGD	J11	F16	O	D	Resume Reset powergood (Open-drain output) (active low)
SCLK	J1	M1	I	D	I^2C Clock
SDA	H1	K1	I/O	D	I^2C Data
SHUTDOWNZ	C7	C8	I	D	Set shutdown mode (all supplies off) (active low)
SLAVEADDR	L3	N4	I	D	I^2C Slave Address select (low = 0x30, high = 0x32, open = float = 0x34). Keep same connection during operation.
STANDBYZ	D9	C10	I	D	Set rails in standby when low (low power mode)
SWVR1	N11	T13	I	VR	VR1 Switch node connection
SWVR2	H12, H13	K15, K16	I	VR	VR2 Switch node connection
SWVR3	A11	A13	I	VR	VR3 Switch node connection
SWVR4	A3	A4	I	VR	VR4 Switch node connection
SWVR5	N2	T4	I	VR	VR5 Switch node connection
SYS_PWROK	H11	K13	O	D	Delayed version of ALL_SYS_PWRGD (Open-drain output)
TEMP_ALERTZ	L2	P3	O	D	Open-drain output of silicon temperature sensor. Input to Power Monitor Unit (connect to PROCHOT# of system). Active low, recommended pull-up to V1.00S with 50 Ω.
TRIPZ	H10	L12	O	D	VCOMP comparator push-pull output (active low)
VBATTBKUP	B13	C16	I	AS	RTC backup battery supply connection
VBSTVR1	M11	R14	I	VR	VR1 Bootstrap pin
VBSTVR3	B11	B13	I	VR	VR3 Bootstrap pin
VBSTVR4	B3	C4	I	VR	VR4 Bootstrap pin
VBSTVR5	M3	R4	I	VR	VR5 Bootstrap pin
VCCST_PWRGD	E4	C1	O	D	VCCST powergood (Open-drain output)
VCOMP	J4	L6	I	AS	VCOMP comparator input
VDCSNS	G3	G1	I	AS	VDC voltage monitor

Table 4-1. Pin Functions (continued)

PIN			I/O	TYPE(1)	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER			
VDDIO	E1, M13	F1, P16	I	VR	Voltage supply input for I/O buffers. VDDIO should be tied to LDO3V (3.3 V)
VDDLV	L8	N10	I	VR	LVx buffer supply, sets output level for Level Shifter pins
VDDPG	D1	G2	I	VR	PGx supply, sets output level for PG pins for A-H, if PG pin is push-pull
VDD5 VPROGOTP	D3	D3	I	AS	Always connect to LDO5V. supply voltage for OTP programming (must be connected to LDO5V in normal operation)
VIN	N6	T8	I	VR	IC input voltage
VINLDO1	A6, B6	A7, B7	I	VR	LDO1 Input supply
VINLDO3	M8	R10	I	VR	LDO3V input supply
VINLDO1S	F9	H9	I	AS	LDO1 Input voltage reference sense (Connect to vout of VR4 at output load capacitor)
VINPP	E5	H7	I	AS	VIN for Power Path Domain. Connect to external diode OR from: AC, BAT1, BAT2.
VINVR2	F12, F13	H15, H16	I	VR	VR2 Power Input voltage. Connect to a 3.3-V voltage regulator, such as V3.3A_DSW .
VINVR3	G9	H11	I	AS	VR3 Input voltage sense and high-side current-sense (Kelvin connect to drain of high-side FET)
VINVR5	L7	N8	I	AS	VR5 Input voltage sense and high-side current-sense (Kelvin connect to drain of high-side FET)
VIN5VSW	N5	T7	I	VR	Internal load switch from 5-V switching regulator to LDO5Voutput. Connect VIN5VSW to 5-V switching regulator output.
VOUTLDO1	A8, B8	A9, B9	O	VR	LDO1 Output voltage, VOUTLDO1 = (1/2 * VINLDO1SNS)
VOUT3V3SW	M7	P9	O	VR	EC domain load switch output and discharge path from LDO3V
VREF1V25	B1	D1	O	AS	Decoupling cap connection for internal voltage reference
VREGVR1	M10	R12	I	VR	5-V drive supply input (shorted on board with LDO5V), supply for VR1 and VR5
VREGVR2	E13	G16	I	VR	VR2 5-V drive supply input (shorted on board with LDO5V)
VREGVR4	B4	B5	I	VR	VR4 5-V drive supply input (shorted on board with LDO5V), shared with VR3
VSA	E7	F7	I	AS	Powergood comparator input and discharge path for external rail
VSB	K9	M9	I	AS	Powergood comparator input and discharge path for external rail
VSC	K8	L8	I	AS	Powergood comparator input and discharge path for external rail
VSD	E6	L10	I	AS	Powergood comparator input and discharge path for external rail
VSE	F4	G6	I	AS	Powergood comparator input and discharge path for external rail
VSF	E8	J8	I	AS	Powergood comparator input and discharge path for external rail
VSG	J10	K7	I	AS	Powergood comparator input and discharge path for external rail
VSH	F5	G8	I	AS	Powergood comparator input and discharge path for external rail
V3P3A_RTC	C13	D16	O	AS	PCH RTC power supply
1HZ	K11	M13	O	D	1-Hz clock output for waking up embedded controller, EC.

Table 4-1. Pin Functions (continued)

PIN			I/O	TYPE(1)	DESCRIPTION
NAME	ZAJ PACKAGE NUMBER	ZCG PACKAGE NUMBER			
DEPOPULATED BALL - FOR VIAS	No Depopulated Balls for Vias in 7x7. Type 4 PC put micro-vias under each ball pad	B3, B4, B6, B10, B12, B14, C3, C5, C7, C9, C11, C13, C15, D2, D4, D6, D8, D10, D12, D14, E2, E3, E5, E7, E9, E11, E13, E15, F2, F4, F6, F8, F10, F12, F14, G3, G5, G7, G9, G11, G13, G15, H2, H4, H6, H8, H10, H12, H14, J3, J5, J7, J9, J11, J13, K2, K4, K6, K8, K10, K12, K14, L3, L5, L7, L9, L11, L13, L15, M2, M4, M6, M8, M10, M12, M14, N3, N5, N7, N9, N11, N13, N15, P2, P4, P6, P8, P10, P12, P14, P15, R3, R5, R7, R9, R11, R13,	DEPOPULATED BALL	-	VIA PLACEMENT FOR INTERNAL BALL ROUTES - For Type3 PCBs, put a plated through-hole (PTH) via at each depopulated ball, to connect to the internal row balls.
DEPOPULATED BALL - PICK-N-PLACE INDICATOR	B2	C3 (also used for via - see below)	DEPOPULATED BALL	-	PICK-N-PLACE INDICATOR
NC POPULATED BALL - CORNERS	A1, A13, N1, N13	A1, A2, B1, A15, A16, B16, R16, T16, T15, R1, T1, T2	POPULATED BALL	-	CORNERS - solder to PCB for mechanical strength

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
CHIP				
Power input pins	VIN, VINLDO3	-0.3	28	V
Analog ground pins	AGND1, AGND2, AGND3, AGND4, AGND (16 center pins)	-0.3	0.3	V
SWITCHING REGULATORS				
Input pins - controllers	VINVR3, VINVR5	-0.3	28	V
Switch pins - controllers	SWVR1 , SWVR3 , SWVR4 , SWVR5	-1	28	V
Switch pins - controllers (transient <10 ns)	SWVR1 , SWVR3 , SWVR4 , SWVR5 (transient <10 ns)	-2	28	V
High drive pins - controllers	DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5	-0.3	32	V
Low drive pins - controllers	DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5	-0.3	7	V
Bootstrap pins - controllers	VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5	-0.3	32	V
Bootstrap pins - controllers	Differential voltage between VBSTVRx and SWVRx	-0.3	7	V
Input pin - converter	VINVR2	-0.3	3.6	V
Switch pins - converter	SWVR2	-1	4.0	V
Switch pins - converter (transient <10 ns)	SWVR2 (transient <10 ns)	-2	5.5	V
Power ground pins	PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5	-0.3	0.3	V
Enable pins	ENVR1, ENVR2, ENVR3, ENVR4, ENVR5	-0.3	3.6	V
NVDC select pin	NVDC#	-0.3	3.6	V
Positive remote feedback pins	FBVR1P, FBVR2P, FBVR3P, FBVR4P	-0.3	3.6	V
Positive remote feedback pin	FBVR5P	-0.3	5.7	V
Negative remote feedback pins	FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N	-0.3	0.3	V
Gate drive regulator input power pins	VREGVR1, VREGVR2, VREGVR4	-0.3	5.7	V
Low-side current limit	ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS	-0.3	3.6	V
High-side current limit	ILMVR3HS, ILMVR5HS	-0.3	3.6	V
LDO REGULATOR				
Input pin	VINLDO1	-0.3	3.6	V
Output pin	VOUTLDO1	-0.3	3.6	V
Power ground pin	PGNDLDO1	-0.3	0.3	V
Input feedback pin	VINLDO1S	-0.3	3.6	V
Output feedback pin	FBLDO1	-0.3	3.6	V
I2C				
SCLK, SDAT, SLAVEADDR		-0.3	3.6	V
POWERGOOD COMPARATOR LOGIC				
Powergood (push/pull) supply for input pins	VDDPG	-0.3	3.6	V
Powergood input voltage sense pins	VSA, VSB, VSC, VSD, VDE, VSF, VSG, VSH	-0.3	5.7	V
Powergood enable pins	ENA, ENB, ENC, END, ENE, ENF, ENG, ENH	-0.3	3.6	V
Powergood output pins	PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5	-0.3	3.6	V
POWERGOOD TREE LOGIC				
Open-drain outputs	DPWROK, RSMRSTZ_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK	-0.3	3.6	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Absolute Maximum Ratings *(continued)*

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
DDR CONTROL				
Input pins	DDR_VTT_CTRL, DDRID	-0.3	3.6	V
LEVEL SHIFTERS				
Level shifter (push/pull) supply input pin	VDDLV	-0.3	3.6	V
Level shifter enable input pins	ENLVA	-0.3	3.6	V
Level shifter output pins	LVA, LVB	-0.3	3.6	V
POWER PATH LOGIC				
Power path comparator input voltage sense pins	VCOMP, BAT1, BAT2, ACIN	-0.3	7	V
Power path comparator open-drain output pins	BAT1SWONZ, BAT2SWONZ, ACSWONZ	-0.3	28	V
PTC over-temperature comparator open-drain output pin	TRIPZ	-0.3	3.6	V
Power path domain diode OR input pin	VINPP	-0.3	28	V
POWER BUTTON				
PWRBNTIN, PCH_PWRBTNZ, EC_ONOFFZ		-0.3	3.6	V
RESETS				
ECVCC, RESETZ, EC_RSTZ		-0.3	3.6	V
CLOCKS				
EC wake clock: 1HZ		-0.3	3.6	V
POWER MONITOR				
VDCSNS		-0.3	28	V
TEMP_ALERTZ		-0.3	3.6	V
ACOK		-0.3	12	V
REFERENCE				
LDO output pins	LDO5V	-0.3	7	V
LDO output pins	VREF1V25, LDO3V	-0.3	3.6	V
3.3-V load switch enable pin	EN3V3SW	-0.3	3.6	V
3.3-V load switch output pin	VOUT3V3SW	-0.3	3.6	V
5-V load switch enable pin	EN5VSW	-0.3	3.6	V
5-V load switch input pin	VIN5VSW	-0.3	6	V
BACKUP BATTERY RTC SELECTOR				
VBATTBKUP, V3P3A_RTC		-0.3	3.6	V
MISC				
Input control pins	STANDBYZ, SHUTDOWNZ	-0.3	3.6	V
Output interrupt pin	PMIC_INTZ	-0.3	3.6	V
Output DS3 VR enable pin	DS3_VREN	-0.3	3.6	V
Buffers supply input pin	VDDIO	-0.3	3.6	V
VPROGOTP		-0.3	7	V
GENERAL				
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
CHIP			
Power input pins: VIN, VINLDO3	-0.3	21	V
Analog ground pins: AGND1, AGND2, AGND3, AGND4, AGND (16 center pins)	-0.3	0.3	V
SWITCHING REGULATORS			
Input pins - controllers: VINVR3, VINVR5	-0.3	21	V
Switch pins - controllers: SWVR1 , SWVR3 , SWVR4 , SWVR5	-1	21	V
High drive pins - controllers: DRVHVR1, DRVHVR3, DRVHVR4, DRVHVR5	-0.3	26	V
Low drive pins - controllers: DRVLVR1, DRVLVR3, DRVLVR4, DRVLVR5	-0.3	5	V
Bootstrap pins - controllers: VBSTVR1, VBSTVR3, VBSTVR4, VBSTVR5	-0.3	26	V
Bootstrap pins - controllers: (differential voltage between VBSTVRx and SWVRx)	-0.3	5	V
Input pin - converter: VINVR2	-0.3	3.3	V
Switch pins - Converter: SWVR2	-1	3.3	V
Power ground pins: PGNDVR1, PGNDVR2, PGNDVR3, PGNDVR4, PGNDVR5	-0.3	0.3	V
Enable pins: ENVR1, ENVR2, ENVR3, ENVR4, ENVR5	-0.3	3.3	V
NVDC select pin: NVDC#	-0.3	3.3	V
Positive remote feedback pins: FBVR1P, FBVR2P, FBVR3P, FBVR4P	-0.3	3.3	V
Positive remote feedback pin: FBVR5P	-0.3	5	V
Negative remote feedback pins: FBVR1N, FBVR2N, FBVR3N, FBVR4N, FBVR5N	-0.3	0.3	V
Gate drive regulator input power pins: VREGVR1, VREGVR2, VREGVR4	-0.3	5	V
Low-side current limit: ILIMVR1, ILIMVR3LS, ILIMVR4, ILMVR5LS	-0.3	3.3	V
High-side current limit: ILMVR3HS, ILMVR5HS	-0.3	3.3	V
LDO REGULATOR			
Input pin: VINLDO1	-0.3	3.3	V
Output pin: VOUTLDO1	-0.3	1.65	V
Power ground pin: PGNDLDO1	-0.3	0.3	V
Input feedback pin: VINLDO1S	-0.3	3.3	V
Output feedback pin: FBLDO1	-0.3	1.65	V
I2C			
SCLK, SDAT, SLAVEADDR	-0.3	3.3	V
POWERGOOD COMPARATOR LOGIC			
Powergood (push/pull) supply for input pins: VDDPG	-0.3	3.3	V
Powergood input voltage sense pins: VSA, VSB, VSC, VSD, VDE, VSF, VSG, VSH	-0.3	5	V
Powergood enable pins: ENA, ENB, ENC, END, ENE, ENF, ENG, ENH	-0.3	3.3	V
Powergood output pins: PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5	-0.3	3.3	V
POWERGOOD TREE LOGIC			
Open-drain outputs: DPWROK, RSMRSTZ_PWRGD, VCCST_PGOOD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK	-0.3	3.3	V
DDR CONTROL			
Input pins: DDR_VTT_CTRL, DDRID	-0.3	3.3	V

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
LEVEL SHIFTERS			
Level shifter (push/pull) supply input pin: VDDLV	-0.3	3.3	V
Level shifter enable input pins: ENLVA	-0.3	3.3	V
Level shifter output pins: LVA, LVB	-0.3	3.3	V
POWER PATH LOGIC			
Power path comparator input voltage sense pins: VCOMP, BAT1, BAT2, ACIN	-0.3	5	V
Power path comparator open-drain output pins: BAT1SWONZ, BAT2SWONZ, ACSWONZ	-0.3	21	V
PTC over-temperature comparator open-drain output pin: TRIPZ	-0.3	3.3	V
Power path domain diode or input pin: VINPP	-0.3	21	V
POWER BUTTON			
PWRBNTIN, PCH_PWRBTNZ, EC_ONOFFZ	-0.3	3.3	V
RESETS			
ECVCC, RESETZ, EC_RSTZ	-0.3	3.3	V
CLOCKS			
EC Wake Clock: 1 HZ	-0.3	3.3	V
POWER MONITOR			
VDCSNS	-0.3	21	V
TEMP_ALERTZ	-0.3	3.3	V
ACOK	-0.3	3.3	V
REFERENCE			
LDO output pins: LDO5V	-0.3	5	V
LDO output pins: VREF1V25, LDO3V	-0.3	3.3	V
3.3-V load switch enable pin: EN3V3SW	-0.3	3.3	V
3.3-V load switch output pin: VOUT3V3SW	-0.3	3.3	V
5-V load switch enable pin: EN5VSW	-0.3	3.3	V
5-V load switch input pin: VIN5VSW	-0.3	5	V
BACKUP BATTERY RTC SELECTOR			
VBATTBKUP, V3P3A_RTC	-0.3	3.3	V
MISC			
Input control pins: STANDBYZ, SHUTDOWNZ	-0.3	3.3	V
Output interrupt pin: PMIC_INTZ	-0.3	3.3	V
Output DS3 VR enable pin: DS3_VREN	-0.3	3.3	V
Buffers supply input pin: VDDIO	-0.3	3.3	V
VPROGOTP	-0.3	5	V
GENERAL			
Operating free air temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	°C

5.4 Thermal Information

THERMAL METRIC (1)		TPS650830		UNIT
		ZAJ (NFBGA)	ZCG (NFBGA)	
		168 PINS	159 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	13.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL						
CONTROL - SYSTEM						
V_{IN} Parametric	System input voltage	Parametric and functional	5.4	7.4	21	V
V_{IN} Functional	System input voltage	Functional	5.4	7.4	24	V
I_Q	System quiescent current (includes IDDQ for LDO5V, LDO3V, and VREF1.25V, all registers are default setting)	Measured at VIN = 7.4 V		95	150	µA
$V_{UVLO\_5V\_Main}$	System under voltage lockout threshold - All IC functionality including 5VLDO, except LDO3V and internal refsys	V_{VIN} voltage decreasing - measured at VIN (falling edge)	4.95	5.1	5.25	V
$V_{Hys\_5V\_Main}$	System under voltage lockout threshold hysteresis	V_{VIN} voltage increasing - measured at VIN		200		mV
CONTROL - INTERNAL REFERENCES						
$V_{O(VLDO5)}$	LDO5V output	VIN = 5.4 V - 21 V, 10-mA load	4.9	5.0	5.1	V
Line regulation $V_{O(LDO5V)}$	Line regulation for regulator over operating voltage range	VIN = 5.4 V to 21 V, Measured as ($\Delta V_{O(LDO5V)}/V_{O(LDO5V)}$) over this operating range with 40-mA load current. measured at LDO5V pin with respect to AGND pin			0.5%	
Load regulation $V_{O(LDO5V)}$	Load regulation for regulator over operating current range	VIN = 5.4 V - 21 V Measured as ($\Delta V_{O(LDO5V)}/V_{O(LDO5V)}$) over this operating range with 10-mA to 100-mA load current. measured at LDO5V pin with respect to AGND pin			2%	
$I_{SC\ (LDO5V)}$	Over current protection	Measured at 90% of the regulation voltage	115			mA
$C_{O\ (LDO5V)}$	External output capacitance range after derating	Actual capacitance after derating. ex: 2.7-µF capacitance, then use a 4.7-µF capacitor with 60% deratingat 5 V.	2.7	4.7	10	µF
$V_{O(VREF1V25)}$	VREF1V25 output - Internal buffered bandgap output	See below for output capacitance. measured at VREF1V25 pin with respect to AGND pin	1.244	1.25	1.256	V
$C_{O\ (VREF1V25)}$	External output capacitance range after derating	Actual capacitance after derating. ex: 0.27-µF capacitance, then use a 0.47-µF capacitor with 60% derating at 1.25 V	0.2		1.0	µF
$V_{I(LDO3V)}$	LDO3V input	Parametric and functional	5.4	7.4	21	V
$V_{I(LDO3V)}$	LDO3V input	Functional	3.45	7.4	24	V
$V_{O(LDO3V)}$	LDO3V output	VIN = 7.4 V, 1-mA load	3.267	3.3	3.333	V

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O\ (LDO3V)}$	Output current	Maximum current for external user is limited 40 mA			40	mA
$I_{SC\ (LDO3V)}$	Output circuit current limit	Measured at 90% of the regulation voltage	75			mA
Line regulation $V_{O(LDO3V)}$	Line regulation for regulator over operating voltage range	VIN = 5.4 V to 21 V, Measured as ($\Delta V_{O(LDO3V)}/V_{O(LDO3V)}$) over the operating range with 20-mA load current. measured at LDO3V pin with respect to AGND pin			0.5%	
Load regulation $V_{O(LDO3V)}$	Load regulation for regulator over operating current range	VIN = 7.4 Measured as ($\Delta V_{O(LDO3V)}/V_{O(LDO3V)}$) over this operating range with 0-mA to 50-mA load current. measured at LDO3V pin with respect to AGND pin			0.5%	
$C_{O\ (LDO3V)}$	External output capacitance range after derating	Actual capacitance after derating. ex: 2.7-µF capacitance, then use a 4.7-µF capacitor with 60% deratingat 3.3 V.	2.2	4.7	10	µF
$T_{R\ (LDO3V)}$	Rise time	Measured from 5% to 95% of the output voltage with 2.2 µF	300		450	µs
CONTROL - INPUT/ OUTPUT BUFFERS						
CONTROL - DDR_VTT_CTRL (Intel external connection DDR_VTT_CTRL) - 1 V logic, tolerates 3 V						
$V_{IL\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL input low voltage	Input low voltage threshold			0.49	V
$V_{IH\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL input high voltage	Input high voltage threshold	0.61			V
$V_{HYST\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL hysteresis voltage	Hysteresis voltage		70		mV
$I_{leakage\_DDR\_VTT\_CTRL}$	DDR_VTT_CTRL input current	Input current, Clamped to 1.0 V		0.01	0.2	µA
CONTROL - INPUT TTL BUFFERS (ALL INPUT PINS), (DEFAULT: SHUTDOWNZ, STANDBYZ, ENLVA, EN3V3SW, EN5VSW, ENVR1, ENVR2, ENVR3, ENVR4, ENVR5, ENA. ENB, ENC, END, ENE, ENF, ENG, ENH), (OPTIONAL: VSA, VSB, VSC, VSD, VSE, VSF, VSG, VSH, ENLVA)						
V_{IL_INPUTS}	Input low voltage				0.4	V
V_{IH_INPUTS}	Input high voltage		1.2			V
V_{HYST_INPUTS}	Hysteresis voltage			300		mV
$I_{leakage\_INPUTS}$	Input current	Clamped on 3.3 V		0.01	0.3	µA
$V_{IL\_PWRBTNZ}$	Input low voltage for PWRBTNZ				0.4	V
$V_{IH\_PWRBTNZ}$	Input high voltage for PWRBTNZ	Internal 5-kΩ pull-up resistor between PWRBTNZ pin and VDDIO	1.6			V
$V_{HYST\_PWRBTNZ}$	Hysteresis voltage for PWRBTNZ			580		mV
$I_{Output\_PWRBTNZ}$	Output current for PWRBTNZ when power button is pressed to close and pulling PWRBTNZ to GND.	PWRBTNZ = GND, Internal 5-kΩ pull-up resistor between PWRBTNZ pin and VDDIO		660	790	µA
$T_{EC\_ONOFFZ\_Debouinc\_0e}$	EC_ONOFFZ_Debounce time, 0 setting	Time set to 0 ms, Measured from 0.5% PWBTNZ rising to 5% of the EC_ONOFFZ output		0		ms
$T_{EC\_ONOFFZ\_Debouinc\_30e}$	EC_ONOFFZ_Debounce time, 30 ms setting	Time set to 30 ms, Measured from 0.5% PWBTNZ rising to 5% of the EC_ONOFFZ output		30		ms
CONTROL - VDDIO DOMAIN PUSH-PULL OUTPUTS, (RESETZ, 1HZ, DS3_VREN), (Optional: PGVR1, PGVR2, PGVR3, PGVR4, PGVR5)						
V_{PP}	Pull-up output voltage supply	Pulled-Up to VDDIO pin which should by tied to LDO3V pin = 3.3 V		VDDIO		V
V_{OL_PP}	Low level output voltage	I_{OL} = 3 mA			0.6	V

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH_PP}	High level output voltage	I_{OH} = 3 mA	VDDIO - 0.6			V
CONTROL - VDDPG DOMAIN PUSH-PULL OUTPUTS, (Optional: PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH)						
V_{PP}	Pull-up output voltage supply	Pulled-Up to VDDPG pin		VDDPG		V
V_{OL_PP}	Low level output voltage	I_{OL} = 3 mA			0.6	V
V_{OH_PP}	High level output voltage	I_{OH} = 3 mA	VDDPG - 0.6			V
CONTROL - VDDLV DOMAIN PUSH-PULL OUTPUTS (Optional: LVA, LVB)						
V_{PP_VDDLV}	LV pull-up output voltage supply	Pulled up to VDDLV pin		VDDLV		V
$V_{OL\_PP\_LV}$	LV low level output voltage	I_{OL} = 3 mA			0.6	V
$V_{OH\_PP\_LV}$	LV high level output voltage	I_{OH} = 3 mA	VDDLV - 0.6			V
CONTROL - GENERAL OPEN-DRAIN OUTPUTS, (ACSWONZ, BAT1SWONZ, BAT2SWONZ, VCCST_PWRGD, SYS_PWROK, PCH_PWROK, RSMRSTZ_PWRGD, ALL_SYS_PWRGD, PMIV_INTZ, EC_RSTZ, PCH_PWRBTNZ, EC_ONOFFZ, DPWROK) (Optional: PGA, PGB, PGC, PGD, PGE, PGF, PGG, PGH, PGVR1, PGVR2, PGVR3, PGVR4, PGVR5, LVA, LVB)						
V_{OL_OD1}	OD- output voltage	I_{OL} = 2 mA			0.4	V
I_{LK_OD1}	OD leakage current	$V_{(PIN)}$ = 3.3 V			0.45	µA
CONTROL - OPEN-DRAIN OUTPUT (TEMP_ALERT)						
V_{OL_OD}	Open-drain low level output voltage	I_{OL} = 15 mA, with 75-Ω pull-up resistor to 1 V			0.165	V
I_{LK_OD}	Open-drain leakage current	$V_{(PIN)}$ = 3.3 V, with 75-Ω pull-up resistor to 1 V			0.35	µA
CONTROL - TRISTATE INPUT BUFFER (SLAVEADDR, DDRID)						
$V_{IL\_TRISTATE}$	Low level input voltage	I_{OL} = 6 µA			0.33	V
$V_{IH\_TRISTATE}$	High level input voltage	I_{OH} = 6 µA	1.8			V
$I_{TRISTATE}$	$I_{TRISTATE}$ current	Maximum allowable current in or out of pin when floating to maintain FLOAT logic state	-0.650		0.675	µA
$I_{TRISTATE\_TOTAL\_PIN\_GND}$	Total current drawn when pin connected to GND	VINLDO3 current when TRISTATE pin = GND			6	µA
$I_{TRISTATE\_TOTAL\_PIN\_3.3V}$	Total current drawn when pin connected to 3.3 V	VINLDO3 current when TRISTATE pin = LDO3V = 3.3 V			6	µA
$I_{TRISTATE\_TOTAL\_PIN\_FLOAT}$	Total current drawn when pin Floating	VINLDO3 current when TRISTATE pin = Floating			4.5	µA
CONTROL - VSA, VSB, VSC, VSD, VSE, VSF, VSG, VSH (EXTERNAL VR and EXTERNAL LOADSWITCH POWERGOOD COMPARATORS)						
	VSx input voltage range	When VSx configured as voltage sense input	0.7	1.8	5	V
	VSx input leakage current	When VSx configured as voltage sense input, VSx = 5.7 V	0		9	µA
	Powergood exit threshold high VSx	VSx rising out of powergood. When VSx configured as voltage sense input and powergood window comparator.	106%	108%	110%	
	Powergood threshold high VSx hysteresis	VSx falling into powergood. When VSx configured as voltage sense input and powergood window comparator.		-3%		
	Powergood exit threshold low VSx	VSx falling out of powergood. When VSx configured as voltage sense input and powergood window comparator.	90%	92%	94%	
	Powergood threshold low VSx hystersis	VSx rising into powergood. When VSx configured as voltage sense input and powergood window comparator.		3%		

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{VSx\_POWERGOOD\_DEGLITCH}$	Powergood deglitch time for both rising and falling edges	VSx voltage must cross powergood threshold and stay for at least this time to change powergood output state.Measured from VSx into or out of powergood threshold, until PGx toggles, for both rising and falling edges.	27	30	33	µs
EMBEDDED CONTROLLER RESET						
V_{OL_OD}	EC_RSTZ output low voltage	I_{OL} = 2 mA, V_{EC_RST} = 3.3 V			0.4	V
I_{LKG_OD}	EC_RSTZ leakage current	Output buffer in open-drain mode, V_{EC_RST} = 3.3 V		0.01	0.2	µA
	EC_RST time duration (Trst)	Reset timer register value: 00		20		ms
	EC_RST time duration (Trst)	Reset timer register value: 01		40		ms
	EC_RST time duration (Trst)	Reset timer register value: 10		80		ms
	EC_RST time duration (Trst) - Default setting	Reset timer register value: 11		200		ms
I_{LK}	ECVCC input quiescent current				3	µA
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 000	1.344	1.4	1.456	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 001	1.44	1.5	1.56	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 010	1.536	1.6	1.664	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 011	1.632	1.7	1.768	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 100	2.304	2.4	2.496	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 101	2.496	2.6	2.704	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 110	2.688	2.8	2.912	V
	ECVCC voltage threshold (Vth)	Reset Voltage Threshold register value: 111	2.88	3.0	3.12	V
POWER PATH COMPARATORS and CRITICAL SUPPLY VOLTAGE (ACIN, BAT1, BAT2, VDCSNS)						
	Output low saturation voltage for open-drain logic output pin (TRIPZ)	Comparator input voltage > internal reference voltage. Output pulling low, Sink current = 5 mA			0.5	V
	IOUT VCOMP- internal current source	Current out of the VCOMP pin when IOUT VCOMP enabled	9.5	10	10.6	µA
	VREF_VCOMP_rising, internal reference voltage	Rising voltage at VCOMP pin, changes TRIPZ to logic low	1.211	1.223	1.235	V
	VHYST VCOMPFalling, internal hysteresis voltage	Falling voltage at VCOMP pin, changes TRIPZ to logic high		61		mV
	Output low saturation voltage for open-drain logic output pin (ACSWONZ, BAT1SWONZ, BAT2SWONZ)	Comparator input voltage > internal reference voltage. Output pulling low, Sink current = 5 mA			0.5	V
I_{LKG}	ACIN, BAT1, BAT2 - Current leakage	Current into the ACIN, BAT1, or BAT2 pins from 5.4 V - 24 V (when pin is below, at, or above 6-V internal protection switch.)			0.1	µA
V_{REF_PP}	VREF_ACIN_rising - Internal reference voltage	Rising voltage at ACIN pin, makes ACSWONZ trigger low	1.2365	1.25	1.2645	V
V_{HYST_PP}	VHYST_ACIN_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_ACIN at ACIN pin, makes ACSWONZ trigger high		125		mV

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF_PP}	VREF_BAT1_rising - Internal reference voltage	Rising voltage at BAT1 pin, makes BAT1SWONZ trigger low	1.2365	1.25	1.2645	V
V_{HYST_PP}	VHYST_BAT1_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_BAT1 at BAT1 pin, makes BAT1SWONZ trigger high		125		mV
V_{REF_PP}	VREF_BAT2_rising - Internal reference voltage	Rising voltage at BAT2 pin, makes BAT2SWONZ trigger low	1.2365	1.25	1.2645	V
V_{HYST_PP}	VHYST_BAT2_falling - Internal hysteresis voltage	Falling voltage with respect to VREF_BAT2 at BAT1 pin, makes BAT2SWONZ trigger high		125		mV
	Critical supply voltage (VDCSNS) falling threshold	Critical supply voltage threshold register value VDLMTCRT[3:0]: 0100, Supply voltage decreasing. With 2S resistor divider from VDC to VDCSNS with 4R top, R bottom. VDC = 6 V when VDCSNS pin = 1.12 V.	1.10	1.12	1.14	V
	Critical supply voltage (VDCSNS) rising threshold hysteresis	Critical supply voltage hysteresis, Supply voltage increasing. With 2S resistor divider from VDC to VDCSNS with 4R top, R bottom. VDC_hyst = 100 mV when VDCSNS_hyst pin = 20 mV.		20		mV
	Critical supply voltage (VDCSNS) input current	VDCSNS = 1.2 V - 1.75 V		0.01	0.1	µA
INTERNAL RAMP COMPARATOR						
	Vramp_comp_VIN_rising	Rising voltage at VIN pin, makes internal ramp compensation of all controllers slightly smaller	10.5	11	11.5	V
	Vramp_comp_VIN_falling_hyst	Falling voltage hysteresis at VIN pin, makes the internal ramp compensation of all controllers slightly bigger		1.1		V
AC-ADAPTER DETECTION						
V_{IL}	ACOK input low voltage				0.4	V
V_{IH}	ACOK input high voltage		1.2			V
	ACOK input current	ACOK = 3.3 V		0.01	0.1	µA
	Adapter detection debounce time	ACOKDB register value: 00	50	61	95	µs
	Adapter detection debounce time	ACOKDB register value: 01	7	10	13	ms
	Adapter detection debounce time	ACOKDB register value: 10	15	20	25	ms
	Adapter detection debounce time	ACOKDB register value: 11 default	24	30	36	ms
EMERGENCY RESET SHUTDOWN Types with Time to shutdown						
$t_{UVLO\_shutdown}$	UVLO low shutdown time	Time from VIN < UVLO5 low threshold until shut down.			1	µs
$t_{SHUTDOWNZ\_shutdown}$	SHUTDOWNZ low shutdown time	Time from SHUTDOWNZ pin falling-edge until shut down.			1	µs
$t_{PWRBTNIN\_shutdown}$	PWRBTNIN low shutdown time	Time from PWRBTNIN pin falling-edge until shut down.			n/a	µs
$t_{PWRGD\_Fault\_shutdown}$	PWRGD Fault shutdown time	Time from PWRGD Fault detected including deglitch time until shut down. Output voltage is overvoltage or undervoltage	27	30	33	µs
$t_{CRIT\_Temp\_shutdown}$	CRITICAL Temperature high shutdown time	Time from $T_J > T_{CRIT\_Temp}$ including deglitch time until shut down. [Deglitch time can be changed from 5 µs to 300 µs]			5	µs
$t_{SDWNCTRL\_bit\_shutdown}$	SDWNCTRL bit set to 1 shutdown time	Time from SDWNCTRL register (0x49) bit 0 set to 1 until shut down. Time after SDWNCTRL register is written to by I^2C.			1	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REGULATORS					
VR1 Controller POWER					
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
V1.00A Output voltage	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V100ACNT[7:4] = 4'b0000))		1.05		V
V1.00A Output voltage - Default	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V100ACNT[7:4] = 4'b0001)) (Default)		1.00		V
V1.00A Output voltage	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V100ACNT[7:4] = 4'b0010))		0.975		V
V1.00A Output voltage	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V100ACNT[7:4] = 4'b0011))		0.950		V
V1.00A Output voltage	Power save mode enabled, ((STANDBYZ (SLP_S0#) = L) and (V100ACNT[7:4] = 4'b01XX))		0.850		V
Output voltage	Power save mode enabled, ((STANDBYZ (SLP_S0#) = L) and (V100ACNT[7:4] = 4'b10XX))		0.900		V
V1.00A Output voltage	Power save mode enabled, ((STANDBYZ (SLP_S0#) = L) and (V100ACNT[7:4] = 4'b11XX))		0.950		V
Current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	-30	-25	-20	mV
	V_{TRIP} = 0.8 V	-105	-100	-95	mV
	V_{TRIP} = 2 V	-260	-250	-240	mV
Negative current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	20	25	30	mV
	V_{TRIP} = 0.8 V	95	100	105	mV
	V_{TRIP} = 2 V	240	250	260	mV
I_{LIM} - Current limit pin source current	T_A = 25℃	45	50	55	µA
TC_{ILIM} - External FET Rdson current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - Current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
Maximum line regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, $I_{OUT} = I_{MAX}$ = 6.810 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR1P - FBVR1N).	-0.5%		0.5%	
Maximum load regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 7.4 V, I_{OUT} = 0 A to I_{MAX} = 6.810 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR1P - FBVR1N).	-0.5%		0.61%	
Maximum total output voltage load transient variation with respect to nominal Vout	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, I_{OUT} = 0 A to 70% max load, 70% max load to 0 mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5 A/µs	-5%		5%	

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching frequency (7.4 V)	PWM Mode (NVDC# = 3.3 V = programmed to low switching frequency)	379	500	550	kHz
	PWM Mode (NVDC# = GND = programmed to high switching frequency)	715	800	865	kHz
Soft-Start total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal)	770	876	1000	µs
Soft-Start delay time	Delay time from enable to first switching pulse.	120	136	150	µs
Soft-Start ramp-up time	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).	650	740	850	µs
DVS total fall time (delay time + output ramp-down time)	Time to start switching from enable to 5% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for falling edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from High to Low, until the output voltage begins to fall.	1	1.25	1.5	µs
DVS ramp time for falling edge	From first switching pulse to 5% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
DVS slew rate for falling edge	DVS falling edge slew rate for V_{VOUT} to change from the upper target to the lower target after STANDBYZ (SLP_S0#) changes from High to Low. Total ramp time = ((Vout_high - Vout_low) / slew_rate)	4.5	5	5.5	mV / µs
DVS total rise time (delay time + output ramp-rise time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for rising edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	1	1.25	1.5	µs
DVS ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
DVS slew rate for rising edge	DVS rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High. Total ramp time = ((Vout_high - Vout_low) / slew_rate)	4.5	5	5.5	mV / µs
Decay exit Total turn-on time (delay time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	69	79	99	µs
Decay exit delay time for rising edge	Decay delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	10	12	16	µs
Decay exit ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - 0 V) / slew_rate). For Vout target = 1.00 V.	59	67	83	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Decay exit slew rate for rising edge	Decay rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High . Total ramp time = ((Vout_high - 0 V) / slew_rate).	12	15	17	mV / µs
VR1 Controller MOSFET Drivers					
DRVH resistance	Source, IDRVH = -50 mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50 mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50 mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50 mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on	65	80	105	ns
High-side driver minimum off-time	DRVH - off	235	260	285	ns
VR1 Controller OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	125	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω
Output auto discharge resistance, Default	Discharge register value: 11	450	550	690	Ω
VR1_Controller Feedback input resistance	Controller enabled		1	2.25	MΩ
VR1_Bootstrap switch ON resistance (Rdson)	$-40 \le T_A \le 125°C$		15	25	Ω
VR1 Controller CONTROL					
VR1_Powergood exit threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR1_Powergood threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR1_Powergood exit threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR1_Powergood threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
VR1_Powergood deglitch time for both rising and falling edges	FBVR1P voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBVR1P into or out of powergood threshold, until PGVR1 toggles, for both rising and falling edges.	27	30	33	µs
VR1_Powergood Mask time during and after soft-start ramp-up time	Powergood is kept low and power fault is masked during soft-start until 100 µs after the internal reference has stepped up to the final voltage setting.	9	10	11	ms
VR1_Powergood Mask time during DVS ramp down (enter DVS)	Powergood is kept high and masked during DVS enter, ramp down, and until 100 µs after the internal reference has stepped down to the final voltage setting.	ramp-down + 90	ramp-down + 100	ramp-down + 110	µs
VR1_Powergood Mask time during DVS ramp up (exit DVS)	Powergood is kept high and masked during DVS exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	ramp-up + 90	ramp-up + 100	ramp-up + 110	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VR1_Force PWM time (deglitch time) during CCM to DCM transition	PWM is forced for 16 switching cycles before PFM is enabled turning off the low-side power MOSFET. Low-side FET current during each cycle must fall below the PFM current comparator valley threshold. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	16	16	16	cycles
VR1_Force PWM time during DVS ramp down (enter DVS)	PWM is forced during DVS enter, ramp down, and until 10 µs after the internal reference has stepped down to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-down + 9	ramp-down + 10	ramp-down + 11	µs
VR1_Force PWM time during DVS ramp up (exit DVS)	PWM is forced during DVS exit, ramp up, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-up + 9	ramp-up + 10	ramp-up + 11	µs
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
VR2 Converter POWER					
V_{VINVR2} power input voltage - Parametric and functional	V_{VINVR2} voltage range, V_{VIN} = 5.4 V to 21 V	3.135	3.3	3.465	V
V_{VINVR2} power input voltage - Functional	V_{VINVR2} voltage range, V_{VIN} = 5.4 V to 24 V	2.97	3.3	3.63	V
Output voltage	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V18ACNT[7:4] = 4'b0000))		1.854		V
Output voltage	Power save mode disabled (STANDBYZ ((SLP_S0#) = X) and (V18ACNT[7:4] = 4'b0001))		1.836		V
Output voltage - Default	Power save mode disabled (STANDBYZ ((SLP_S0#) X) and (V18ACNT[7:4] = 4'b0010)) (DEFAULT)		1.8		V
Output voltage	Power save mode disabled ((STANDBYZ (SLP_S0#) = X) and (V18ACNT[7:4] = 4'b0011))		1.764		V
Output voltage	Power save mode enabled, (STANDBYZ (SLP_S0#) = L) and (V18ACNT[7:4] = 4'b01XX))		1.728		V
Output voltage	Power save mode enabled, ((STANDBYZ (SLP_S0#) = L) and (V18ACNT[7:4] = 4'b10XX))		1.746		V
Output voltage	Power save mode enabled, ((STANDBYZ (SLP_S0#) = L) and (V18ACNT[7:4] = 4'b11XX))		1.764		V
Maximum average output current range	V_{VINVR2} = 2.97 V to 3.63 V	2500			mA
Ripple current range	V_{VINVR2} = 2.97 V to 3.63 V	325		1110	mA
Low side valley cycle by cycle positive current limit	V_{VINVR2} = 2.97 V to 3.63 V	2260		3360	mA
Low side valley cycle by cycle negative current limit	V_{VINVR2} = 2.97 V to 3.63 V	1400		1875	mA
PFM valley current threshold	V_{VINVR2} = 2.97 V to 3.63 V	90		125	mA
High side switch on resistance	V_{VINVR2} = 3.3 V, 100% duty cycle	30		105	mΩ

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low side switch on resistance	V_{VINVR2} = 3.3 V, 0% duty cycle	30		95	mΩ
Maximum line regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VINVR2} = 2.97 V to 3.63 V, I_{OUT} = Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.5%		0.5%	
Maximum load regulation - PWM Mode with respect to nominal Vout	ULQ/Auto Mode, V_{VINVR2} = 2.97 V to 3.63 V, I_{OUT} = 0 A to Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.5%		0.5%	
Maximum load regulation - AUTO Mode with respect to nominal Vout	ULQ/Auto Mode, V_{VINVR2} = 2.97 V to 3.63 V, I_{OUT} = 0 A to Imax, ALL VOUTS, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-0.65%		1.0%	
Maximum total output voltage load transient variation	DC and AC, ULQ/Auto Mode, V_{VINVR2} = 2.97 V to 3.63 V, I_{OUT} = 0 A to 70% max load, 70% max load to 0 mA, di/dt = 2.5 A/µs, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-5%		5%	
	DC and AC, ULQ/Auto Mode, V_{VINVR2} = 2.97 V to 3.63 V, I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5 A/µs, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR2P - FBVR2N).	-5%		5%	
Switching frequency	PWM Mode, I_{OUT} = 67% of max output current	1700	2000	2300	kHz
Soft-Start total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	730	800	1050	µs
Soft-Start delay time	Delay time from enable to first switching pulse.	120	135	150	µs
Soft-Start ramp-up time	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).	610	665	900	µs
DVS total fall time (delay time + output ramp-down time)	Time to start switching from enable to 5% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for falling edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from High to Low, until the output voltage begins to fall.	1	1.25	1.5	µs
DVS ramp time for falling edge	From first switching pulse to 5% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DVS slew rate for falling edge	DVS falling edge slew rate for V_{VOUT} to change from the upper target to the lower target after STANDBYZ (SLP_S0#) changes from High to Low. Total ramp time = ((Vout_high - Vout_low) / slew_rate)	4.5	5	5.5	mV / µs
DVS total rise time (delay time + output ramp-rise time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for rising edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	1	1.25	1.5	µs
DVS ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
DVS slew rate for rising edge	DVS rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High. Total ramp time = ((Vout_high - Vout_low) / slew_rate).	4.5	5	5.5	mV / µs
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 00, Default	250	860	1450	kΩ
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 01	80	100	120	Ω
Output auto discharge resistance	Discharge register value DISCHGCNT3[7:6]: 10	160	200	240	Ω
Output auto discharge resistance, Default	Discharge register value DISCHGCNT3[7:6]: 11	400	500	600	Ω
Feedback input resistance	Enabled			3	MΩ
Quiescent current associated with converter when enabled	I_{Vout} = 0 mA, enabled, at T_A = 25°C Not switching, Measured at LDO3V, VREGVR2		30	55	µA
VR2 Converter CONTROL					
Powergood exit threshold high	Fail when Vout increasing	106%	108%	110%	
Powergood threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
Powergood exit threshold low	Fail when Vout decreasing	90%	92%	94%	
Powergood threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
VR2_Powergood deglitch time for both rising and falling edges	FBVR2P voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBVR2P into or out of powergood threshold, until PGVR2 toggles, for both rising and falling edges.	27	30	33	µs
VR2_Powergood Mask time during and after soft-start ramp-up time	Powergood is kept low and power fault is masked during soft-start until 100 µs after the internal reference has stepped up to the final voltage setting.	9	10	11	ms
VR2_Powergood Mask time during DVS ramp down (enter DVS)	Powergood is kept high and masked during DVS enter, ramp down, and until 100 µs after the internal reference has stepped down to the final voltage setting.	ramp-down + 90	ramp-down + 100	ramp-down + 110	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VR2_Powergood Mask time during DVS ramp up (exit DVS)	Powergood is kept high and masked during DVS exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	ramp-up + 90	ramp-up + 100	ramp-up + 110	µs
	VR2_Force PWM time during DVS ramp down (enter DVS)	PWM is forced during DVS enter, ramp down, and until 10 µs after the internal reference has stepped down to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-down + 9	ramp-down + 10	ramp-down + 11	µs
	VR2_Force PWM time during DVS ramp up (exit DVS)	PWM is forced during DVS exit, ramp up, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-up + 9	ramp-up + 10	ramp-up + 11	µs
	Over temperature protection THOT		120		140	°C
	Over temperature hysteresis THOT			10		°C
	Over temperature protection TSHUT		130		160	°C
	Over temperature hysteresis TSHUT			10		°C
VR3 Controller POWER						
	Input voltage	Parametric and functional	5.4	7.4	21	V
	Input voltage	Functional	5.4	7.4	24	V
	Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b00)		3.399		V
	Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b01)		3.366		V
	Output voltage - Default	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b10) (DEFAULT)		3.3		V
	Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V33ADSWCNT[7:6] = 2'b00, V33ADSWCNT[5:4] = 2'b11)		3.234		V
	Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = STANDBYZ = L, V33ADSWCNT[7:4] = 4'b01XX		3.168		V
	Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = STANDBYZ = L, V33ADSWCNT[7:4] = 4'b10XX		3.201		V
	Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = L, V33ADSWCNT[7:4] = 4'b11XX		3.234		V
	Current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	-30	-25	-20	mV
		V_{TRIP} = 0.8 V	-105	-100	-95	mV
		V_{TRIP} = 2 V	-260	-250	-240	mV

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Negative current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	20	25	30	mV
	V_{TRIP} = 0.8 V	95	100	105	mV
	V_{TRIP} = 2 V	240	250	260	mV
High-side I_{LIM} - current limit pin source current	T_A = 25℃	44	50	56	µA
High-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		3300		ppm/℃
High-side V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
Low-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
Maximum range low side zero crossing threshold		-10		10	mV
Maximum line regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, $I_{OUT} = I_{MAX}$, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-0.5%		0.65%	
Maximum load regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 7.4 V, I_{OUT} = 0 A to I_{MAX} , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-0.5%		0.55%	
Maximum total output voltage load transient variation with respect to nominal Vout	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, I_{OUT} = 0 A to 70% max load, 70% max load to 0 mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5 A/µs, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR3P - FBVR3N).	-5%		5%	
VR3_Controller switching frequency	PWM Mode (NVDC# = 3.3 V) (TPS650830, TPS650832)	715	800	865	kHz
VR3_Controller switching frequency	PWM Mode (NVDC# = 3.3 V = programmed to low switching frequency)	430	500	550	kHz
	PWM Mode (NVDC# = GND = programmed to high switching frequency)	715	800	865	
Soft-Start delay time	Delay time from enable to first switching pulse.		16		ms
Soft-Start ramp-up time	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).	650	740	1050	µs
DVS total fall time (delay time + output ramp-down time)	Time to start switching from enable to 5% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for falling edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from High to Low, until the output voltage begins to fall.	1	1.25	1.5	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DVS ramp time for falling edge	From first switching pulse to 5% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
DVS slew rate for falling edge	DVS falling edge slew rate for V_{VOUT} to change from the upper target to the lower target after STANDBYZ (SLP_S0#) changes from High to Low. Total ramp time = ((Vout_high - Vout_low) / slew_rate)	4.5	5	5.5	mV / µs
DVS total rise time (delay time + output ramp-rise time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for rising edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	1	1.25	1.5	µs
DVS ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
DVS slew rate for rising edge	DVS rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High. Total ramp time = ((Vout_high - Vout_low) / slew_rate).	4.5	5	5.5	mV / µs
Decay exit Total turn-on time (delay time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	66	75	95	µs
Decay exit delay time for rising edge	Decay delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	10	12	16	µs
Decay exit ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - 0V) / slew_rate). For Vout target = 0.95.	56	63	79	µs
Decay exit slew rate for rising edge	Decay rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High. Total ramp time = ((Vout_high - 0 V) / slew_rate).	12	15	17	mV / µs
VR3 Controller MOSFET Drivers					
DRVH resistance	Source, IDRVH = -50 mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50 mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50 mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50 mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on	65	80	105	ns
High-side driver minimum off-time	DRVH - off	235	260	285	ns
VR3 Controller OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	125	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output auto discharge resistance, Default	Discharge register value: 11	450	550	690	Ω
VR3_Controller feedback input resistance	Controller enabled		1	2.25	MΩ
VR3_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
VR3_Controller HSD leakage	V_{IN} = 7.4 V, Controller disabled			1.55	µA
VR3 Controller CONTROL					
VR3_Powergood exit threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR3_Powergood threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR3_Powergood exit threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR3_Powergood threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
VR3_Powergood deglitch time for both rising and falling edges	FBVR3P voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBVR3P into or out of powergood threshold, until PGVR3 toggles, for both rising and falling edges.	27	30	33	µs
VR3_Powergood Mask time during and after soft-start ramp-up time	Powergood is kept low and power fault is masked during soft-start until 100 µs after the internal reference has stepped up to the final voltage setting.	9	10	11	ms
VR3_Powergood Mask time during DVS ramp down (enter DVS)	Powergood is kept high and masked during DVS enter, ramp down, and until 100 µs after the internal reference has stepped down to the final voltage setting.	ramp-down + 90	ramp-down + 100	ramp-down + 110	µs
VR3_Powergood Mask time during DVS ramp up (exit DVS)	Powergood is kept high and masked during DVS exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	ramp-up + 90	ramp-up + 100	ramp-up + 110	µs
VR3_Powergood Mask time during Decay	Powergood is kept high and masked during Decay enter, during decay, exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	decay + 180	decay+ 200	decay + 220	µs
VR3_Force PWM time (deglitch time) during CCM to DCM transition	PWM is forced for 16 switching cycles before PFM is enabled turning off the low-side power MOSFET. Low-side FET current during each cycle must fall below the PFM current comparator valley threshold. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	16	16	16	cycles
VR3_Force PWM time during DVS ramp down (enter DVS)	PWM is forced during DVS enter, ramp down, and until 10 µs after the internal reference has stepped down to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-down + 9	ramp-down + 10	ramp-down + 11	µs
VR3_Force PWM time during DVS ramp up (exit DVS)	PWM is forced during DVS exit, ramp up, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-up + 9	ramp-up + 10	ramp-up + 11	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VR3_Powergood Mask time during Decay ramp up (exit Decay)	PWM is forced for 30 µs starting 80 µs after DVS exit, This includes the last 20 µs of the final ramp up steps, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	27	30	33	µs
Overtemperature protection		130	145	160	°C
Overtemperature hysteresis			10		°C
VR4 Controller POWER					
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b000 DDRID = 0 V		1.236		V
Output voltage	Power save mode disabled, Output voltage select registerV1P2UCNT[6:4] = 3'b001 DDRID = 0 V		1.224		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b010 DDRID = 0 V		1.212		V
Output voltage	Power save mode disabled, Output voltage select registerV1P2UCNT[6:4] = 3'b011, default DDRID = 0 V		1.200		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b100 DDRID = 0 V		1.188		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b101 DDRID = 0 V		1.176		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b110 DDRID = 0 V		1.164		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b111 DDRID = 0 V		1.152		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b000 DDRID = 3.3 V		1.391		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b001 DDRID = 3.3 V		1.377		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b010 DDRID = 3.3 V		1.364		V

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b011 DDRID = 3.3 V		1.35		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b100, default DDRID = 3.3 V		1.337		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b101, default DDRID = 3.3 V		1.323		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b110 DDRID = 3.3 V		1.310		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b111 DDRID = 3.3 V		1.296		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b000 DDRID = Open		1.082		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b001 DDRID = Open		1.133		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b010 DDRID = Open		1.111		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b 011 DDRID = Open		1.1		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b100, default DDRID = Open		1.089		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b101, default DDRID = Open		1.078		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b110 DDRID = Open		1.067		V
Output voltage	Power save mode disabled, Output voltage select register V1P2UCNT[6:4] = 3'b111 DDRID = Open		1.056		V
Current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	-30	-25	-20	mV
	V_{TRIP} = 0.8 V	-105	-100	-95	mV
	V_{TRIP} = 2 V	-260	-250	-240	mV
Negative current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	20	25	30	mV
	V_{TRIP} = 0.8 V	95	100	105	mV
	V_{TRIP} = 2 V	240	250	260	mV

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
	Low-side TC_{LIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
	V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
	Maximum line regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, $I_{OUT} = I_{MAX}$ =7.5 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-0.5%		0.5%	
	Maximum load regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 7.4 V, I_{OUT} = 0 A to I_{MAX} =7.5 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-0.5%		0.65%	
	Maximum total output voltage load transient variation with respect to nominal Vout	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, I_{OUT} = 0 A to 70% max load, 70% max load to 0 mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5 A/µs , Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR4P - FBVR4N).	-5%		5%	
	Switching frequency	PWM Mode (NVDC# = 3.3 V = programmed to low switching frequency)	430	500	550	kHz
		PWM Mode (NVDC# = GND = programmed to high switching frequency)	715	800	865	
	Soft-Start delay time	Delay time from enable to first switching pulse.		4		ms
	Soft-Start ramp-up time	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).	650	740	850	µs
	DVS total fall time (delay time + output ramp-down time)	Time to start switching from enable to 5% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
	DVS delay time for falling edge	DVS delay time from when DDR_VTT_CTRL changes from High to Low, until the output voltage begins to fall.	1	1.25	1.5	µs
	DVS ramp time for falling edge	From first switching pulse to 5% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV	55	60	67	µs
	DVS slew rate for falling edge	DVS falling edge slew rate for V_{VOUT} to change from the upper target to the lower target after DDR_VTT_CTRL changes from High to Low. Total ramp time = ((Vout_high - Vout_low) / slew_rate)	4.5	5	5.5	mV / µs
	DVS total rise time (delay time + output ramp-rise time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
	DVS delay time for rising edge	DVS delay time from when DDR_VTT_CTRL changes from Low to High, until the output voltage begins to rise.	1	1.25	1.5	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DVS ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV.	55	60	67	µs
DVS slew rate for rising edge	DVS rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after DDR_VTT_CTRL changes from Low to High. Total ramp time = ((Vout_high - Vout_low) / slew_rate).	4.5	5	5.5	mV / µs
VR4 Controller MOSFET DRIVERS					
DRVH resistance	Source, IDRVH = -50 mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50 mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50 mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50 mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on	65	80	105	ns
High-side driver minimum off-time	DRVH - off	235	260	285	ns
VR4 Controller OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance, Default	Discharge register value: 01	90	100	160	Ω
Output auto discharge resistance	Discharge register value: 10	170	225	315	Ω
Output auto discharge resistance, Default	Discharge register value: 11	450	550	690	Ω
VR4_Controller feedback input resistance	VR4 controller enabled		1	2.25	MΩ
VR4_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
VR4 Controller CONTROL					
VR4_Powergood exit threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR4_Powergood threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR4_Powergood exit threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR4_Powergood threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
VR4_Powergood deglitch time for both rising and falling edges	FBVR4P voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBVR4P into or out of powergood threshold, until PGVR4 toggles, for both rising and falling edges.	27	30	33	µs
VR4_Powergood Mask time during and after soft-start ramp-up time	Powergood is kept low and power fault is masked during soft-start until 100 µs after the internal reference has stepped up to the final voltage setting.	9	10	11	ms
VR4_Powergood Mask time during DVS ramp down (enter DVS)	Powergood is kept high and masked during DVS enter, ramp down, and until 100 µs after the internal reference has stepped down to the final voltage setting.	ramp-down + 90	ramp-down + 100	ramp-down + 110	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VR4_Powergood Mask time during DVS ramp up (exit DVS)	Powergood is kept high and masked during DVS exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	ramp-up + 90	ramp-up + 100	ramp-up + 110	µs
	VR4_Force PWM time (deglitch time) during CCM to DCM transition	PWM is forced for 16 switching cycles before PFM is enabled turning off the low-side power MOSFET. Low-side FET current during each cycle must fall below the PFM current comparator valley threshold. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	16	16	16	cycles
	VR4_Force PWM time during DVS ramp down (enter DVS)	PWM is forced during DVS enter, ramp down, and until 10 µs after the internal reference has stepped down to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-down + 9	ramp-down + 10	ramp-down + 11	µs
	VR4_Force PWM time during DVS ramp up (exit DVS)	PWM is forced during DVS exit, ramp up, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-up + 9	ramp-up + 10	ramp-up + 11	µs
	Overtemperature protection		130	145	160	°C
	Overtemperature hysteresis			10		°C
LDO1 POWER						
	Input voltage	DDRID = 0 V		1.2		V
	Output voltage	DDRID = 0 V, VOUTLDO1 = (VINLDO1S) / 2		0.6		V
	Input voltage	DDRID = 3.3 V		1.35		V
	Output voltage	DDRID = 3.3 V, VOUTLDO1 = (VINLDO1S) / 2		0.675		V
	Input voltage	DDRID = Open		1.1		V
	Output voltage	DDRID = Open, VOUTLDO1 = (VINLDO1S)/ 2		0.55		V
	Output voltage tolerance - AC and DC transient load	I_{OUT} ≤ 10 mA, 1.1 V ≤ VINLDO1 ≤ 1.35 V, (FBLDO1 - FBVR4N) = Output voltage relative to (VINLDO1S - FBVR4N) / 2, where VINLDO1S connected to FBVR4P on the board, Load transient from 0mA to 70%*10 mA, dI/dt = 2.5 A/µs.	-20		20	mV
		I_{OUT} ≤ 1 A, 1.1 V ≤ VINLDO1 ≤ 1.35 V, (FBLDO1 - FBVR4N) = Output voltage relative to (VINLDO1S - FBVR4N) / 2, where VINLDO1S connected to FBVR4P on the board, Load transient from 0mA to 70%*1A, dI/dt = 2.5 A/µs.	-30		30	mV
	Leakage current	T_A = 25°C, VINLDO1 = 1.2 V, Disabled			5	µA
	Bias current at VIN13_SENSE	T_A = 25°C Bias current measured when VINLDO1S is at 1.2 V			40	µA
	Source current limit	Max current from LDO without exceeding load regulation	1000			mA
	Sink current limit	Max current sinked into LDO without exceeding load regulation (raise output voltage above programmed value to sink current into LDO)	1000			mA

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Source short circuit current limit	Measured with VOUT at 0.9*Programmed voltage	2000			mA
	Sink short circuit current limit		2000			mA
	Maximum load regulation with respect to nominal Vout	V_{VIN} = 1.1 V, 1.2 V and 1.35 V, I_{OUT} = 0 A to 1.0 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBLDO1 - FBVR4N) = Output voltage relative to (VINLDO1S - FBVR4N) / 2, where VINLDO1S connected to FBVR4P on the board.	-4.5%		4.5%	
	Maximum total output voltage variation with respect to nominal Vout	DC and AC, V_{VIN} = 1.0 V to 1.42 V, I_{OUT} = 0 A to 1.0 A, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBLDO1 - FBVR4N) = Output voltage relative to (VINLDO1S - FBVR4N) / 2, where VINLDO1S connected to FBVR4P on the board.	-5%		5%	
	Total turn-on time (enable + ramp)	Measure from LDO enable to V_{OUT} stable. time to ramp from 0.3 V to $V_{O(min)}$. Continuous slope (no slope reversal). Assumes V_{VIN} is present, with a 4 x 10-µF output capacitor bank (actual capacitance after derating).			35	µs
	External output capacitor (Cout)	Minimum actual capacitance after derating	40			µF
	External input capacitor (Cin)	Minimum actual capacitance after derating	10			µF
	Output auto discharge resistance	Discharge register value: 0, Default	1000			kΩ
	Output auto discharge resistance, Default	Discharge register value: 1	60	80	100	Ω
	FBLDO1 input impedance	Enabled	20	25		MΩ
	Quiescent current into $V_{VINLDO1}$	$V_{VINLDO1}$ = 1.35 V, I_{LDO1} = 0 mA, Enabled		3.5	5	µA
	Quiescent current from 3.3-V reference LDO when LDO1 is enabled	$V_{VINLDO1}$ = 1.35 V, Enabled			250	µA
LDO1 CONTROL						
	LDO1_Powergood threshold high	Fail when V_{OUT} increasing	108%	110%	112%	
	LDO1_Powergood threshold high hysteresis	Good when V_{OUT} decreases (after a PGOOD fail event)		-5%		
	LDO1_Powergood threshold low	Fail when V_{OUT} decreasing	88%	90%	92%	
	LDO1_Powergood threshold low hysteresis	Good when V_{OUT} increases (after a PGOOD fail event)		5%		
	LDO1_Powergood deglitch time for both rising and falling edges	FBLDO1 voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBLDO1 into or out of powergood threshold, until internal register bit toggles, for both rising and falling edges.	27	30	33	µs
	Overtemperature protection		130	145	160	°C
	Overtemperature hysteresis			10		°C
VR5 Controller POWER						

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	Parametric and functional	5.4	7.4	21	V
Input voltage	Functional	5.4	7.4	24	V
Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b00)		5.15		V
Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b01)		5.1		V
Output voltage- Default	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b10) (DEFAULT)		5.0		V
Output voltage	Power save mode disabled (STANDBYZ (SLP_S0#) = H, or STANDBYZ (SLP_S0#) = L, V5ADS3CNT[7:6] = 2'b00, V5ADS3CNT[5:4] = 2'b11)		4.9		V
Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = L , V5ADS3CNT[7:4] = 4'b01XX		4.8		V
Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = L , V5ADS3CNT[7:4] = 4'b10XX		4.85		V
Output voltage	Power save mode enabled, STANDBYZ (SLP_S0#) = L , V5ADS3CNT[7:4] = 4'b11XX		4.9		V
Current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	-30	-25	-20	mV
	V_{TRIP} = 0.8 V	-105	-100	-95	mV
	V_{TRIP} = 2 V	-260	-250	-240	mV
Negative current limit (Vsw - PGND)	V_{TRIP} = 0.2 V	20	25	30	mV
	V_{TRIP} = 0.8 V	95	100	105	mV
	V_{TRIP} = 2 V	240	250	260	mV
High-side I_{LIM} - current limit pin source current	T_A = 25℃	44	50	56	µA
High-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		3300		ppm/℃
High-side V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
I_{LIM} - current limit pin source current	T_A = 25℃	45	50	55	µA
Low-side TC_{ILIM} - current limit temperature coefficient	With respect to 25℃		4780		ppm/℃
V_{ILIM} - current limit pin setting voltage range	$V_{ILIM} = R_{TRIP} * I_{LIM}$ (usable voltage range across the operating temperature range)	0.2		2	V
Maximum range low side zero crossing threshold		-10		10	mV
Maximum line regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 5.4 V to 21 V, $I_{OUT} = I_{MAX}$, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-0.5%		1.05%	

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum load regulation with respect to nominal Vout	ULQ/Auto Mode, V_{VIN} = 7.4 V, I_{OUT} = 0 A to I_{MAX}, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-0.5%		0.75%	
Maximum total output voltage load transient variation with respect to nominal Vout	DC and AC, ULQ/Auto Mode, V_{VIN} = 5.7 V to 21 V (when Vout = 5 V), V_{VIN} = 5.4 V to 21 V (when Vout = 1.8 V), I_{OUT} = 0 A to 70% max load, 70% max load to 0 mA and I_{OUT} = 30% max load to max load, max load to 30% max load, di/dt = 2.5 A/µs, Measured at the regulation point output capacitor with Kelvin connections made directly from the regulation point to the differential feedback pins (FBVR5P - FBVR5N).	-5%		5%	
VR5_Controller switching frequency	PWM Mode (NVDC# = 3.3 V) (TPS650830, TPS650832)	25	875	925	kHz
VR5_Controller switching frequency	PWM Mode (NVDC# = 3.3 V = programmed to low switching frequency)	430	500	550	kHz
	PWM Mode (NVDC# = GND = programmed to high switching frequency) Frequency drops at Vin < 6 V close to Vout = 5 V to extend Ton.	25	875	925	
Soft-Start total turn-on time (start-up time + output ramp-up time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	770	875	1200	µs
Soft-Start delay time	Delay time from enable to first switching pulse.	120	135	150	µs
Soft-Start ramp-up time	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal).	650	740	1050	µs
DVS total fall time (delay time + output ramp-down time)	Time to start switching from enable to 5% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for falling edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from High to Low, until the output voltage begins to fall.	1	1.25	1.5	µs
DVS ramp time for falling edge	From first switching pulse to 5% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV.	55	60	67	µs
DVS slew rate for falling edge	DVS falling edge slew rate for V_{VOUT} to change from the upper target to the lower target after STANDBYZ (SLP_S0#) changes from High to Low. Total ramp time = ((Vout_high - Vout_low) / slew_rate).	4.5	5	5.5	mV / µs
DVS total rise time (delay time + output ramp-rise time)	Time to start switching from enable to 95% of VO(Min), Continuous slope (no slope reversal).	56	61.25	68.5	µs
DVS delay time for rising edge	DVS delay time from when STANDBYZ (SLP_S0#) changes from Low to High, until the output voltage begins to rise.	1	1.25	1.5	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DVS ramp time for rising edge	From first switching pulse to 95% of VO(Min), Continuous slope (no slope reversal). Total ramp time = ((Vout_high - Vout_low) / slew_rate). For Vout change = 300 mV.	55	60	67	µs
DVS slew rate for rising edge	DVS rising edge slew rate for V_{VOUT} to change from the lower target to the upper target after STANDBYZ (SLP_S0#) changes from Low to High . Total ramp time = ((Vout_high - Vout_low) / slew_rate).	4.5	5	5.5	mV / µs
VR5 Controller MOSFET Drivers					
DRVH resistance	Source, IDRVH = -50 mA		3.0	4.5	Ω
DRVH resistance	Sink, IDRVH = 50 mA		2.0	3.5	Ω
DRVL resistance	Source, IDRVL = -50 mA		3.0	4.5	Ω
DRVL resistance	Sink, IDRVL = 50 mA		0.8	2.0	Ω
Dead time	DRVH - off to DRVL - on		10		ns
Dead time	DRVL - off to DRVH - on		20		ns
High-side driver minimum on-time	DRVH - on	65	80	105	ns
High-side driver minimum off-time	DRVH - off	235	260	285	ns
VR5 Controller OUTPUT DISCHARGE					
Output auto discharge resistance	Discharge register value: 00, Default	1000			kΩ
Output auto discharge resistance	Discharge register value: 01	90	150	190	Ω
Output auto discharge resistance	Discharge register value: 10	170	250	315	Ω
Output auto discharge resistance	Discharge register value: 11	450	575	690	Ω
VR5_Controller Feedback input resistance	Controller enabled		2.5	4.25	MΩ
VR5_Bootstrap switch ON resistance (Rdson)	T_A = 25°C			20	Ω
VR5_Controller HSD leakage	V_{IN} = 7.4 V, Controller disabled			1.55	µA
VR5 Controller CONTROL					
VR5_Powergood exit threshold high	Fail when Vout increasing	105.5%	108%	110.5%	
VR5_Powergood threshold high hysteresis	Good when Vout decreases (after a PGOOD fail event)		-3%		
VR5_Powergood exit threshold low	Fail when Vout decreasing	89.5%	92%	94.5%	
VR5_Powergood threshold low hysteresis	Good when Vout increases (after a PGOOD fail event)		3%		
VR5_Powergood deglitch time for both rising and falling edges	FBVR5P voltage must cross powergood threshold and stay for at least this time to change powergood output state. Measured from FBVR5P into or out of powergood threshold, until PGVR5 toggles, for both rising and falling edges.	27	30	33	µs
VR5_Powergood Mask time during and after soft-start ramp-up time	Powergood is kept low and power fault is masked during soft-start until 100 µs after the internal reference has stepped up to the final voltage setting.	9	10	11	ms
VR5_Powergood Mask time during DVS ramp down (enter DVS)	Powergood is kept high and masked during DVS enter, ramp down, and until 100 µs after the internal reference has stepped down to the final voltage setting.	ramp-down + 90	ramp-down + 100	ramp-down + 110	µs

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VR5_Powergood Mask time during DVS ramp up (exit DVS)	Powergood is kept high and masked during DVS exit, ramp up, and until 100 µs after the internal reference has stepped up to the final voltage setting.	ramp-up + 90	ramp-up + 100	ramp-up + 110	µs
	VR5_Force PWM time (deglitch time) during CCM to DCM transition	PWM is forced for 16 switching cycles before PFM is enabled turning off the low-side power MOSFET. Low-side FET current during each cycle must fall below the PFM current comparator valley threshold. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	16	16	16	cycles
	VR5_Force PWM time during DVS ramp down (enter DVS)	PWM is forced during DVS enter, ramp down, and until 10 µs after the internal reference has stepped down to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-down + 9	ramp-down + 10	ramp-down + 11	µs
	VR5_Force PWM time during DVS ramp up (exit DVS)	PWM is forced during DVS exit, ramp up, and until 10 µs after the internal reference has stepped up to the final voltage setting. Forced PWM allows a fast transient response and smaller output voltage ripple during the transition.	ramp-up + 9	ramp-up + 10	ramp-up + 11	µs
	Overtemperature protection		130	145	160	°C
	Overtemperature hysteresis			10		°C
INPUT POWER SOURCE DETECTION						
POWER MONITORING 1-Hz CLOCK - 1-Hz EC CLOCK - pulledup to Internal Pull-up Rail = EC_VCC = 1.8 V or 3.3 V						
	Clock frequency (1)		0.8	1	1.2	Hz
	Duty cycle			50%		
V_{PP}	Pull-up output voltage supply	Pulled-Up to EC_VCC pin which should be tied to 3.3-V LDO3V pin, can also have EC_VCC pull-up to 1.8 V, instead of 3.3 V.		EC_VCC		V
V_{OL_PP}	Low level output voltage	I_{OL} = 3 mA			0.66	V
V_{OH_PP}	High level output voltage	I_{OH} = 3 mA	EC_VCC - 0.66			V
COINCELL SELECTOR						
V_{3v1LDO}	3V1 LDO regulation voltage	VDCIN > UVLO, 3.3-V and 5-V LDOs up, Measured at the V3P3A_RTC pin with respect to AGND. Place a 1-µF capacitor at V3P3A_RTC. (Do not exceed 2 µF actual capacitance).	3.0	3.1	3.2	V
I_{3v1LDO}	Maximum 3V1 LDO output current	Maximum output current out of 3V3RTC.			1	mA
$I_{Q\_bkup\_no\_Vsys}$	VBATTBKUP quiescent current, when no adapter and no main battery connected to system, automatically VBATTBKUP internally selected, internal 3.1-V LDO automatically off	V_{VDC} < UVLO, V_{BBC} = 2.0 V to 3.0 V, V_{VDC} = 0 V		0.03	0.45	µA
$I_{Q\_bkup\_with\_Vsys}$	VBATTBKUP quiescent current, when adapter or main battery connected to system, automatically VBATTBKUP internally not selected, internal 3.1-V LDO automatically on and selected.	V_{VDC} > UVLO, V_{BBC} = 2.0 V to 3.0 V, V_{VDC} = 7.4 V		0.15	0.85	µA

(1) All values referred to V_{IH} min and V_{IH} max levels.

Electrical Characteristics *(continued)*

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ext_bkup}	External resistor in series with backup battery	Place between backup battery and VBATTBKUP pin, for limiting current out of backup battery		1		kΩ
I2C INTERFACE						
V_{IL}	SDA, SCL input low voltage				0.4	V
V_{IH}	SDA, SCL input high voltage		1.2			V
	SDA, SCL input current	Clamped on 3.3 V		0.01	0.3	µA
	SDA output low voltage	I_{SDA} = 5 mA (using a 354 Ω or larger external pull-up resistor)		0.04	0.4	V
C_b	Capacitive load for SDA and SCL				400	pF

5.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C INTERFACE						
t_{I2C_Rdy}	Minimum time for I^2C to be ready after VIN > UVLO5V rising	Time after VIN rising above > $V_{UVLO\_5V\_Main}$ + $V_{Hys_5V_Main}$until OTP is loaded and I^2C is ready to communicate			1	ms
$f_{(SCL)}$	SCL clock frequency	Standard-mode			100	kHz
		Fast-mode			400	
		Fast-mode Plus			1000	
t_{BUF}	Bus free time between a STOP and START condition	Standard-mode	4.7			µs
		Fast-mode	1.3			
		Fast-mode Plus	0.5			
$t_{HD;\ STA}$	Hold time (repeated) START condition	Standard-mode	4			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns
$t_{SU;\ STA}$	Setup time for a repeated START condition	Standard-mode	4.7			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns
$t_{SU;\ DAT}$	Data setup time	Standard-mode	250			ns
		Fast-mode	100			
		Fast-mode Plus	50			
$t_{HD;\ DAT}$	Data hold time	Standard-mode	0		3.45	µs
		Fast-mode	0		0.9	µs
		Fast-mode Plus	0			ns
t_{rCL}	Rise time of SCL signal	Standard-mode			1000	ns
		Fast-mode	20		300	
		Fast-mode Plus			120	
t_{rDA}	Rise time of SDA signal	Standard-mode (using a 2.95 kΩ or smaller external pull-up resistor)			1000	ns
		Fast-mode (using an 885 Ω or smaller external pull-up resistor)	20		300	
		Fast-mode Plus (using a 354 Ω or smaller external pull-up resistor)			120	

Timing Requirements *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{fDA}	Fall time of SDA signal	Standard-mode			300	ns
		Fast-mode	20 x (V_{DD} / 5.5 V)		300	
		Fast-mode Plus	20 x (V_{DD} / 5.5 V)		120	
$t_{SU;\ STO}$	Setup time for STOP condition	Standard-mode	4			µs
		Fast-mode	600			ns
		Fast-mode Plus	260			ns

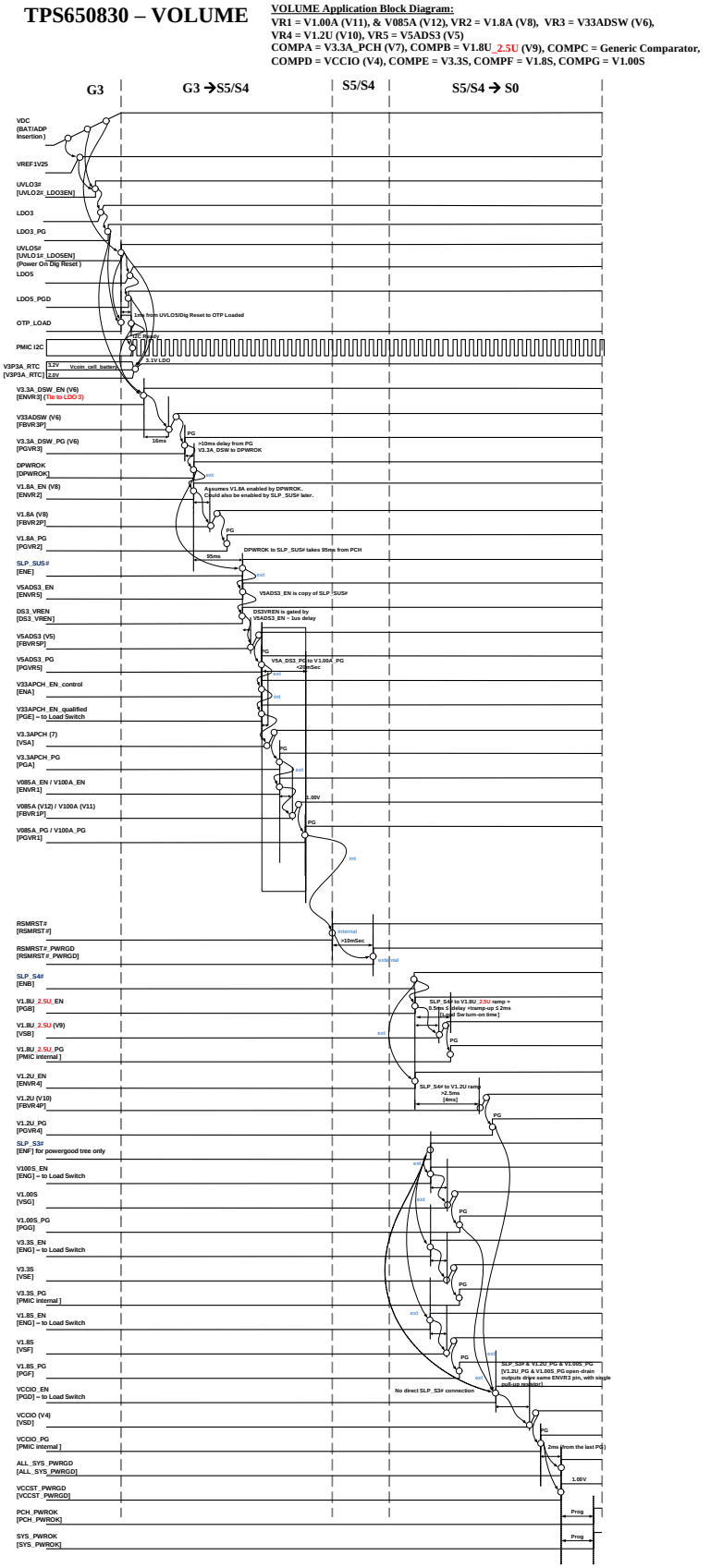


Figure 5-1. TPS650830 Volume Timing Diagram

5.7 Typical Characteristics

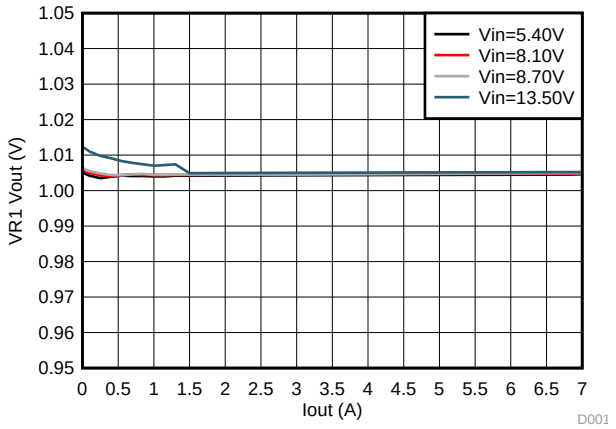


Figure 5-2. VR1 Output Voltage Load Regulation, NVDC

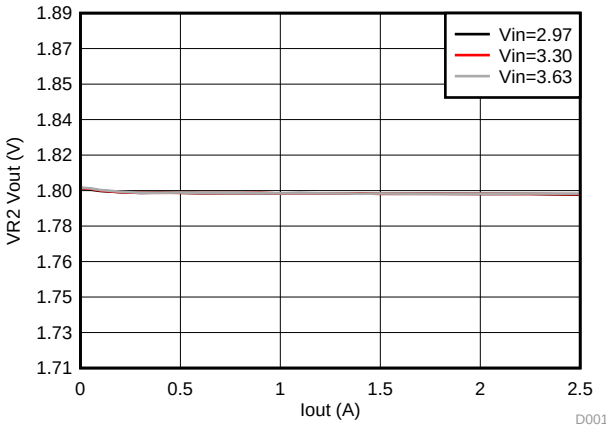


Figure 5-3. VR2 Output Voltage Load Regulation, NVDC

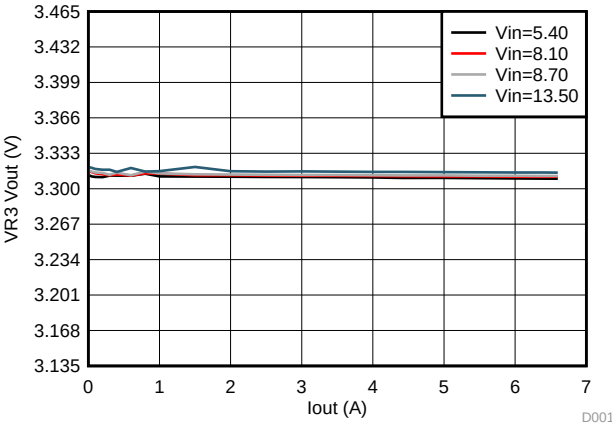


Figure 5-4. VR3 Output Voltage Load Regulation, NVDC

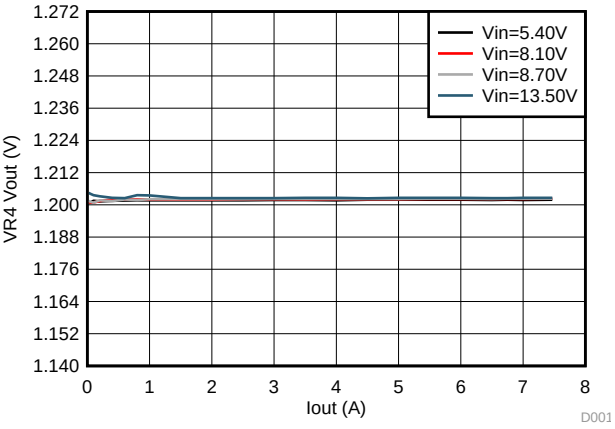


Figure 5-5. VR4 Output Voltage Load Regulation, NVDC

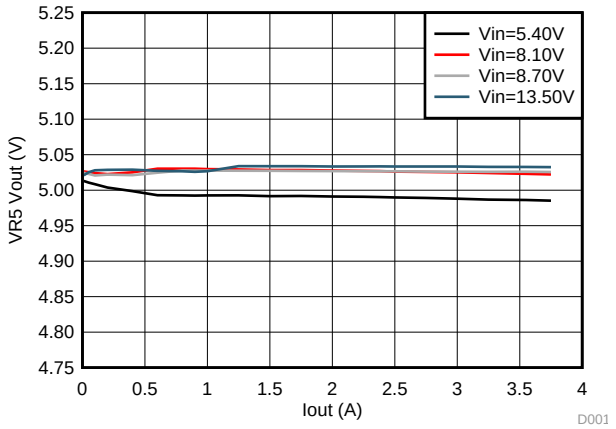


Figure 5-6. VR5 Output Voltage Load Regulation, NVDC

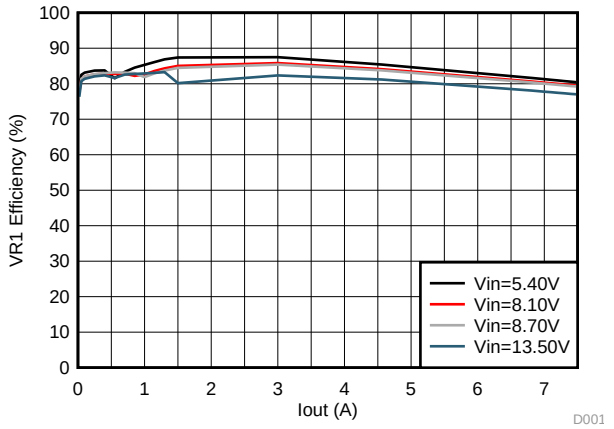


Figure 5-7. VR1 Efficiency vs Load, NVDC

Typical Characteristics *(continued)*

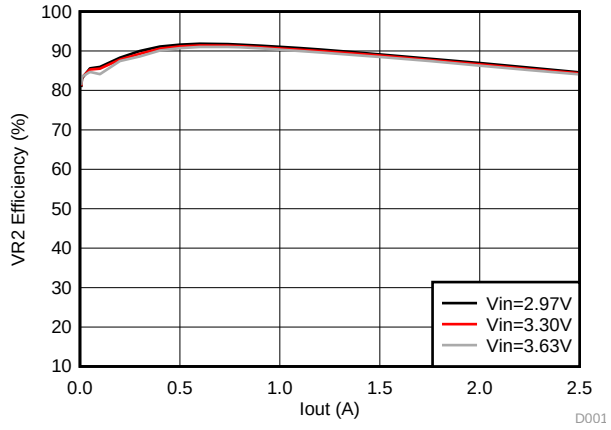


Figure 5-8. VR2 Efficiency vs Load, NVDC

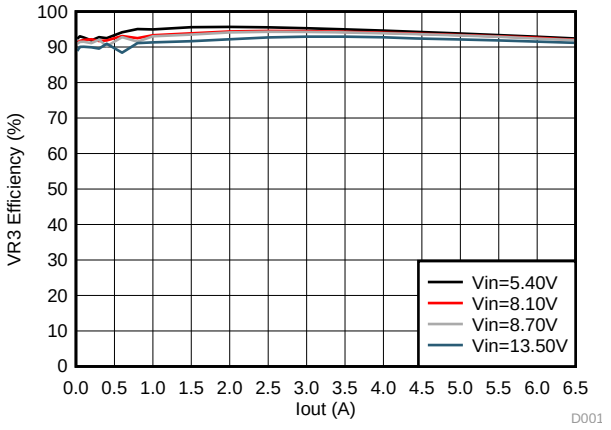


Figure 5-9. VR3 Efficiency vs Load, NVDC

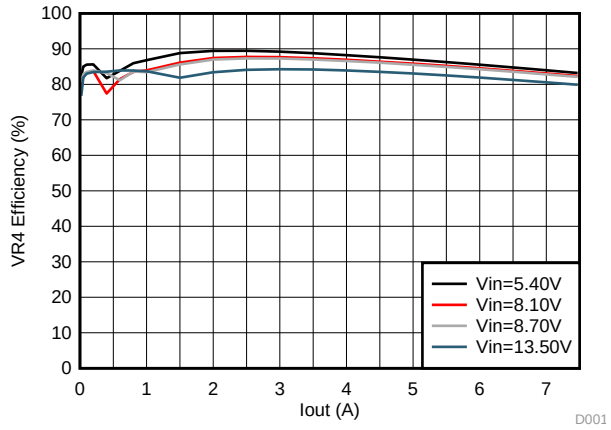


Figure 5-10. VR4 Efficiency vs Load, NVDC

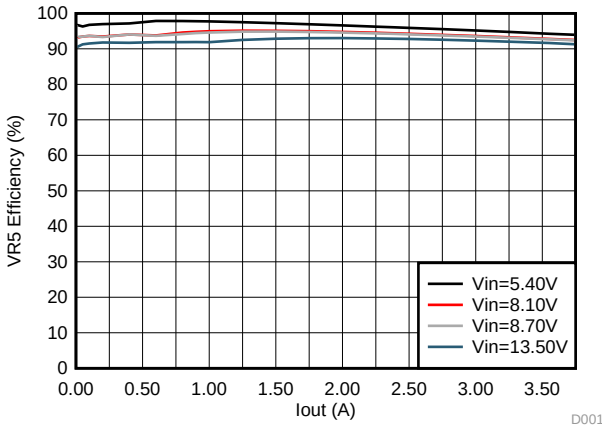


Figure 5-11. VR5 Efficiency vs Load, NVDC

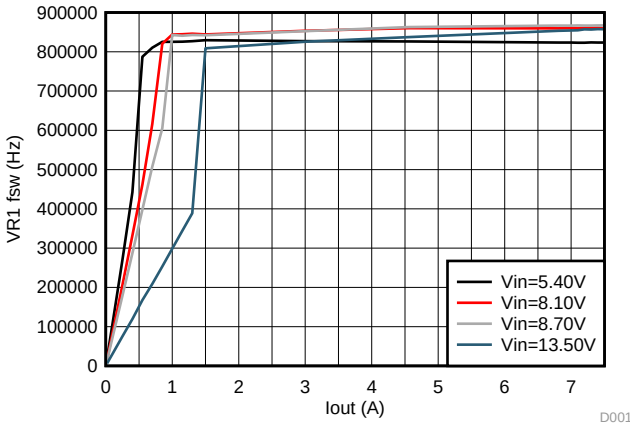


Figure 5-12. VR1 Switching Frequency vs Load, NVDC

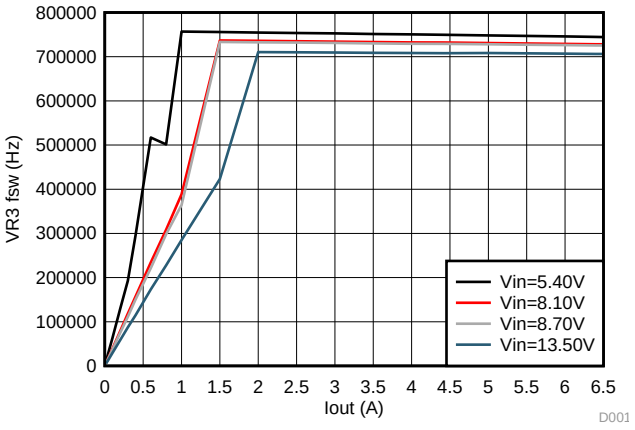


Figure 5-13. VR3 Switching Frequency vs Load, NVDC

Typical Characteristics *(continued)*

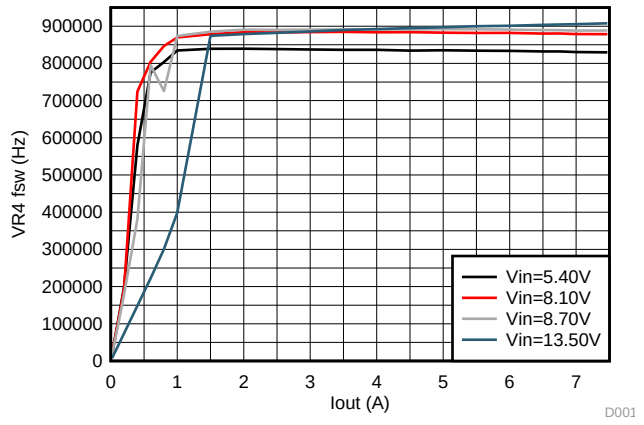


Figure 5-14. VR4 Switching Frequency vs Load, NVDC

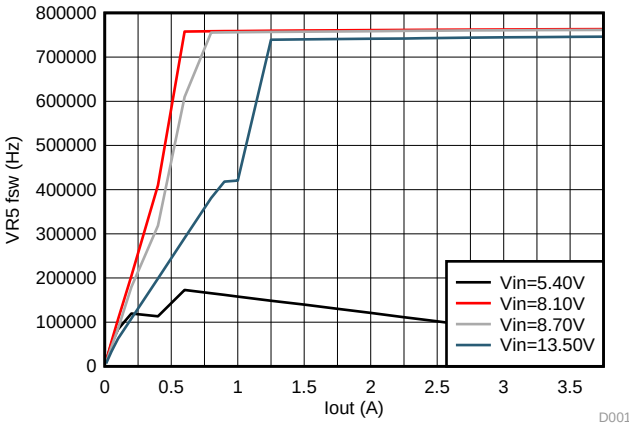


Figure 5-15. VR5 Switching Frequency vs Load, NVDC

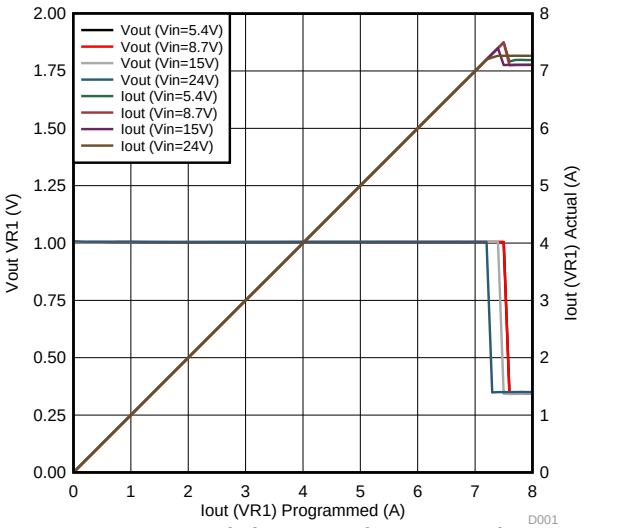


Figure 5-16. VR1 Current Limit: Vout and Iout vs Load, Non-NVDC

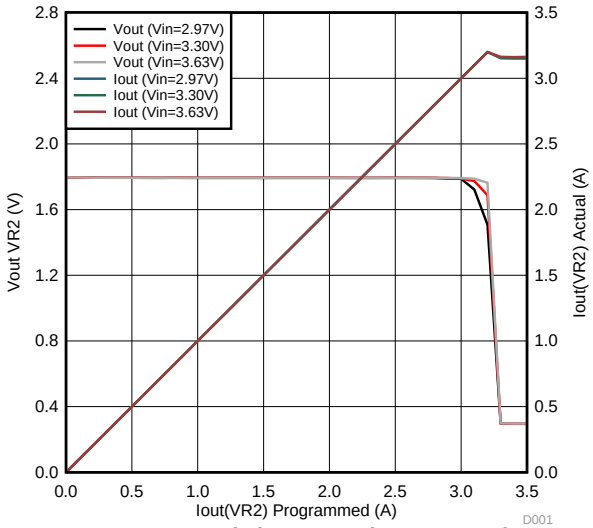


Figure 5-17. VR2 Current Limit: Vout and Iout vs Load, Non-NVDC

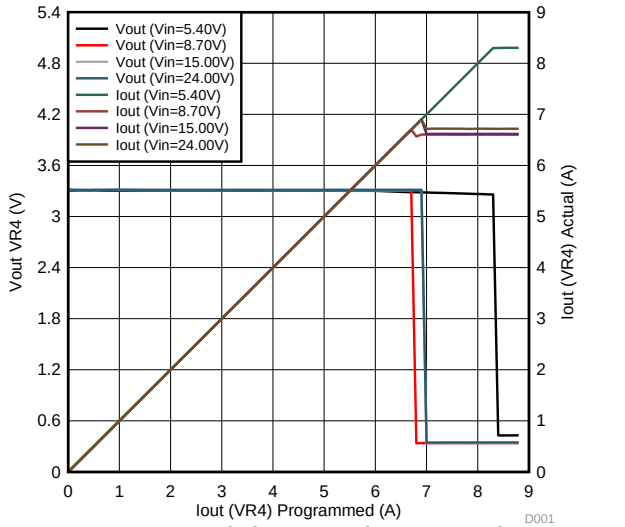


Figure 5-18. VR3 Current Limit: Vout and Iout vs Load, Non-NVDC

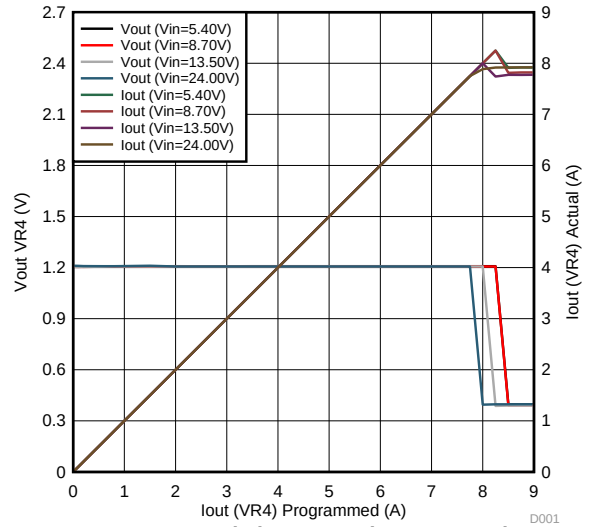


Figure 5-19. VR4 Current Limit: Vout and Iout vs Load, Non-NVDC

Typical Characteristics *(continued)*

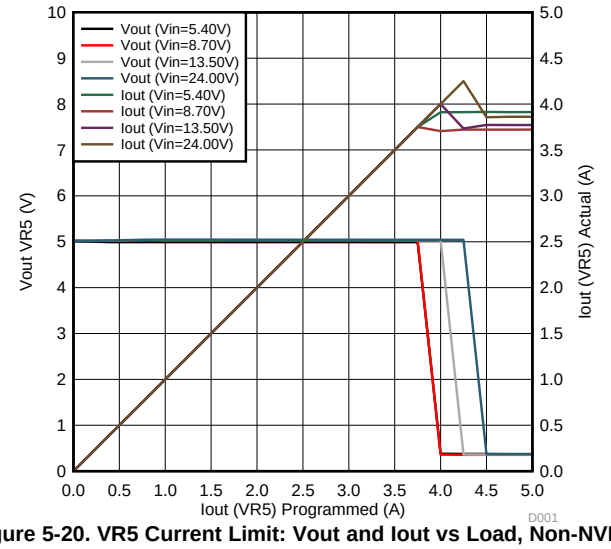
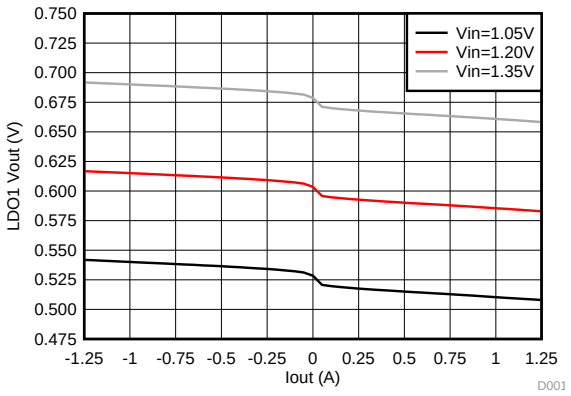


Figure 5-20. VR5 Current Limit: Vout and Iout vs Load, Non-NVDC



Positive current = sinking from load.
Negative current = sourcing to load.
Inherent droop reduces transient ripple response

Figure 5-21. LDO1 Load Regulation: Vout vs Iout

6 Detailed Description

6.1 Overview

The TPS650830 is a single-chip solution Power Management IC designed specifically for the latest Intel Processors targeted for Tablets, Ultrabooks, and Notebooks with NVDC or non-NVDC power architectures, using 2S, 3S, or 4S Lithium-Ion battery packs.

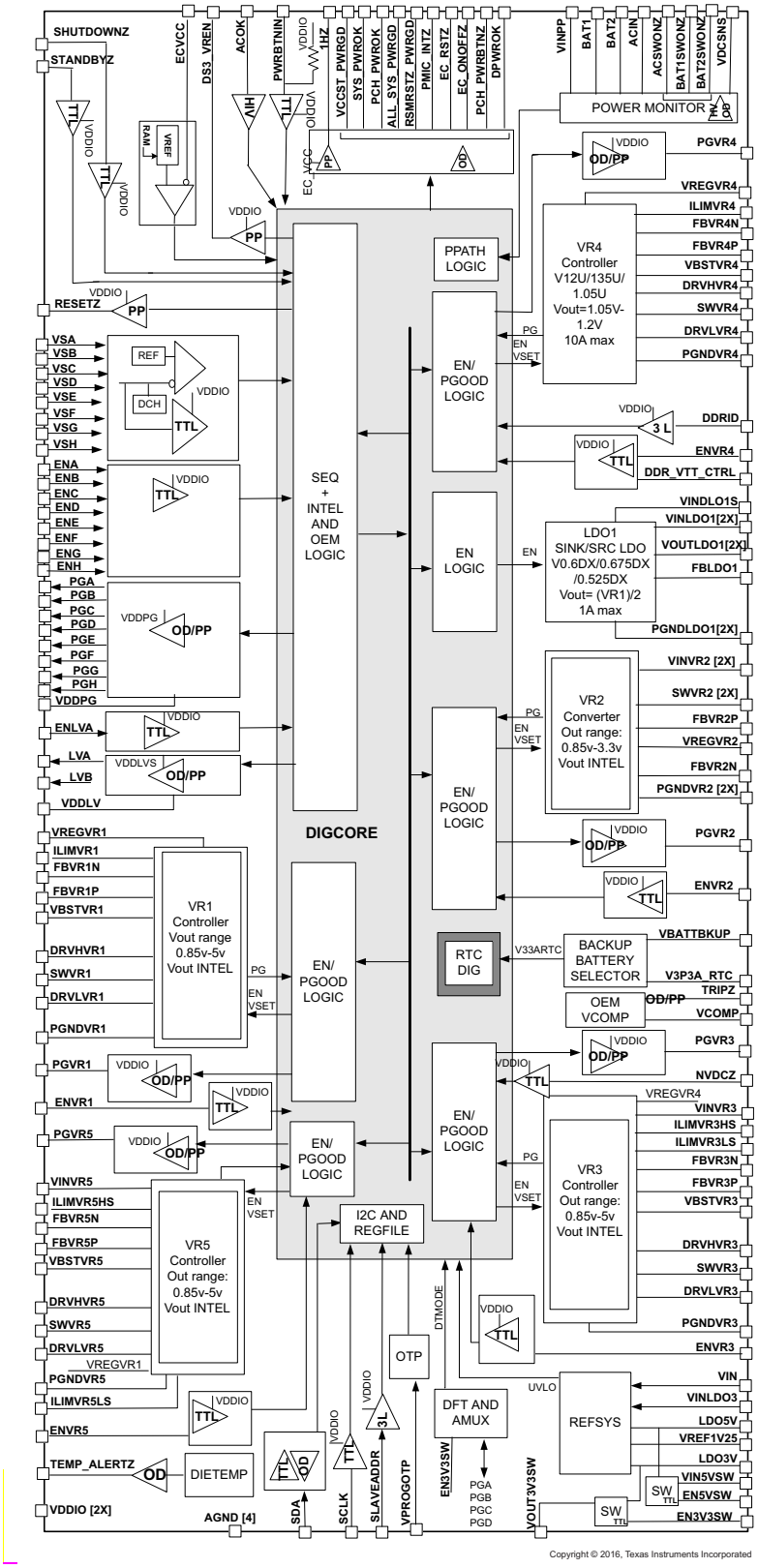
The TPS650830 is used for Volume systems with the low voltage rails merged for the smallest footprint and lowest cost system power solution.

The TPS650830 can provide the complete power solution based on the Intel Reference Designs. Five highly efficient step-down voltage regulators (VRs) and a sink/source LDO, are used along with power-up sequence logic managing external load switches to provide the proper power rails, sequencing, and protection - including DDR3 and DDR4 memory power. The regulators support dynamic voltage scaling (DVS) for maximum efficiency including Connected Standby. The high frequency voltage regulators use small inductors and capacitors to achieve a small solution size. Output power is adjustable on four VR controllers. An I^2C interface allows simple control by the embedded controller (EC). Each version is available in a 7x7 NFBGA package and a 9x9 NFBGA package. The 7x7 NFBGA package can be used in Type 4 PCB boards for the smallest area implementation. The 9x9 NFBGA package can be used in Type 3 and Type 4 PCB boards allowing to minimize cost and area.

The Powergood Comparator Logic allows controlling and monitoring up to eight external load switches within the sequence. All the VR and Load Switch Powergood signals are used in the Powergood Tree of which the outputs are shown with open-drain outputs. Enable inputs allow connecting externally to set the sequence, and it also allows using various Sleep Mode State signals. The STANDBYZ allows entering a Deep Sleep Mode, in which the out put voltages of the voltage regulators can be reduced to save power by DVS.

The Power Monitoring comparators are used to detect and monitor up to three input power sources (adapter, battery1, battery2, or any other combination). Over temperature of the PMIC self-protects, and outputs a Status output, TEMPALERTZ; plus there is a dedicated comparator that can monitor system over temperature with multiple stacked PTC thermistors, or an NTC thermistor. The PMIC automatically switches between an internal 3.1-V LDO when a power source is connected; or to a Backup Battery (Coin Cell) when all power sources are removed. This output RTC rail is used to maintain the always-on RTC rails for critical register data.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Voltage Regulator Assignment and Powergood Comparator Logic Assignment (External Voltage Regulator or Load Switch) for Skylake and Kabylake Platform

For the Skylake and Kabylake Power Map implementation, the five PMIC voltage regulators and LDO1 are assigned with the low -voltage rails merged or split according to the configuration. For the Volume (merged low voltage rails) configuration six external load switches are controlled and monitored by using six powergood comparator logic blocs.

Table 6-1. Voltage Regulator and Powergood Comparator Logic Assignment for Skylake and Kabylake Platforms

TPS650830	Skylake and Kabylake PLATFORM POWER SYSTEM VOLTAGE RAIL VOLUME (Merged Low Voltage Rails)	OUTPUT VOLTAGE, V_{out} DEFAULT, or COMPARATOR INPUT	SWITCHING FREQUENCY, F_{sw} NVDC# = 1 / 0	LPM VOLTAGE, V_{out} DEFAULT	POWER GOOD OUTPUT SETTING, (PGVRx or PGx is PP or OD)
VR1	V1.00A / V0.85A	1.00 V	500 kHz / 800 kHz	LPM = 1.00 V	PP
VR2	V1.8A	1.8 V	2 MHz / 2 MHz	LPM = 1.8 V	PP
VR3	V3.3A_DSW	3.3 V	800 kHz / 800 kHz	LPM = 3.3 V	PP
VR4	V1.2U	1.2 V,1.35 V,1.1 V	500 kHz / 800 kHz	LPM = 1.2 V,1.35 V,1.1 V	OD
VR5	V5A_DS3	5 V	800 kHz / 800 kHz	LPM = 5.0 V	PP
LDO1	V0.6Dx	0.6 V, 0.675 V, 0.55 V	-	LPM = DDR_VTT_CTRL = Off	NA
External VR_a	none	-	-	-	NA
External VR_b	none	-	-	-	NA
Powergood Comparator Logic a	V3.3A_PCH Enable/Sense External Load Switch	3.3 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic b	V1.8U_2.5U Enable/Sense External Load Switch	1.8 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic c	Generic Comparator	-	–	–	--
Powergood Comparator Logic d	VCCIO Enable/Sense External Load Switch	1.00 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic e	V3.3S Sense External Load Switch	3.3 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic f	V1.8S Sense External Load Switch	1.8 V, Comparator Analog Input	–	–	PP
Powergood Comparator Logic g	V1.0S Sense External Load Switch	1.00 V, Comparator Analog Input	–	–	OD

6.3.2 Generic Powergood Window Comparator with Open-Drain Output

The generic powergood comparator monitors the output voltage to ensure it is within ±10% of the nominal target voltage there is a 30-µs deglitch on both rising and falling edges of all comparators (converter, controller, comparators). The open-drain output requires an external pull-up resistor - typically in the 100-kΩ range. Open-Drain outputs can be combined to create an "AND" logic function.

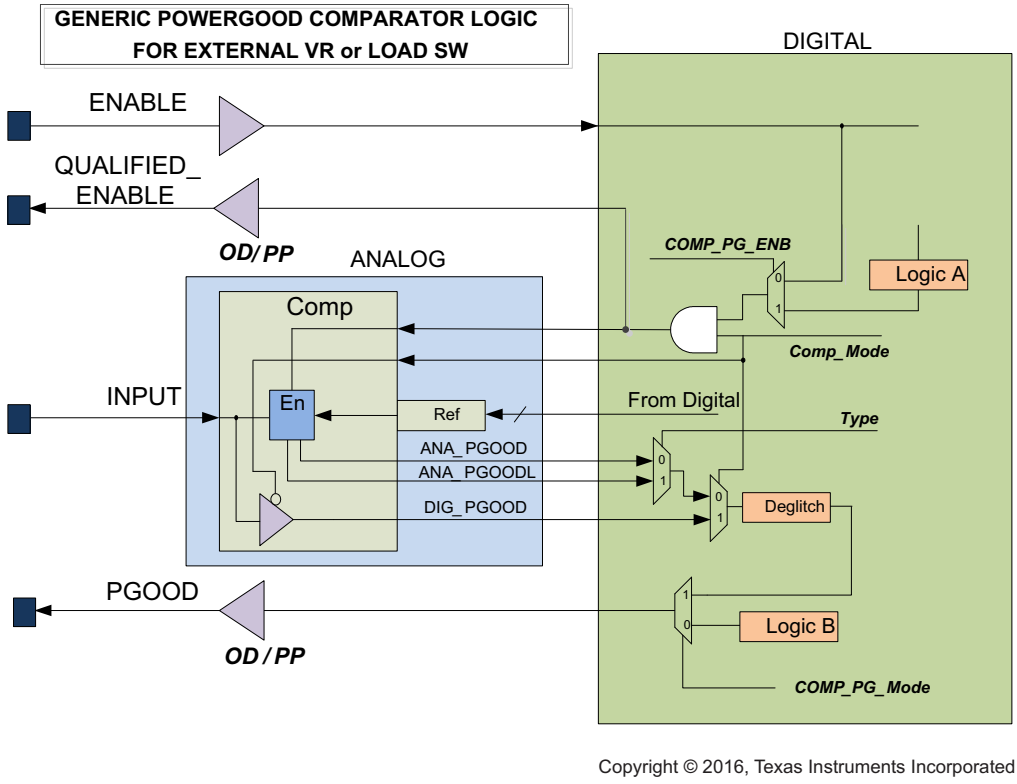


Figure 6-1. Generic Powergood Window Comparator with Open-Drain Output

6.3.3 Powergood Window Comparator

All the powergood comparators (converter, controller, comparators) can be configured for either Open-Drain outputs or Push-Pull outputs.

All the powergood comparators (converter, controller, comparators) in analog configuration monitors the output voltage to ensure it is within ±10% of the nominal target voltage. A 30-µs deglitch exists on the output of all the powergood comparators (converter, controller, comparators). The open-drain output requires an external pull-up resistor - typically in the 100-kΩ range. Open-Drain outputs can be combined to create an "AND" logic function. The push-pull output internally pulls up to VDDIO pin rail, or other noted input rail. Care should be taken to minimize series impedance on the PCB and providing adequate bulk and decoupling capacitance for the load switch rails. The Intel Skylake and Kabylake specification is ±5% at each rail, including those provided by load switches, therefore the load switch rails are still protected for ±10% powergood, as required by Intel Skylake and Kabylake specification.

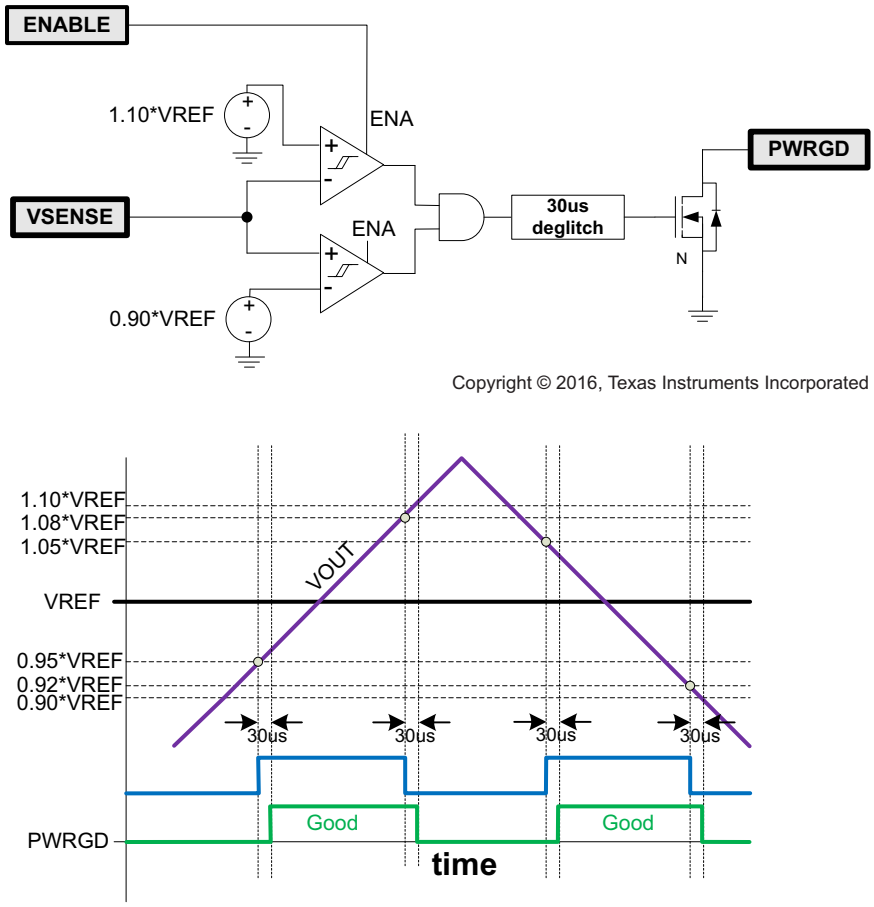


Figure 6-2. Powergood Window Comparator with Open-Drain Output

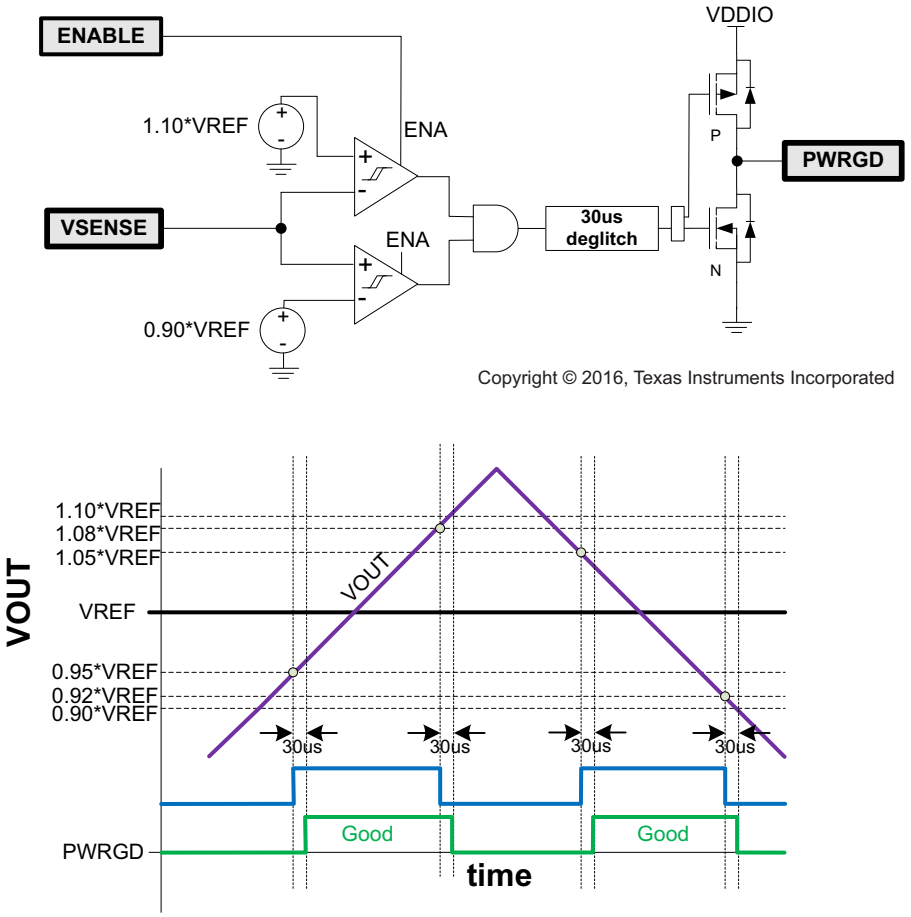


Figure 6-3. Powergood Window Comparator with Push-Pull Output

6.3.4 3.3-V LDO and 3V3SW Load Switch

The LDO3V powers up when Vin_LDO3V pin goes above the UVLO3V threshold. The LDO3V powers the internal digital blocks and analog blocks of the PMIC. It is also used as the positive rail of the powergood comparator and level-shifter outputs. The 3V3 load switch is optional to connect or disconnect the VOUT3V3SW output to a load. The load switch is enabled by the EN3V3SW pin.

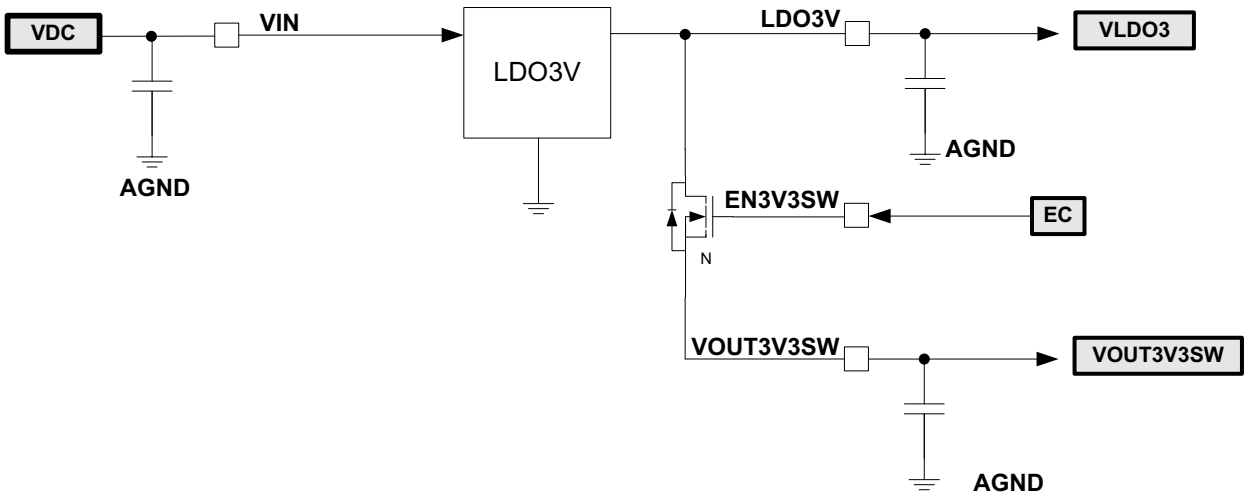


Figure 6-4. LDO3V and 3V3SW Load Switch

6.3.5 5-V LDO and 5VSW Load Switch

The LDO5V powers up when Vin pin goes above the UVLO5V threshold. The LDO5V powers the gate drives for all the five VRs of the PMIC. The 5-V load switch is used to switch the gate drive source from the internal LDO5V LDO to the 3.3-V PWM VR output as soon as the 3.3-V VR powergood signal indicates it is good. This significantly improves the efficiency of the VRs whose effect is more significant at lower VR load current, and VR input voltage. The load switch is enabled by the EN5VSW pin. Connect the V5A_PG signal to the EN5VSW pin. When the EN5VSW pin is high, the LDO5V internal reference drops to 4.5 V to ensure the 5-V VR drives all the gate drive current, but also ensures the gate drive never falls below 4.5 V. When EN5VSW is low, the LDO resumes to 5-V internal reference and the load switch is turned off to disconnect the 5-V VR.

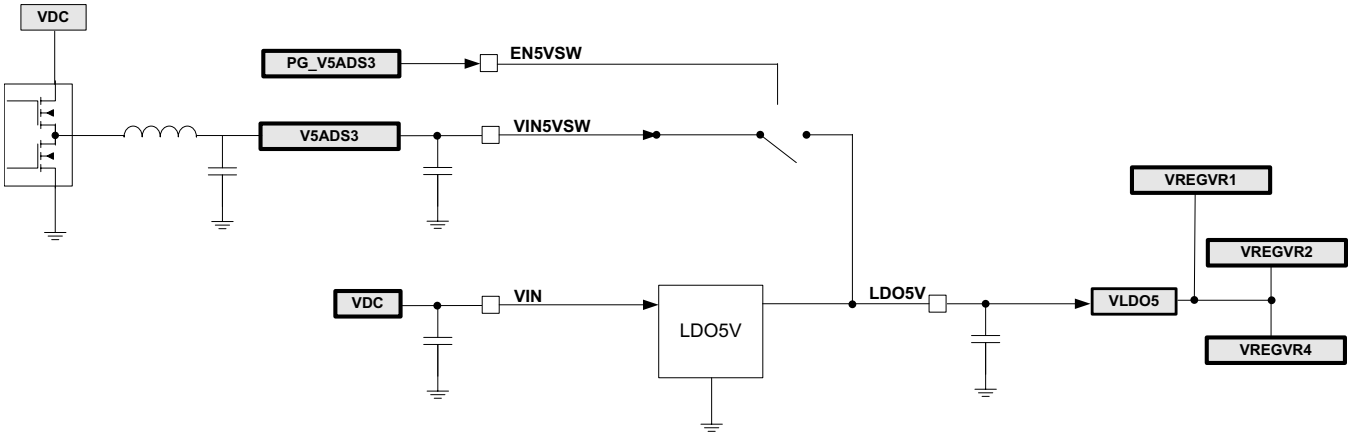


Figure 6-5. 5-V LDO and 5VSW Load Switch

6.3.6 RTC Selector and 3.1-V LDO

The RTC selector is used to select between the coincell backup battery or the internal 3.3-V LDO to power the 3P3A_RTC output rail for the RTC domain rail. If the Vin is below the UVLo5V threshold, the coincell battery is selected. If the Vin is greater than the UVLO5V, then the internal 3.1-V LDO is selected. The backup battery selector logic has a very low current draw when battery is selected to extend the charge life of the backup battery. This rail allows keeping the RTC registers' data even when the adapter and main battery is removed from the system. If the coincell voltage falls below the minimum threshold, the RTC registers will be reset to the default values. The 3.1-V LDO is at 3.1 V to ensure the PCH voltage is always below 3.2 V maximum to protect the PCH.

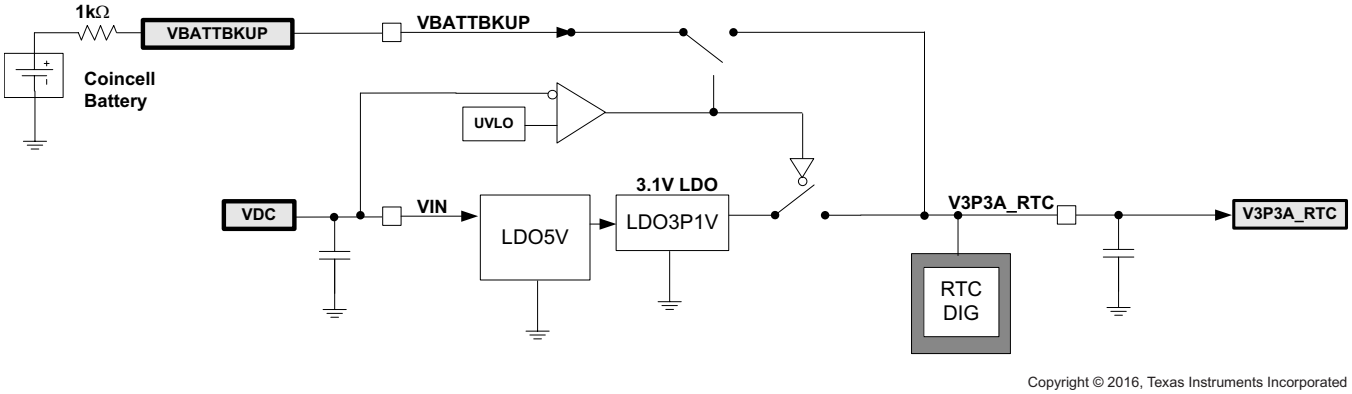


Figure 6-6. RTC Selector and 3.1-V LDO

6.3.7 Power Path Comparators

The Power Path comparators are high voltage comparators rated at 28 V both input and output that are independent of the rest of the PMIC. These can be used even when the PMIC is powered down, as long as the VINPP pin is above the UVLO5V threshold. Connect a resistor divider from the source to set the 1.25-V trigger threshold. These comparators can be used to detect adapter, and up to two batteries. An open-drain pin can detect the status, and a status register detects the status, that can issue an interrupt to the EC. The high voltage rated outputs can be used to turn on external P-channel power MOSFETs to control the power source path. A diode "OR" connection from all the power sources used is recommended to ensure the VINPP is up when a source is available. If these comparators are not used tie the VINPP pin to VIN and VIN_LDO3. Do not ground the VINPP pin when the VIN pin is powered up. These comparators can also be used a general purpose comparators.

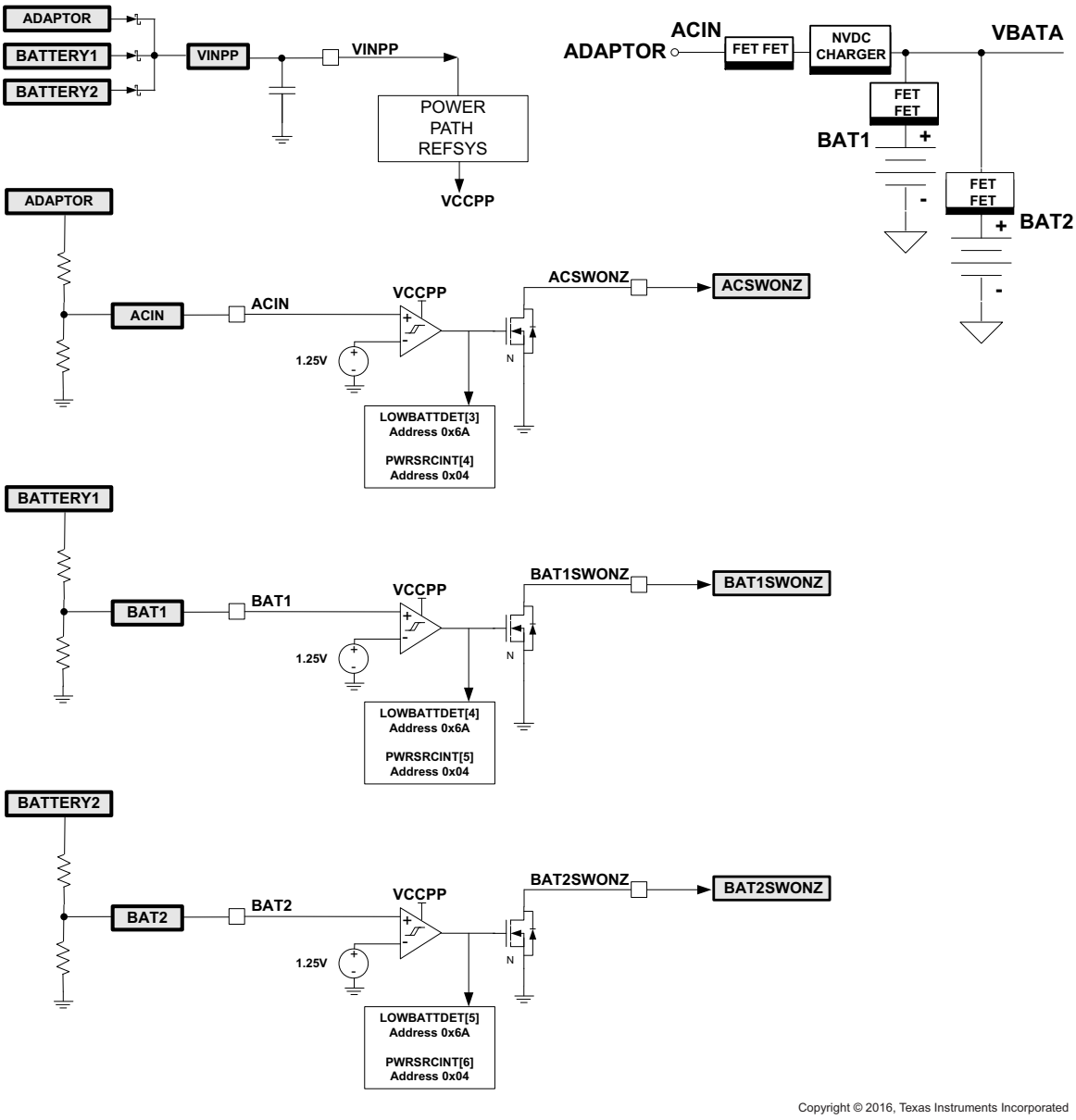


Figure 6-7. Power Path Comparators

6.3.8 UVLO Comparators

The UVLO comparators are high voltage comparators rated at 28-V input are powered by the VIN pin for LDO5V and 1.25-V LDO, and the VIN_LDO3V pin for th LDO3V. The VDCSNS input is also a high voltage input pin to detect if VBATA is above a programmable voltage. The Vin and VIN_LDO3 pin are tied directly to VBATA, while the VDCSNS pin requires a resistor divider to set the proper detection gain.

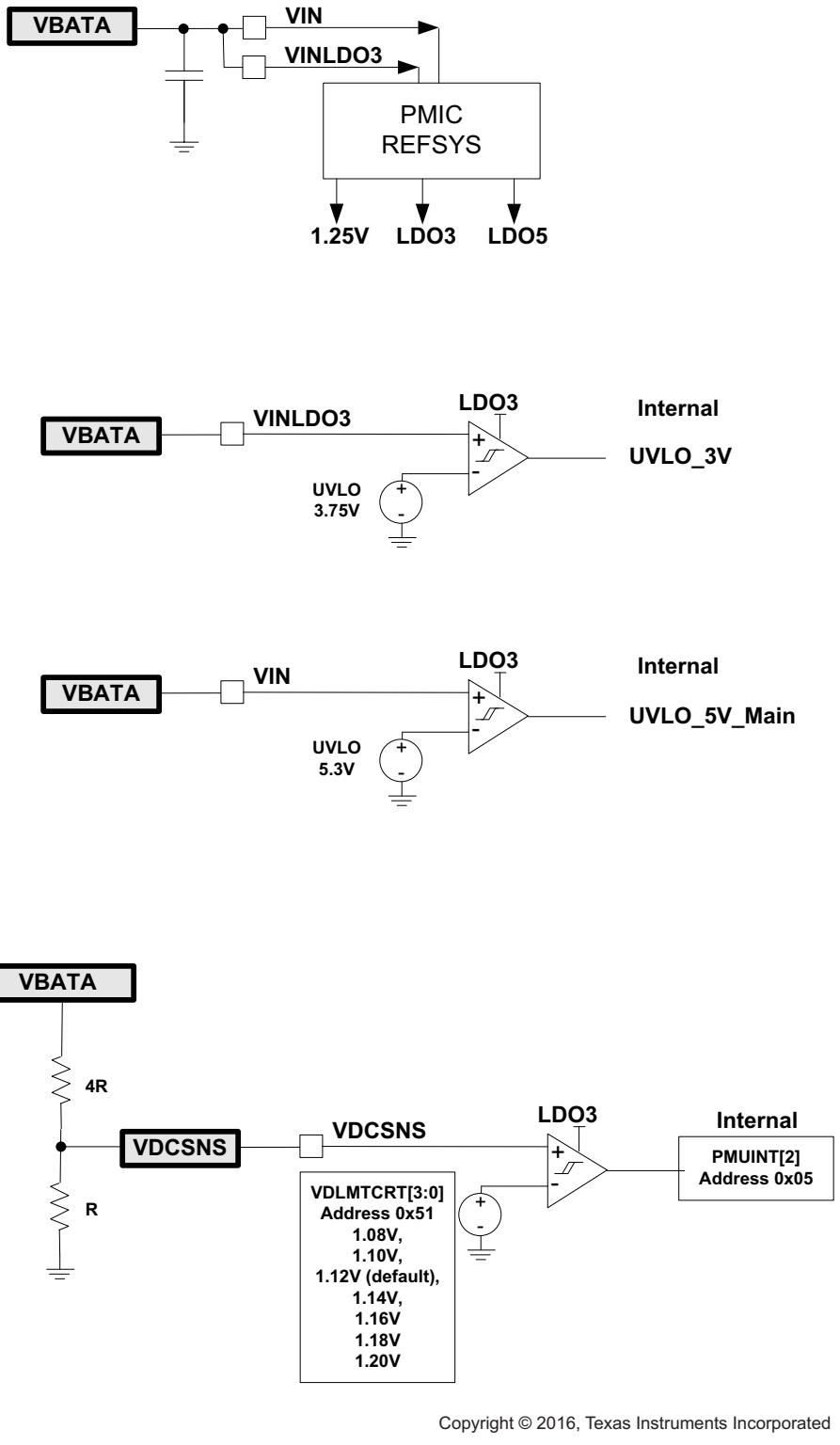


Figure 6-8. UVLO Comparators

6.3.9 Temperature Comparator

The temperature comparator is used to detect either several PTC thermisters stacked in series string, or a single NTC thermister. The PTC thermisters allow an inexpensive overtemperature detection of any fault throughout several points on the motherboard with each PTC thermister selected to have its own temperature threshold trigger point. An internal current source can be enabled to drive the PTC thermisters to minimize noise sensitivity. The current source can be disabled to drive with a voltage source such as the LDO3V to allow a tighter accuracy. Only a single NTC thermister can be detected at a time, but the NTC allows tracking several temperature profiles. This comparator can also be used as a general purpose comparator.

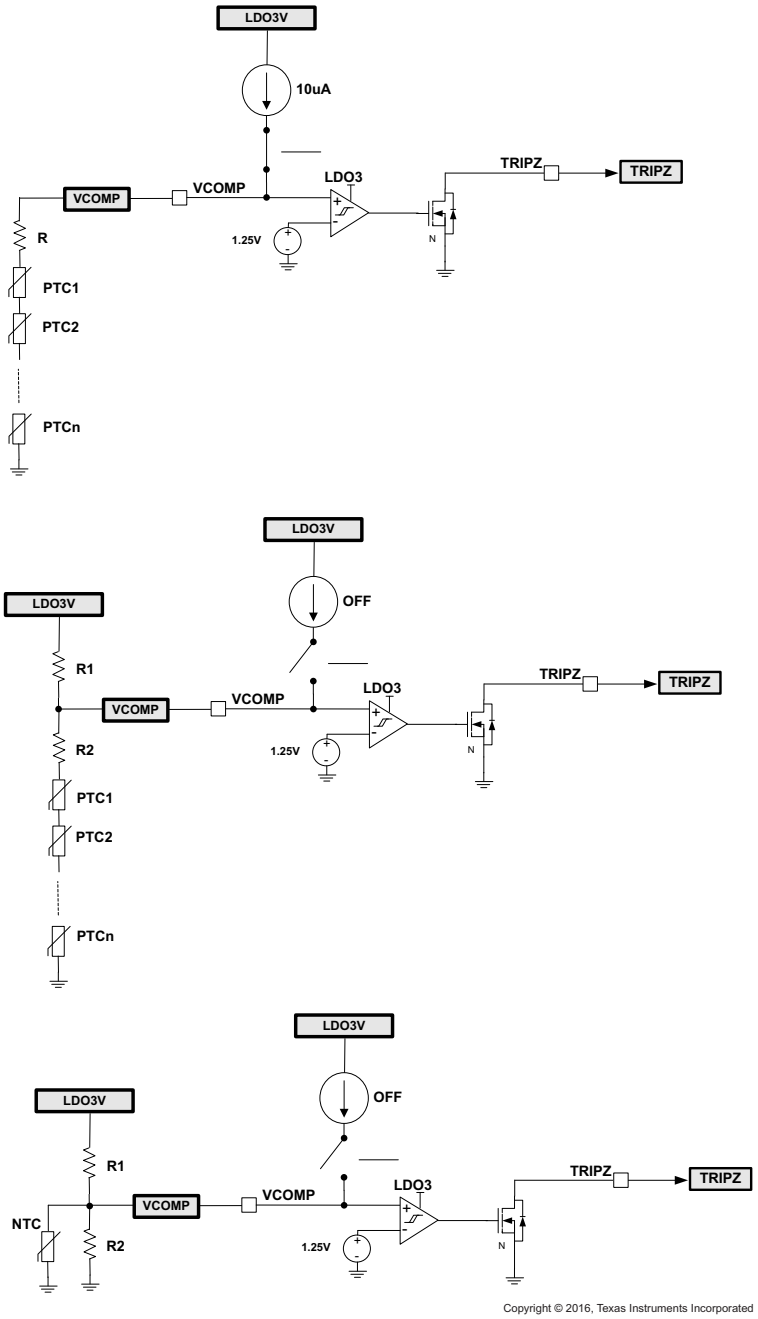


Figure 6-9. Temperature Comparator

6.3.10 Low Power Mode (LPM) / Connected Standby / Instant Go of VRs

All the Voltage regulators from the PMIC can be programmed by register to change the voltage in active mode, or to change to a lower voltage or decay in the low power mode. This can be used to save system power and extend battery life. And such capability is useful to meet the Connected Standby and Instant Go specifications. The STANDBYZ pin triggers low power mode (LPM) when low. The STANDBYZ triggers active mode (not in LPM) when high. Connect the SLP_S0# signal from the PCH to the STANDBYZ pin to trigger the low power mode, LPM. The default settings can be changed by the user with the I^2C register at any time.

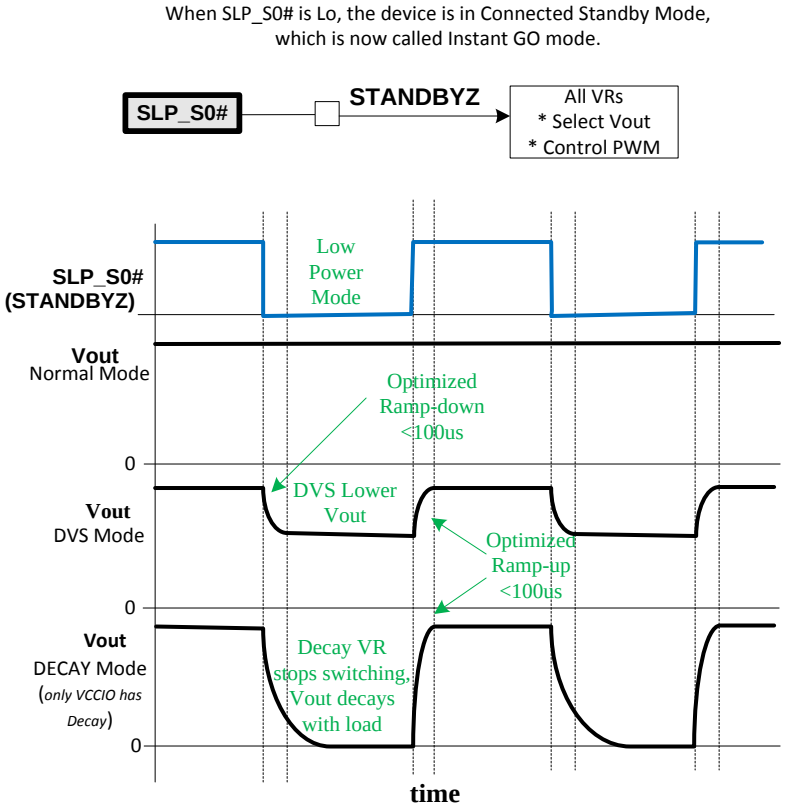


Figure 6-10. Low Power Mode (LPM) / Connected Standby / Instant Go of VRs

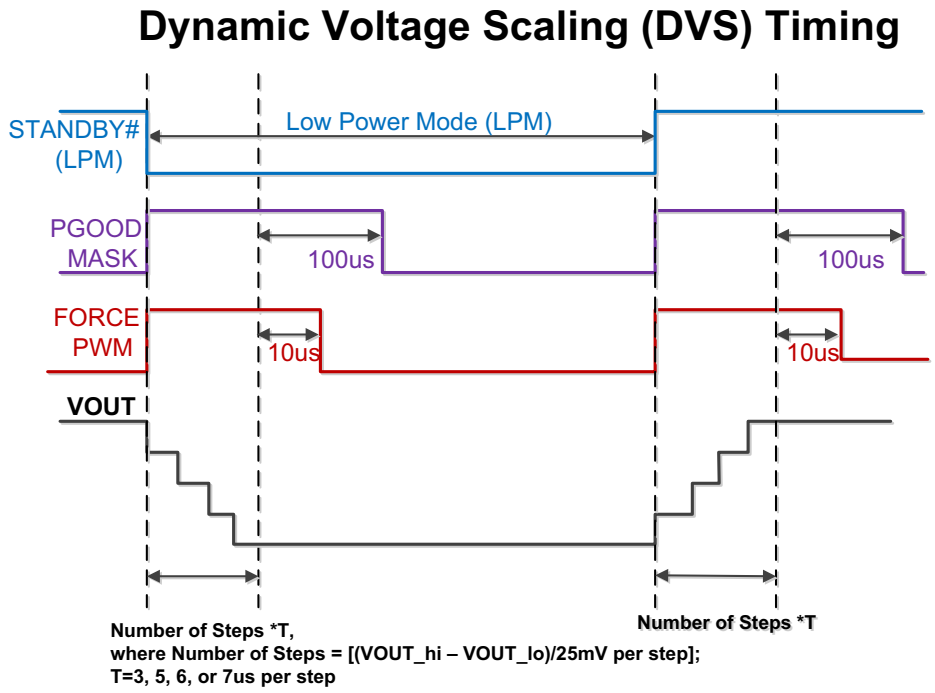


Figure 6-11. Dynamic Voltage Scaling (DVS) Transition Timing

The DVS Timing is controlled by the stepping the internal reference down/up. The total ramp down/up transition time is equal to the step time times the number of steps. The number of steps is equal to [(the VOUT_hi voltage minus the VOUT_lo voltage) divided by 25 mV per step]. The step time of 5 µs per 25-mV step ensures a time less than 70 µs for a 300-mV voltage change. The Controller is forced in PWM from the STANDBY# (LPM) transition until 10 µs after the reference ramp down/up ends. This helps ensure a fast response. Likewise the Powergood signal for that rail is masked from the STANDBY# (LPM) transition until 100 µs after the internal reference ramp down/up ends. This ensures there is no false powergood fault turn-off during DVS. In most cases undershoot/overshoot is negligible.

6.3.11 Enable and Powergood of VRs

The VRs are enabled by the ENVRx pins. The powergood is output on the PGVRx pins. The powergood pins can be defined as open-drain or push-pull output, depending on the function in order to allow "ANDing" or to reduce external components and quiescent current. there is a 30-µs deglitch on both edges of the powergood comparator outputs. A status register monitors the powergood outputs, and the powergood tree monitors the powergood for proper sequence and protection. The powergood signals can be masked by a register.

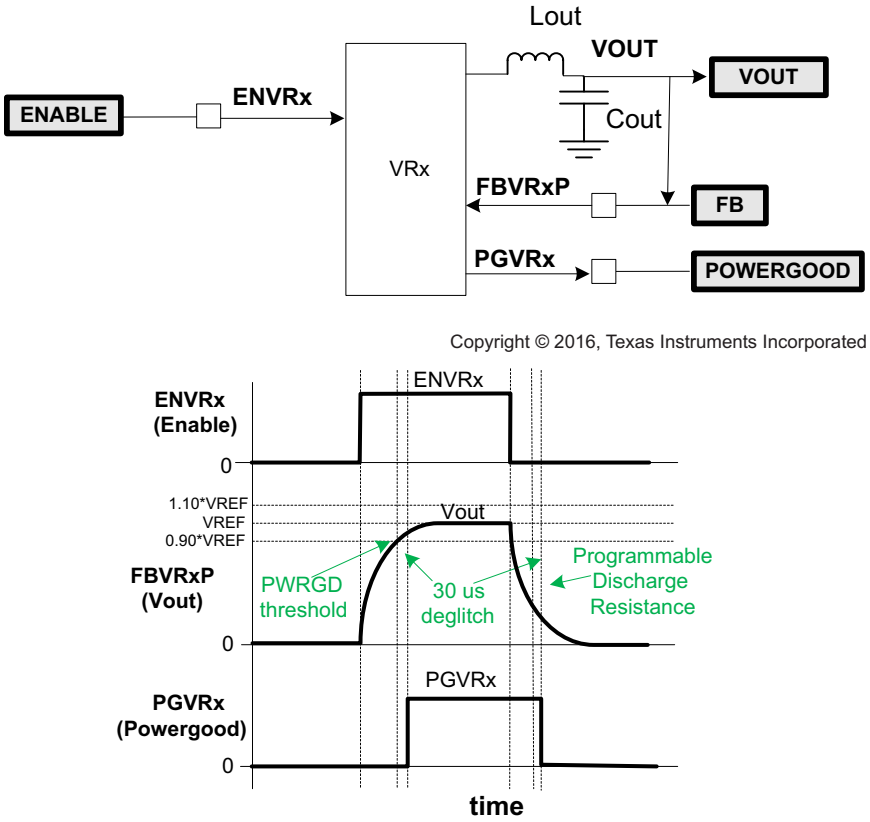
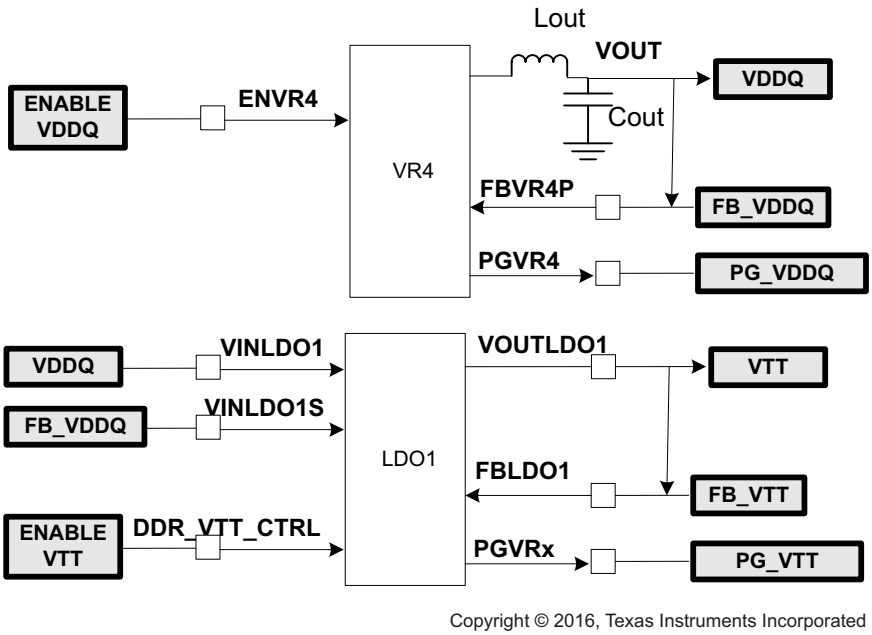


Figure 6-12. Enable and Powergood of VRs

6.3.12 VR4 VDDQ and LDO1 VTT Enabling

The VDDQ is enabled by the ENVR4 pin, while the LDO1 VTT push-pull LDO is enabled by the DDR_VTT_CTRL pin. The DDR_VTT_CTRL pin is often connected to the SLP_S0# pin to turn off during sleep mode. The DDRID pin is a tri-level pin that sets the VR4 VDDQ voltage to either 1.2 V, 1.35 V, or 1.1 V. DDR_VTT_CTRL pin ais also used for DVS control of VR4, as defined on register 0x36, V1P2UCNT.



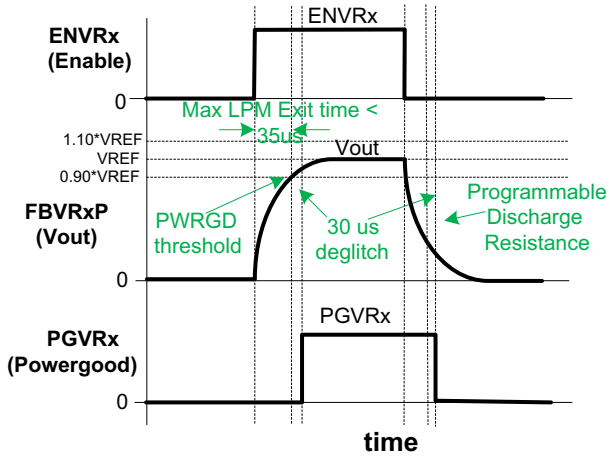


Figure 6-13. VR4 VDDQ and LDO1 VTT Enabling

6.3.13 Converters

The PMIC has 5 built in DCDC converters. The voltage regulators are highly configurable both in terms of voltage and current. Of the five voltage regulators, four voltage regulators have an external power stage, with programmable current limit (programmed by an external resistor), which allows optimal selection of external passive components based on desired system load. VR2 has a completely integrated power stage, except for the required passive components. To maintain high efficiency, the converters are implemented as synchronous step down converters.

One additional voltage regulators in the form of Low Drop Out (LDO) linear regulators are integrated as part of the PMIC. One of the LDOs, LDO1, is capable of sinking and sourcing current that regulates from the step down controller (for DDR memory). This LDO is designed to specifically provide the VTT power to DDR memory. Its output voltage tracks the output voltage of the step down controller and is set to regulate to half of the step down controller voltage.

6.3.13.1 Power Save Mode

At medium and heavy loads, the converter and the controllers operate in a PWM mode. As soon as the inductor current gets discontinuous, which means that the output current gets lower than half of the inductor ripple current, the converters enter Power Save Mode. In Power Save Mode the switching frequency decreases linearly with the load current and maintains a high efficiency. By default, the converters and controller operate in the AutoPFM mode such that the transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

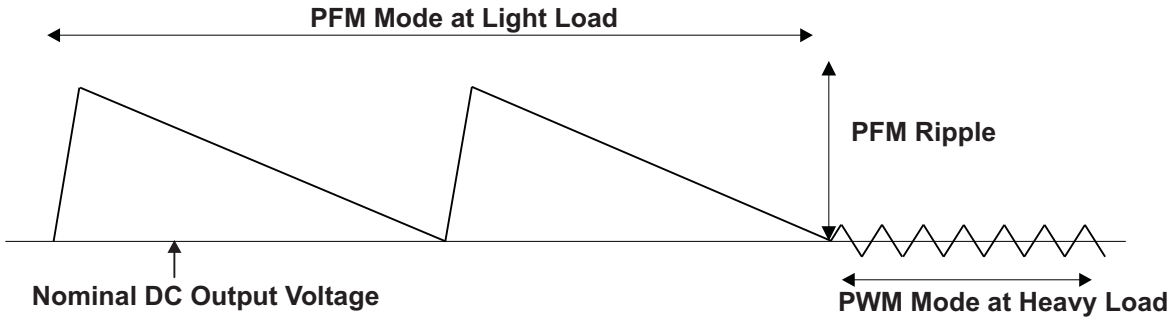


Figure 6-14. PFM and PWM Mode Operation

The figure above shows the converter/ controller operation in PFM and PWM mode. In PFM mode the minimum voltage that the output falls to is the programmed regulation voltage. The output voltage ripple in PFM mode is determined based on the external passive components (L and C). The regulator ensures that the minimum voltage during PFM mode is the same as the programmed regulation voltage (within the AC and DC tolerance).

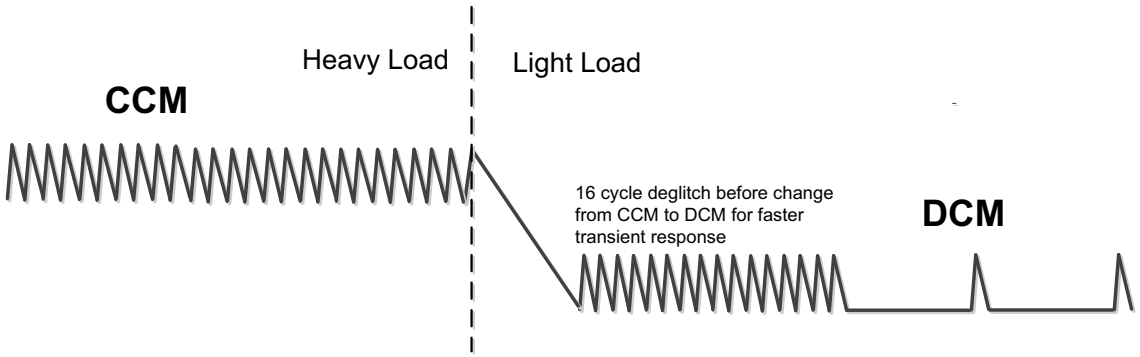


Figure: Inductor Current during CCM to DCM Transition

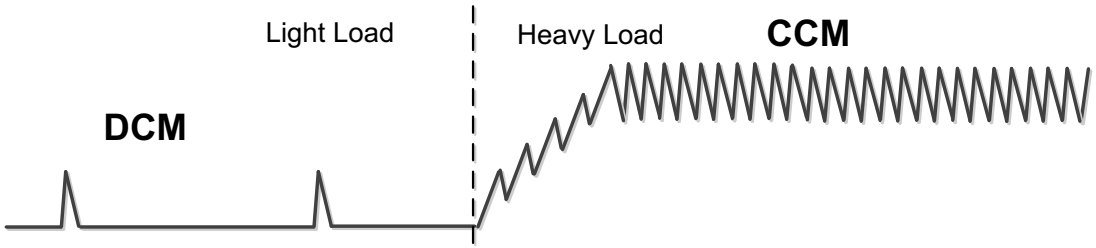


Figure: Inductor Current during DCM to CCM Transition

Figure 6-15. Operation During Load Step Transient: CCM to DCM Transition and DCM to CCM Transition

The figure above shows the inductor current of the controller during a load transient as it transitions in and out of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). CCM is often referred to as pulse width modulation (PWM) mode, and DCM is referred to as pulse frequency mode (PFM) mode. When the load step falls, there is a 16 cycle deglitch going from CCM to DCM. This allows a fast transient response and tighter peak to peak ripple voltage. When the load step rises, there is no deglitch time, so the controller goes directly from DCM to CCM in a quick response characteristic of CCM. The VR1, VR3, VR4, and VR5 controllers have the CCM to DCM 16 cycle count deglitch enabled.

6.3.13.2 Voltage Regulator Startup

All the voltage regulators including the VTT LDO1 can be enabled using either pin enables or I^2C commands. The default setting uses the pin enable. The VTT LDO1 can only be enabled using the DDR_VTT_CTRL discrete input. VTT LDO1 can be enabled by pin (DDR_VTT_CTRL) or by register (0xE9, MSB bit 7 masks the DDR_VTT_CTRL pin, and bit 6 enables the VTT LDO1). Each Voltage Regulator (VR) can be enabled by the enable pin (ENAVRx) or by I^2C Register (xCNT). The voltage should not be changed by register at the exact same time the voltage regulator is enabled. If a different voltage than the default is needed at power-up, then the register (xCNT) should program the voltage first, and then a separate command should enable the register separately. Dynamic voltage change (DVS) can be done any time after power-up.

Each of the voltage regulators except for the VTT LDO1 are controlled by an internal softstart to make sure the output voltage ramps up gently and does not cause huge inrush current during startup to prevent droop on the input. The VTT LDO1 startup time is driven by the DDR memory requirements for the VTT voltage rail - which requires that the ramp up on voltage be faster than 35 µs.

6.3.13.3 Powergood, Power Fault, and Emergency Power Shutdown

During operation, when the voltage regulators are enabled, the output voltage for each rail is monitored in order to assess if the output voltage is within a specified voltage range. A powergood status bit is generated and stored in the PGOOD_STAT1 and PGOOD_STAT2 registers. If the output voltage is within the specified voltage range, the respective powergood status bit is set to a logic high. If the output voltage falls below or goes above the specified voltage range, the powergood status bit will be set to a logic low.

By default, if any of the output voltage rails experience a power fault condition, the PMIC will automatically shutdown in order to protect the system unless the power fault is masked. If a power fault occurs, the source of the power fault is maintained in the PWRSTAT1 and PWRSTAT2 registers which are maintained in the RTC domain. The voltage thresholds for each of the powergood comparators is a percentage relative to the nominal voltage setting of the output voltage - see the parametric table for each voltage regulator powergood for the USL and LSL limits of the powergood comparators.

If a particular voltage rail is not critical to the performance of the overall system, the respective powergood output can be masked using the PGMASK1 and PGMASK2 registers. The masking of a power fault will inhibit an automatic PMIC shutdown. This can be also very helpful for debug purposes in case of system failure to isolate the voltage regulator with the sensitive output voltage.

In order to avoid an erroneous power fault during the turn-on of the voltage regulators, the power fault is masked for 10 ms relative to the enable whether it be from the discrete signal or from an I^2C command. powergood is also masked when coming out of sleep (S3 state) for 100 µs after the ALL_SYS_PWRGD pin goes high to ensure that there is no false triggering of the powergood comparators.

The PMIC will only cause a Emergency Power Shutdown of the rails for the conditions shown in the table below. The PMIC monitors each rail and ensures there is no problem. All rails are monitored for fault protection, except for V3.3A_DSW and V5A external voltage regulators. The V3.3A_DSW and V5A have no effect on Power Fault and cannot cause a shutdown, unless either one affects another rail. Notice also, that the current limit (OCP) does not directly cause a shutdown. Instead, OCP could cause a shutdown indirectly by means of a Power Fault. The OCP will limit the maximum possible output current, such that if the load current exceeds the Ilim, then the voltage will drop, until eventually the lower output voltage causes a Power Fault if it is below the powergood threshold for more than 30 µs. Emergency Power Shutdown causes all rails to power-down within 1 us. The LDO3, LDO5, and VREF1.25V will stay up if the input voltage is greater than the UVLO3 and UVLO5.

Table 6-2. All Possible Emergency Power Shutdown Conditions

SHUTDOWN CONDITION
VIN pin ≤ UVLO5V
VINLDO3 pin ≤ UVLO3V
Powergood Fault (OVP, UVP): Vout ≤ 90% or Vout ≥ 110% for ≥ 30 µs
Tj ≥ Tcritical (OTP)
SHUTDOWNZ pin pulled-low
I^2C Control Force Shutdown by SDWNCTRL register (address = 0x49)

6.3.13.4 Current Limit

All voltage regulators are current limited, the current limit can be set based on the application load current using an external resistor for all VRs except for VR2 which has an internally set current limit as it has an integrated power stage. The current limit controls the maximum output current. If the maximum current is reached, the output voltage will start to droop since the load can no longer be supplied with sufficient power. If the voltage drops below the powergood threshold, the power fault status will be set to a logic high and if the power fault is not masked, the PMIC will automatically shutdown in a controlled manner to protect the system.

6.3.13.5 Output Discharge Feature

All the voltage regulators have a built in output discharge feature. The output discharge feature consists of being able to configure register bits to enable a discharge resistor which is only active whenever the voltage regulator is disabled. The discharge resistors for each of the voltage regulators can be configured using the DISCHCNT1, DISCHCNT2, DISCHCNT3 and DISCHCNT4 registers. The discharge resistors are disconnected when the voltage regulators are enabled in order to minimize any losses within the PMIC.

6.3.13.6 Output Voltage Control

All voltage regulators are designed to regulate a fixed output voltage. To achieve high accuracy the output voltage for the converters and controller is sensed using a separate feedback pin. For each of the voltage rails, except for the VTT LDO, the output voltage can be changed to slightly higher or lower values by changing the default setting in the voltage regulator control registers (see section on the Voltage Regulator Voltage Options). This function can be used to save power when supplying the connected load at its minimum possible supply voltage or to compensate for voltage drops during load transients by programming it slightly higher. In addition the range of the output voltage for the regulators is highly programmable. If you need a different output voltage configuration from the specified default, please contact TI to generate you a custom part.

6.3.13.7 Converter Low Power Mode Operation

For optimizing low power operation, the output voltage of the converters can be set to a specific value. The low power output voltage is set by the specific register and bits shown in the Voltage Regulator Voltage Options tables. Entering the low power mode is accomplished by asserting the SLP_S0# signal to a logic low. In this low power mode, the powergood function remains active and is not affected by the transition from normal operation mode to the low power mode and vice versa.

6.3.13.8 Controller Low Power Mode Operation

For optimizing low power operation, the output voltage of the controllers can be set to a specific value. The low power output voltage is set by the specific register and bits shown in the Voltage Regulator Voltage Options tables. Entering the low power mode is accomplished by asserting the DDR_VTT_CTRL pin or the STANDBYZ pin to a logic low. In this low power mode, the powergood function remains active and is not affected by the transition from normal operation mode to the low power mode and vice versa. DDR_VTT_CTRL pin asserts DVS on VR4, while STANDBYZ pin asserts DVS in VR1, VR2, VR3, and VR5, as defined by ther CNT registers. In situations where the output current demand from the controller is very small, the controller is automatically placed in an Ultra Low Quiescent (ULQ) mode to reduce power consumption and increase the efficiency.

6.3.13.9 Controller Internal Ramp Comparator

The controllers have an internal ramp, characteristic of th DCAP2 control architecture, to give improved performance with low-ESR output capacitors. This internal ramp provides ramp compensation that helps maintain a relatively constant frequency during CCM, and it provides better stability for designs with very low ESR on the output capacitors. The ramp height can be optimized and is a function of the input voltage to provide proportional feed-forward. At very high voltages, the ramp may exceed the operating window of the PWM comparator and may overpower the natural ripple of the output, so there is a need to switch to a smaller ramp. As the ramp was already getting large, it helps to switch back to a smaller size. To achieve this, a comparator monitors the input voltage at the VIN pin. When input voltage rises and exceeds 11 V, it changes the ramp to a slightly smaller value. There is a wide 1.1-V hysteresis, so at approximately 9.9 V as the Vin falls, the ramp returns to the slightly bigger size. In most cases this difference is negligible.

6.3.13.10 Undervoltage Lockout

An undervoltage lockout function prevents the PMIC from operating if the supply voltage on the VIN pin of the PMIC is lower than the undervoltage lockout threshold (see Electrical Characteristics table). During operation, if the supply voltage on the VIN pin drops below the undervoltage lockout threshold, the system/PMIC will shutdown.

6.3.14 Coincell Selector

6.3.14.1 Functional Description of RTC Powerpath and LDO

In case where the main system battery is removed and there is no alternate power source, the RTC data, configuration and status registers, oscillator and timekeeping path of the RTC block are backed up by either a super capacitor or a coin cell battery. If the coincell/ super capacitor battery voltage falls below the minimum operational voltage and there is no input voltage (AC/ DC above the PMIC UVLO), the RTC data registers will be invalid. As the Intel RTC cannot handle a max voltage higher than 3.2 V, when AC/DC is present and is higher than the UVLO threshold, the RTC is supplied by the AC/DC rather than from the coincell - thus maximizing the stored charge in the coincell battery. When AC/DC is present, the internal coincell selector selects the higher of the coincell voltage and the AC/DC voltage. When AC/DC is chosen as a source, there is a coincell LDO which is driven from the 5-V PMIC LDO to regulate The output voltage is fixed at 3.1 V to ensure the maximum voltage is kept below 3.2 V.

The main power source for the RTC LDO is the 5-V PMIC internal LDO, when the main system battery (VDC) is greater than 5.4 V. The RTC LDO will be bypassed and the RTC supply will be powered by the coincell when VDC falls below this threshold - to maximize the coincell battery life. The coincell is used as a last resort. All power routing of the source selection for the RTC power is done internally and no external connections other than the coin cell or super cap is required.

6.4 Device Functional Modes

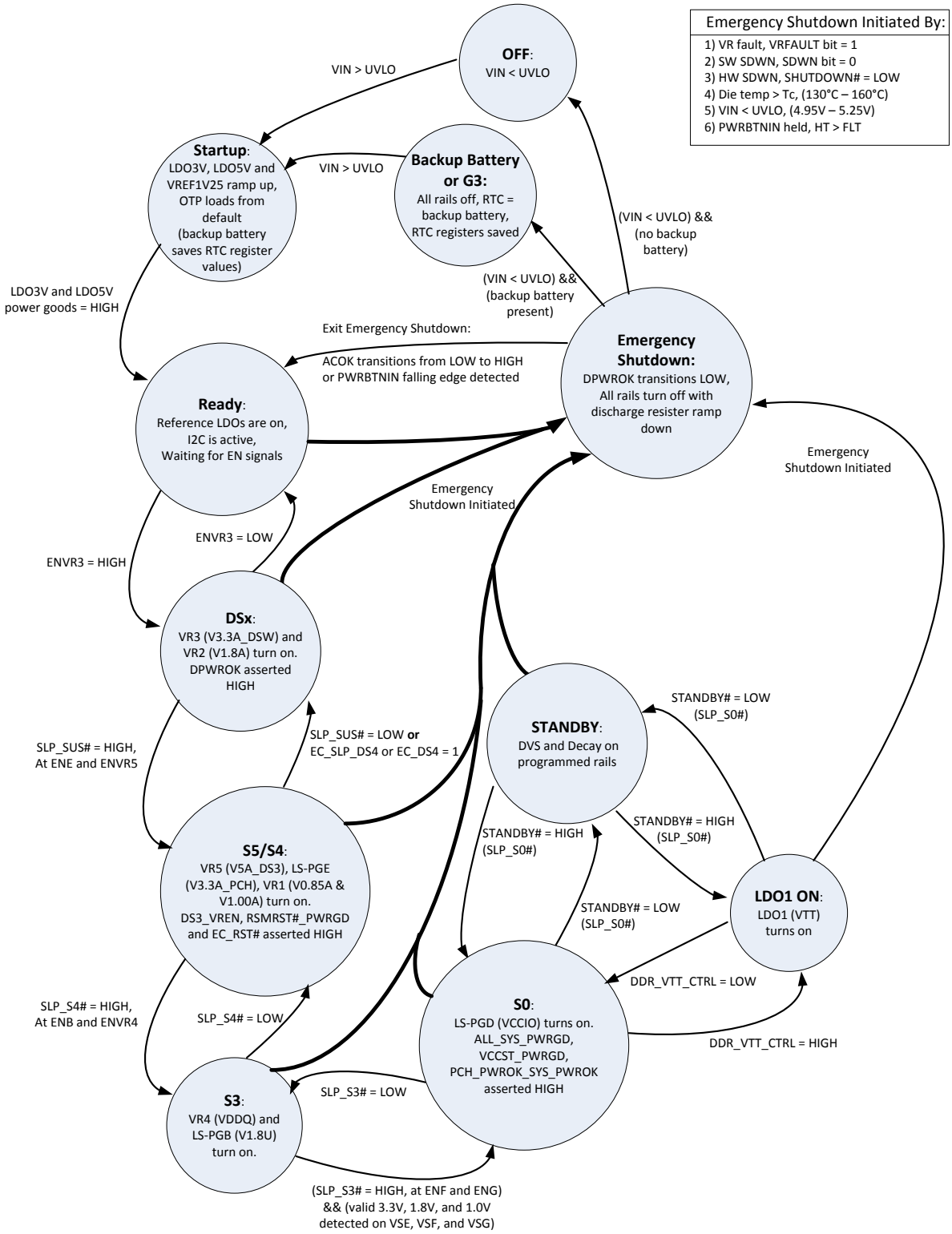


Figure 6-16. Sequence of Function Modes - Assuming the TPS650830 Application Configuration Connections

6.4.1 OFF State - No VIN and No Backup Battery

If the VIN and the VBATTBKUP battery are both lower than their respective UVLOs then, the device will be in the OFF state. In this state the device will not be able to turn on or enable any VRs or discrete load switches / regulators. The clock and I^2C are not active in this state.

In the OFF state, the power path switch comparators, ACIN, BAT1, and BAT2 are the only block available for use. In order to use these comparators the VINPP must be supplied with the highest of the 3 input voltages from AC, BAT1, and BAT2. In all other states the VINPP must be supplied from the same source as VIN.

6.4.2 Startup

The device enters STARTUP once the VIN > UVLO. During STARTUP LDO3V, LDO5V, and VREF1V25 ramp up. Once both LDO3V and LDO5V reach their nominal voltage and their powergoods assert HIGH, the OTP loads into the I^2C registers. After the LDO5V_PG asserts HIGH, the RTC LDO is turned on and the V3.3A_RTC is regulated to 3.1 V powered from the LDO5V. Once the OTP is loaded and the RTC is regulated to 3.1 V the device enters READY state.

6.4.3 Ready State

The device is considered to be in the READY state once, all of the internal supplies and RTC are regulated and the OTP is loaded into the registers. In this state the device is ready for enable commands. The comparators, level shifters and all other blocks are available for use.

6.4.4 S5/S4 State

The S5/S4 states are entered when the V3.3A_DSW, V1.8A, V5A_DS3, V3.3A_PCH, V0.85A, and V1.00A are all enabled and regulating with valid powergoods. In this state the RSMRST#_PWRGD will be asserted HIGH.

6.4.5 S3 State

To enter S3 state the SLP_S4# signal must be asserted HIGH. Upon SLP_S4# assertion the VDDQ (VR4), and V1.8U rails are turned on.

6.4.6 S0 State

To enter S0 state the SLP_S3# signal must be asserted HIGH in addition to valid 3.3-V, 1.8-V, and 1.0-V signals on VSE, VSF, and VSG pins. Upon PGG = 1 and PGVR4 = 1 the VCCIO and rail is turned on and the device transitions to S0 state. ALL_SYS_PWRGD asserts HIGH in this state.

6.4.7 Standby

Standby is entered when the STANDBYZ pin transitions from HIGH to LOW provided that ALL_SYS_PWRGD is HIGH. During the STANDBY state the device will DVS and/or decay the VRs that are programmed to DVS or decay from the I^2C register definitions, (registers x30 - x38).

6.4.8 DSx State

The DSx state is entered from STARTUP by the enabling of V3.3A_DSW. From the S5/S4 states it can be entered by either pulling the SLP_SUS# signal LOW or writing to VREN, EC_SLP_S4 = EC_DS4 = 1. In this state, the V5A_DS3 and V1.8A may be turned off.

6.4.9 Emergency Shutdown

Emergency Shutdown is a protection feature for the system loads. It reduces the risk of reverse bias in the processor or other devices from once rail to another. Once Emergency Shutdown is initiated the DPWROK pin is pulled LOW, discharge resistors are enabled for all rails, and all rails are disabled at the same time. The PMIC remains in Emergency Shutdown until any of the follow occurs:

- PWRBTNIN falling edge detected
- ACOK transitions from LOW to HIGH
- VIN < UVLO

Emergency Shutdown is initiated when:

- VR Fault detected - Read RESETIRQ1 to determine if VR fault caused shutdown.
- Hardware force shutdown
- Software force shutdown
- Die Thermal Fault - Read RESETIRQ2 to determine if thermal fault caused shutdown.
- PWRBTN held longer than defined time by FLT[5:0] - Read RESETIRQ1 to determine if push button caused shutdown.
- VIN < UVLO - Read IRQLVL1 bit 2 to determine if VIN < UVLO caused shutdown.

6.4.10 Backup Battery / G3 - No VIN

G3 is an Intel defined state where the VIN < UVLO to the device but, a valid backup battery is present on VBATTBKUP pin. In this state, the backup battery is passed to the RTC output and the RTC domain I^2C register values are saved. Once the VIN > UVLO these register retain their value and can be read once I^2C is ready.

In this state, all VRs and internal LDOs are off and I^2C access is not available.

6.5 Programming

6.5.1 I^2C - Interface

I^2C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see I^2C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS650830 works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to TPS650830 higher than the undervoltage lockout threshold. The I^2C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document.

The TPS650830 supports 7-bit addressing; 10-bit addressing and general call address are not supported. The default device address is defined by the status of the SLAVEADDR pin. 3 different slave addresses are possible, 0x30 (SLAVEADDR 0 V), 0x32 (SLAVEADDR 3.3 V) and 0x34 (SLAVEADDR floating).

All registers are set to their default value when the supply voltage is below the UVLO threshold.

6.5.1.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 6-17. All I^2C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 6-18. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 6-19, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 6-17. This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out. FS I^2C operation does not support repeated start

6.5.1.2 Diagrams of I²C Protocol

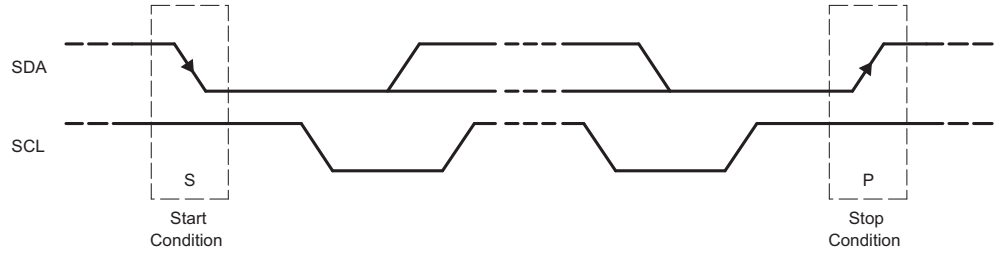


Figure 6-17. START and STOP Conditions

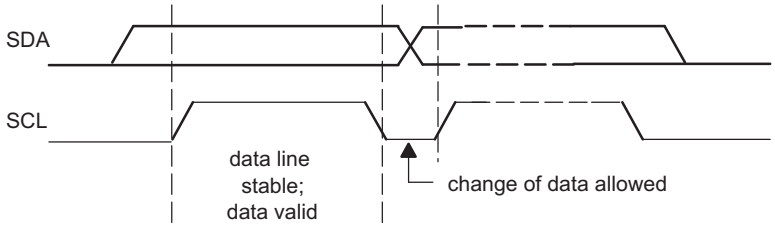


Figure 6-18. Bit Transfer on the I²C-bus

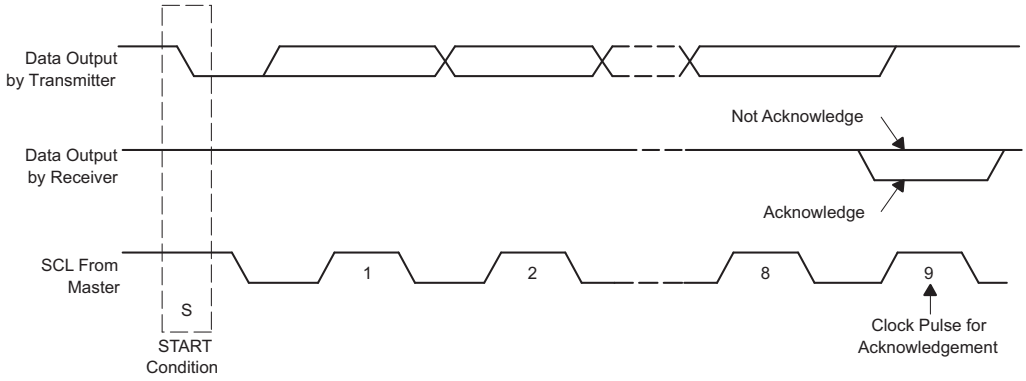


Figure 6-19. Acknowledge on the I²C-Bus

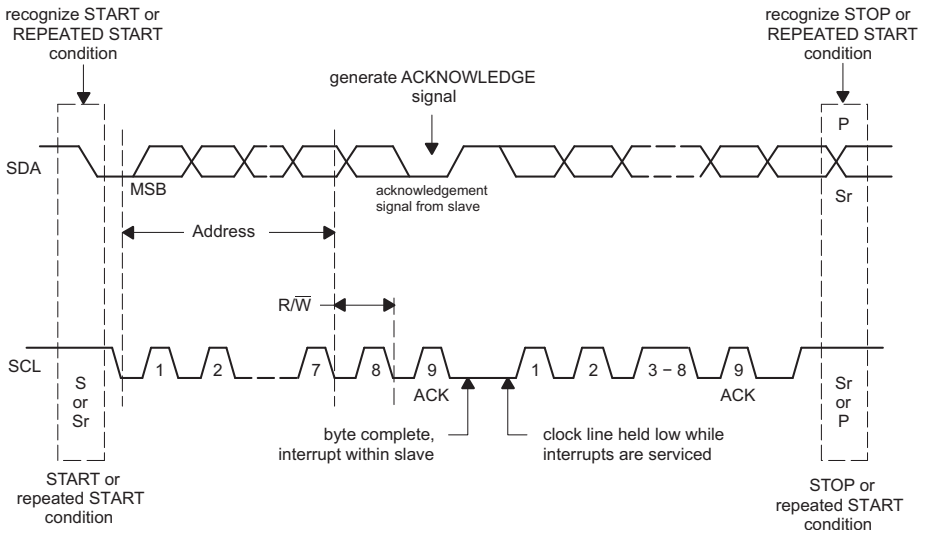


Figure 6-20. Bus Protocol

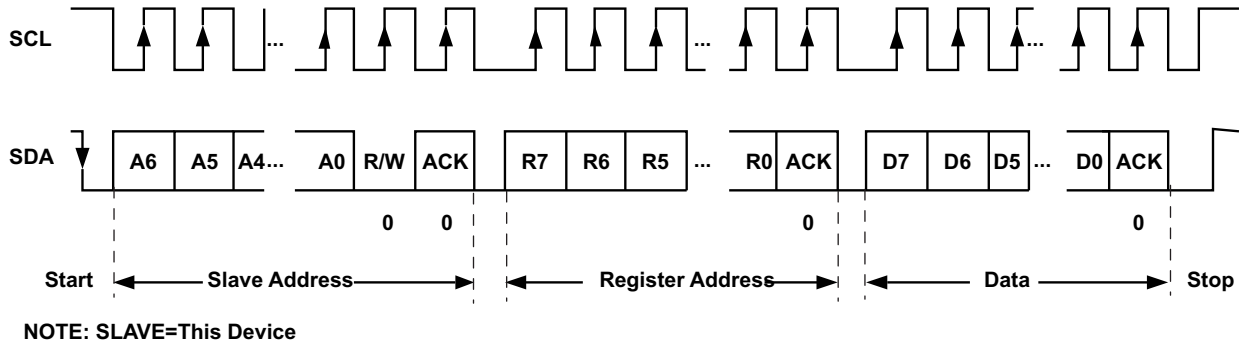


Figure 6-21. I²C Interface WRITE to Device in F/S Mode

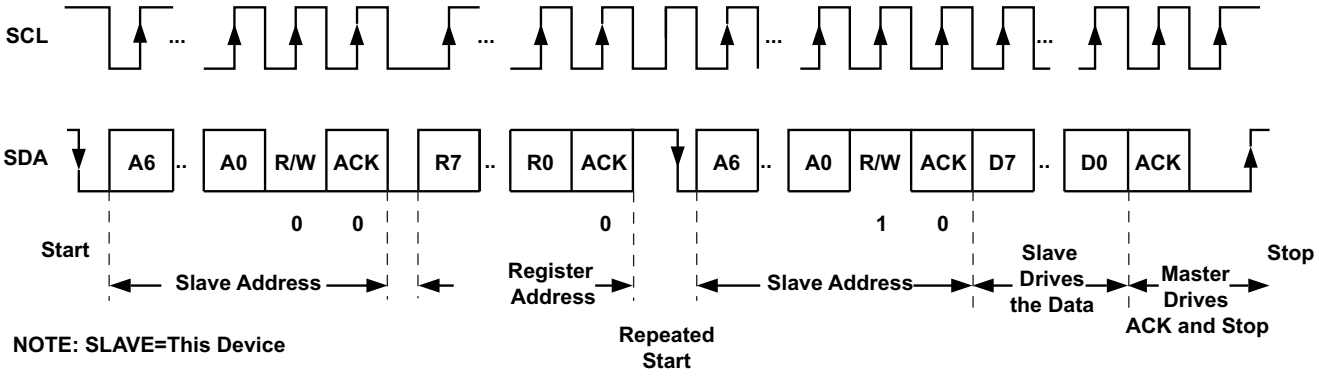


Figure 6-22. I²C Interface READ from Device in F/S Mode

6.6 Register Map

Table 6-3. Register Summary

Register Address	Register Name	Domain	Short Description
x00	VENDORID	UVLO	Code that indicated a Texas Instruments' PMIC device.
x01	REVID	UVLO	Code to identify device revision and programming revision.
x02	IRQLVL1	RTC	Top level interrupts
x04	PWRSRCINT	RTC	Input power interrupts
x05	PMUINT	RTC	PMU interrupts
x08	RESETIRQ1	RTC	Emergency Shutdown interrupts
x09	RESETIRQ2	RTC	Emergency Shutdown interrupts
x0B	MPMUINT	RTC	Mask PMU interrupts
x0C	MPWRSRCNT	RTC	Mask input power interrupts
x11	RESETIRQ1MASK	RTC	Mask Emergency Shutdown interrupts
x12	RESETIRQ2MASK	RTC	Mask Emergency Shutdown interrupts
x13	IRQLVL1MSK	RTC	Mask top level interrupt
x14	PBCONFIG	RTC	Power Button configuration
x15	PBSTATUS	RTC	Power Button Status
x16	PWRSTAT1	RTC	VR Fault Reporting
x17	PWRSTAT2	RTC	VR Fault Reporting
x18	PGMASK1	RTC	Mask VR PGs from System Power Good Tree
x19	PGMASK2	RTC	Mask VR PGs from System Power Good Tree
x30	VCCIOCNT	UVLO	VCCIO (PGD) Control

Table 6-3. Register Summary (continued)

Register Address	Register Name	Domain	Short Description
x31	V5ADS3CNT	UVLO	V5A_DS3 (VR5) Control
x32	V33ADSWCNT	UVLO	V3.3A_DSW (VR3) Control
x33	V33APCHCNT	UVLO	V3.3A_PCH (PGE) Control
x34	V18ACNT	UVLO	V1.8A (VR2) Control
x35	V18U25UCNT	UVLO	V1.8U_2.5U (PGB) Control
x36	V1P2UCNT	UVLO	V1.2U / VDDQ (VR4) Control
x37	V100ACNT	UVLO	V1.00A (VR1) Control
x38	V08ACNT	UVLO	V0.85A (VR1) Control
x3B	VRMODECTRL	UVLO	Force Low Power Mode
x3C	DISCHCNT1	UVLO	Discharge Resistors Settings
x3D	DISCHCNT2	UVLO	Discharge Resistors Settings
x3E	DISCHCNT3	UVLO	Discharge Resistors Settings
x3F	DISCHCNT4	UVLO	Discharge Resistors Settings
x40	PWRGDCNT1	UVLO	System Level Power Goods
x41	VREN	UVLO	Deep Sleep Enable
x42	REGLOCK	UVLO	Lock for Control Registers, x30 - x38
x43	VRENPINMASK	UVLO	Mask hardware enable pins
x48	RSTCTRL	RTC	Reset Control
x49	SDWNCTRL	UVLO	Software Force Shutdown
x51	VDLMTCRT	UVLO	VDCSNS Settings
x69	ACOKDBDM	UVLO	ACOK Settings
x6A	LOWBATTDET	UVLO	Battery Detection Settings
x6F	SPWRSRCINT	UVLO	Input power Statuses
xD0	CLKCTRL1	RTC	Clock Control
xDD	COMPA_REF	UVLO	Comparator A Settings
xDE	COMPB_REF	UVLO	Comparator B Settings
xDF	COMPC_REF	UVLO	Comparator C Settings
xE0	COMPD_REF	UVLO	Comparator D Settings
xE1	COMPE_REF	UVLO	Comparator E Settings
xE2	COMPF_REF	UVLO	Comparator F Settings
xE3	COMPG_REF	UVLO	Comparator G Settings
xE4	COMPH_REF	UVLO	Comparator H Settings
xE5	PWRFAULT_MASK1	UVLO	Mask VR Faults from Emergency Shutdown
xE6	PWRFAULT_MASK2	UVLO	Mask VR Faults from Emergency Shutdown
xE7	PGOOD_STAT1	UVLO	VR PGs Statuses
xE8	PGOOD_STAT2	UVLO	VR PGs Statuses
xE9	MISC_BITS	UVLO	Misc. Bits
xEA	STDY_CTRL	RTC	VCOMP and Standby Control
xEB	TEMPCRIT	RTC	VR Critical Temperature
xEC	TEMPHOT	RTC	VR Hot Temperature
xED	OVERCURRENT	RTC	VR Overcurrent
xEE	VREN_PIN_OVR	UVLO	VR Enable Override with Software

6.6.1 Registers

6.6.1.1 VENDORID Register (address = 0x00) [reset = 00100010]

Figure 6-23. VENDORID Register Format

B7	B6	B5	B4	B3	B2	B1	B0
VENDORID[7]	VENDORID[6]	VENDORID[5]	VENDORID[4]	VENDORID[3]	VENDORID[2]	VENDORID[1]	VENDORID[0]
0	0	1	0	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-4. VENDORID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDORID[7:0]	RW	00100010	Vendor ID

6.6.1.2 REVID Register (address = 0x01) [reset = 00000000]

Figure 6-24. REVID Register Format

B7	B6	B5	B4	B3	B2	B1	B0
DNUM[3]	DNUM[2]	DNUM[1]	DNUM[0]	OTPREV[3]	OTPREV[2]	REVID[1]	REVID[0]
0	0	0	1	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-5. REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DNUM[3:0]	RW	0000	Major revision ID **1010**: A **1011**: B **1100**: C **1101**: D **1110**: E **1111**: F
3:2	OTPREV[1:0]	RW	00	Minor revision ID **0000**: 0 **0001**: 1 **0010**: 2 **0011**: 3 **0100**: 4 **0101**: 5 **0110**: 6 **0111**: 7
1:0	REVID[1:0]	RW	00	Minor revision ID **0000**: 0 **0001**: 1 **0010**: 2 **0011**: 3 **0100**: 4 **0101**: 5 **0110**: 6 **0111**: 7

6.6.1.3 IRQLVL1 Register (address = 0x02) [reset = 00000000]

Figure 6-25. IRQLVL1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESET	RESERVED2	PMU	RESERVED1[1]	RESERVED1[0]	PWRSRC	RESERVED	PWRBTN
0	0	0	0	0	0	0	0
RW	R	RW	R	R	RW	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-6. IRQLVL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R	0	RESET interrupt **0**: Not asserted **1**: Asserted
6	RESERVED2	R	0	
5	PMU	R	0	Power monitor interrupt **0**: Not asserted **1**: Asserted
4:3	RESERVED1[1:0]	R	00	
2	PWRSRC	R	0	Power source interrupt **0**: Not asserted **1**: Asserted
1	RESERVED	R	0	
0	PWRBTN	RW	0	Power button interrupt **0**: Not asserted **1**: Asserted, write '1' to clear

6.6.1.4 PWRSRCINT Register (address = 0x04) [reset = 00000000]

Figure 6-26. PWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_PWRSRCINT	LOWBATT2	LOWBATT1	ACOK	PMICHOT	RESERVED[2]	RESERVED[1]	RESERVED[0]
0	0	0	0	0	0	0	0
R	RW	RW	RW	RW	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-7. PWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_PWRSRCINT	R	0	
6	LOWBATT2	RW	0	Low battery2 interrupt [rising-edge detect threshold = 1.25 V; falling-edge hysteresis = 125 mV] **0**: No battery2 detected **1**: Battery2 detected
5	LOWBATT1	RW	0	Low battery1 interrupt [rising-edge detect threshold =1.25 V; falling-edge hysteresis = 125 mV] **0**: No battery1 detected **1**: Battery1 detected
4	ACOK	RW	0	AC/DC adapter detection interrupt. [rising-edge detect threshold =1.25 V; falling-edge hysteresis = 125 mV] **0**: No adapter detected **1**: Adapter detected
3	PMICHOT	RW	0	PMIC internal temperature interrupt **0**: PMIC temperature normal **1**: PMIC temperature hot
2:0	RESERVED[2:0]	R	000	

6.6.1.5 PMUINT Register (address = 0x05) [reset = 00000000]

Figure 6-27. PMUINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED2[2]	RESERVED2[1]	RESERVED2[0]	PMUACOK	RESERVED1_PMUINT	PMUVDC	RESERVED_PMUINT[1]	RESERVED_PMUINT[0]
0	0	0	0	0	0	0	0
R	R	R	RW	R	RW	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-8. PMUINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED2[2:0]	R	000	
4	PMUACOK	RW	0	Adapter detection interrupt **0**: No Interrupt Pending **1**: AC Adapter removed (SACOK H -> L)
3	RESERVED1_PMUINT	R	0	
2	PMUVDC	RW	0	Power monitor critical supply voltage interrupt **0**: Critical supply voltage over threshold limit **1**: Critical supply voltage below threshold limit
1:0	RESERVED_PMUINT[1:0]	R	00	

6.6.1.6 RESETIRQ1 Register (address = 0x08) [reset = 00000000]

Figure 6-28. RESETIRQ1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_RESETIRQ1[1]	RESERVED1_RESETIRQ1[0]	FCO	VRFAULT	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]
0	0	0	0	0	0	0	0
R	R	RW	RW	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-9. RESETIRQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED1_RESETIRQ1[1:0]	R	00	
5	FCO	RW	0	Power button triggered reset interrupt **0**: Power button counter has not forced an emergency reset **1**: Power button counter has forced an emergency reset
4	VRFAULT	RW	0	Voltage regulator triggered reset interrupt **0**: Voltage regulator fault has not triggered an emergency reset **1**: Voltage regulator fault has triggered an emergency reset
3:0	RESERVED[3:0]	R	0000	

6.6.1.7 RESETIRQ2 Register (address = 0x09) [reset = 00000000]

Figure 6-29. RESETIRQ2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1[5]	RESERVED1[4]	RESERVED1[3]	RESERVED1[2]	RESERVED1[1]	RESERVED1[0]	CRITTEMP	RESERVED_RESETIRQ2
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-10. RESETIRQ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED1[5:0]	R	000000	
1	CRITTEMP	RW	0	Temperature triggered reset interrupt **0**: Critical temperature not reached **1**: Critical temperature reached, forcing emergency shutdown
0	RESERVED_RESETIRQ2	R	0	

6.6.1.8 MPMUINT Register (address = 0x0B) [reset = 00010100]

Figure 6-30. MPMUINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED2_MPMUINT[2]	RESERVED2_MPMUINT[1]	RESERVED2_MPMUINT[0]	MPMUACOK	RESERVED1_MPMUINT	MPMUVDC	RESERVED_MPMUINT[1]	RESERVED_MPMUINT[0]
0	0	0	1	0	1	0	0
R	R	R	RW	R	RW	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-11. MPMUINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED2_MPMUINT[2:0]	R	000	
4	MPMUACOK	RW	1	Power monitor critical supply voltage (adapter) mask interrupt **0**: Not masked **1**: Masked
3	RESERVED1_MPMUINT	R	0	
2	MPMUVDC	RW	1	Power monitor critical supply voltage mask interrupt **0**: Not masked **1**: Masked
1:0	RESERVED_MPMUINT[1:0]	R	00	

6.6.1.9 MPWRSRCINT Register (address = 0x0C) [reset = 01111000]

Figure 6-31. MPWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_MPWRSRCINT	MLOWBAT2	MLOWBAT1	MACOK	MPMICHOT	RESERVED_MPWRSRCINT[2]	RESERVED_MPWRSRCINT[1]	RESERVED_MPWRSRCINT[0]
0	1	1	1	1	0	0	0
R	RW	RW	RW	RW	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-12. MPWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_MPWRSRCINT	R	0	
6	MLOWBAT2	RW	1	Low battery voltage mask interrupt **0**: Not masked **1**: Masked
5	MLOWBAT1	RW	1	Low battery voltage mask interrupt **0**: Not masked **1**: Masked
4	MACOK	RW	1	AC/DC adapter detection mask interrupt **0**: Not masked **1**: Masked
3	MPMICHOT	RW	1	PMIC internal temperature mask interrupt **0**: Not masked **1**: Masked
2:0	RESERVED_MPWRSRCINT[2:0]	R	000	

6.6.1.10 RESETIRQ1MASK Register (address = 0x11) [reset = 00110000]

Figure 6-32. RESETIRQ1MASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_RESETIRQ1MASK[1]	RESERVED1_RESETIRQ1MASK[0]	MFCO	MVRFAULT	RESERVED_RESETIRQ1MASK[3]	RESERVED_RESETIRQ1MASK[2]	RESERVED_RESETIRQ1MASK[1]	RESERVED_RESETIRQ1MASK[0]
0	0	1	1	0	0	0	0
R	R	RW	RW	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-13. RESETIRQ1MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED1_RESETIRQ1MASK[1:0]	R	00	
5	MFCO	RW	1	Power button triggered reset mask interrupt **0**: Not masked **1**: Masked
4	MVRFAULT	RW	1	Voltage regulator triggered reset mask interrupt **0**: Not masked **1**: Masked
3:0	RESERVED_RESETIRQ1MASK[3:0]	R	0000	

6.6.1.11 RESETIRQ2MASK Register (address = 0x12) [reset = 00000010]

Figure 6-33. RESETIRQ2MASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_RESETIRQ2MASK[5]	RESERVED1_RESETIRQ2MASK[4]	RESERVED1_RESETIRQ2MASK[3]	RESERVED1_RESETIRQ2MASK[2]	RESERVED1_RESETIRQ2MASK[1]	RESERVED1_RESETIRQ2MASK[0]	MCRITTEMP	RESERVED_RESETIRQ2MASK
0	0	0	0	0	0	1	0
R	R	R	R	R	R	RW	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-14. RESETIRQ2MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED1_RESETIRQ2MASK[5:0]	R	000000	
1	MCRITTEMP	RW	1	Temperature triggered reset mask interrupt **0**: Not masked **1**: Masked
0	RESERVED_RESETIRQ2 MASK	R	0	

6.6.1.12 IRQLVL1msK Register (address = 0x13) [reset = 10100101]

Figure 6-34. IRQLVL1msK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MRESET	RESERVED2_IRQLVL1msK	MPMU	RESERVED1_IRQLVL1msK[1]	RESERVED1_IRQLVL1msK[0]	MPWRSRC	RESERVED_IRQLVL1msK	MPWRBTN
1	0	1	0	0	1	0	1
RW	R	RW	R	R	RW	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-15. IRQLVL1msK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MRESET	RW	1	RESET mask interrupt **0**: Not masked **1**: Masked
6	RESERVED2_IRQLVL1msK	R	0	
5	MPMU	RW	1	Power monitor mask interrupt **0**: Not masked **1**: Masked
4:3	RESERVED1_IRQLVL1msK[1:0]	R	00	
2	MPWRSRC	RW	1	Power source mask interrupt **0**: Not masked **1**: Masked
1	RESERVED_IRQLVL1msK	R	0	
0	MPWRBTN	RW	1	Power button mask interrupt **0**: Not masked **1**: Masked

6.6.1.13 PBCONFIG Register (address = 0x14) [reset = 00011111]

Figure 6-35. PBCONFIG Register Format

B7	B6	B5	B4	B3	B2	B1	B0
PWRBTNDBN	CLRHT	FLT[5]	FLT[4]	FLT[3]	FLT[2]	FLT[1]	FLT[0]
0	0	0	1	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-16. PBCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRBTNDBN	RW	0	Power button debounce **0**: 30 ms **1**: 0 ms (no debounce)
6	CLRHT	RW	0	Reset of power button timer logic **0**: No action **1**: Reset of HT, bit is self clearing
5:0	FLT[5:0]	RW	011111	Time that the button must be held to force an emergency reset **000000**: 0 s **000001**: 1 s **000010**: 2 s **000011**: 3 s **000100**: 4 s **000101**: 5 s **000110**: 6 s **000111**: 7 s **001000**: 8 s **001001**: 9 s **001010**: 10 s .. **011111**: 31 s ... **111100**: 60 s **111101**: 61 s **111110**: 62 s **111111**: 63 s

6.6.1.14 PBSTATUS Register (address = 0x15) [reset = 00000000]

Figure 6-36. PBSTATUS Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PBSTATUS	LVL	HT[5]	HT[4]	HT[3]	HT[2]	HT[1]	HT[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-17. PBSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_PBSTATUS	R	0	
6	LVL	R	0	Power button present level **0**: Power button held **1**: Power button released
5:0	HT[5:0]	R	000000	Time that the button has been held **00000**: Disabled **00001**: Disabled **000010**: 2 s **000011**: 3 s **000100**: 4 s **000101**: 5 s **000110**: 6 s **000111**: 7 s **001000**: 8 s **001001**: 9 s **001010**: 10 s .. ... **111100**: 60 s **111101**: 61 s **111110**: 62 s **111111**: 63 s

6.6.1.15 PWRSTAT1 Register (address = 0x16) [reset = 00000000]

Figure 6-37. PWRSTAT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
VCCIO_FAULT	V5A_DS3_FAULT	V33A_DSW_FAULT	V33A_PCH_FAULT	V18A_FAULT	V18U_25U_FAULT	V12U_FAULT	V06DX_FAULT
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-18. PWRSTAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCCIO_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
6	V5A_DS3_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
5	V33A_DSW_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
4	V33A_PCH_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
3	V18A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
2	V18U_25U_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
1	V12U_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
0	V06DX_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault

6.6.1.16 PWRSTAT2 Register (address = 0x17) [reset = 00000000]

Figure 6-38. PWRSTAT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED[5]	RESERVED[4]	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]	V100A_FAULT	V085A_FAULT
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-19. PWRSTAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED[5:0]	R	000000	
1	V100A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault
0	V085A_FAULT	RW	0	These bits indicate that the VR has lost regulation **0**: Clears register **1**: Indicates power fault

6.6.1.17 PGMASK1 Register (address = 0x18) [reset = 00000000]

Figure 6-39. PGMASK1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MVCCIOPG	MV085APG	MV100APG	MV18APG	MV33APCHPG	MV5ADS3PG	MV33ADSWPG	MV100SPG
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-20. PGMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MVCCIOPG	RW	0	VCCIO PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
6	MV085APG	RW	0	V0.85A PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
5	MV100APG	RW	0	V100A PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
4	MV18APG	RW	0	V1.8A PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
3	MV33APCHPG	RW	0	V3.3A PCH PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
2	MV5ADS3PG	RW	0	V5A DS3 PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
1	MV33ADSWPG	RW	0	V3.3A DSW PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
0	MV100SPG	RW	0	V100S PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)

6.6.1.18 PGMASK2 Register (address = 0x19) [reset = 00000000]

Figure 6-40. PGMASK2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PGMASK2[3]	RESERVED_PGMASK2[2]	RESERVED_PGMASK2[1]	RESERVED_PGMASK2[0]	V18U25UPG	MV12UPG	MV33SPG	MV18SPG
0	0	0	0	0	0	0	0
R	R	R	R	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-21. PGMASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_PGMASK2[3:0]	R	0000	
3	V18U25UPG	RW	0	V1.8_2.5U PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
2	MV12UPG	RW	0	V1.2U PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
1	MV33SPG	RW	0	V3.3S PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)
0	MV18SPG	RW	0	V1.8S PG is part of the power good tree **0**: Power Good function is enabled **1**: Power Good function is masked and set to 1 (not part of the Power Good tree)

6.6.1.19 VCCIOCNT Register (address = 0x30) [reset = 00001010]

Figure 6-41. VCCIOCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VCCIOCNT	CSDECAYEN	VCCIOVSEL[1]	VCCIOVSEL[0]	AOACCNTVCCIO[1]	AOACCNTVCCIO[0]	CTLVVCCIO[1]	CTLVVCCIO[0]
0	0	0	0	1	0	1	0
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-22. VCCIOCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_VCCIOCNT	R	0	
6	CSDECAYEN	RW	0	Enables VCCIO decay when SLP_S0# is asserted. [wait 2us after removing FPWM, before entering DECAY mode. Direct FPWM to DECAY by SLP0Z may cause ringing. Decay exit time within 100us not guaranteed for Vout > 1V.] **0**: VCCIO stays at voltage set by VCCIOVSEL independent of state of SLP_S0# **1**: VCCIO decays to 0V, PGOOD is maintained when SLP_S0# is asserted (low)
5:4	VCCIOVSEL[1:0]	RW	00	Output voltage select **00**: 0.975V **01**: 0.950V **10**: 0.875V **11**: 0.850V
3:2	AOACCNTVCCIO[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLVVCCIO[1:0]	RW	10	Mode control (V4) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.20 V5ADS3CNT Register (address = 0x31) [reset = 00101010]

Figure 6-42. V5ADS3CNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V5ADS3LVSEL[1]	V5ADS3LVSEL[0]	V5ADS3VSEL[1]	V5ADS3VSEL[0]	AOACCNTV5ADS3[1]	AOACCNTV5ADS3[0]	CTLV5ADS3[1]	CTLV5ADS3[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-23. V5ADS3CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V5ADS3LVSEL[1:0]	RW	00	V5ADS3 low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V5ADS3VSEL[1:0] **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V5ADS3VSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3% **01**: Vnom + 2% **10**: Vnom **11**: Vnom - 2%
3:2	AOACCNTV5ADS3[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV5ADS3[1:0]	RW	10	Mode control (V5) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.21 V33ADSWCNT Register (address = 0x32) [reset = 00101010]

Figure 6-43. V33ADSWCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V33ADSWLVSEL[1]	V33ADSWLVSEL[0]	V33ADSWVSEL[1]	V33ADSWVSEL[0]	AOACCNTV33ADSW[1]	AOACCNTV33ADSW[0]	CTLV33ADSW[1]	CTLV33ADSW[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-24. V33ADSWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V33ADSWLVSEL[1:0]	RW	00	V33A_DSW low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V33ADSWVSEL[1:0] **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V33ADSWVSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3% **01**: Vnom + 2% **10**: Vnom **11**: Vnom - 2%
3:2	AOACCNTV33ADSW[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV33ADSW[1:0]	RW	10	Mode control (V6) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.22 V33APCHCNT Register (address = 0x33) [reset = 00001010]

Figure 6-44. V33APCHCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_V33APCHCNT[3]	RESERVED_V33APCHCNT[2]	RESERVED_V33APCHCNT[1]	RESERVED_V33APCHCNT[0]	AOACCNTV33APCH[1]	AOACCNTV33APCH[0]	CTLV33APCH[1]	CTLV33APCH[0]
0	0	0	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-25. V33APCHCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_V33APCHCNT[3:0]	RW	0000	
3:2	AOACCNTV33APCH[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01 **10**: Bits D[1:0] set to 10 **11**: Bits D[1:0] set to 11
1:0	CTLV33APCH[1:0]	RW	10	Mode control (V7) **00**: Disabled **01**: Enabled **10**: Enabled **11**: Enabled

6.6.1.23 V18ACNT Register (address = 0x34) [reset = 00101010]

Figure 6-45. V18ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V18ALVSEL[1]	V18ALVSEL[0]	V18AVSEL[1]	V18AVSEL[0]	AOACCNTV18A[1]	AOACCNTV18A[0]	CTLV18A[1]	CTLV18A[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-26. V18ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V18ALVSEL[1:0]	RW	00	V18A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V18AVSEL[1:0] **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V18AVSEL[1:0]	RW	10	Output voltage select **00**: Vnom + 3% **01**: Vnom + 2% **10**: Vnom **11**: Vnom - 2%
3:2	AOACCNTV18A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV18A[1:0]	RW	10	Mode control (V8) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.24 V18U25UCNT Register (address = 0x35) [reset = 00001010]

Figure 6-46. V18U25UCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_V18U25UCNT[3]	RESERVED_V18U25UCNT[2]	RESERVED_V18U25UCNT[1]	RESERVED_V18U25UCNT[0]	AOACCNTV18U25U[1]	AOACCNTV18U25U[0]	CTLV18U25U[1]	CTLV18U25U[0]
0	0	0	0	1	0	1	0
R	R	R	R	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-27. V18U25UCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_V18U25UCNT[3:0]	R	0000	
3:2	AOACCNTV18U25U[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01 **10**: Bits D[1:0] set to 10 **11**: Bits D[1:0] set to 11
1:0	CTLV18U25U[1:0]	RW	10	Mode control (V9) **00**: Disabled **01**: Enabled **10**: Enabled **11**: Enabled

6.6.1.25 V1P2UCNT Register (address = 0x36) [reset = 00111010]

Figure 6-47. V1P2UCNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V1P2ULVSEL	V1P2UVSEL[2]	V1P2UVSEL[1]	V1P2UVSEL[0]	AOACCNTV1P2U[1]	AOACCNTV1P2U[0]	CTLV1P2U[1]	CTLV1P2U[0]
0	0	1	1	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-28. V1P2UCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V1P2ULVSEL	RW	0	V1.2U low power mode output voltage set point - set at assertion of SLP_S0# **0**: Disabled, voltage stays at value set by V1P2UVSEL **1**: Vnom - 3%
6:4	V1P2UVSEL[2:0]	RW	011	Output voltage select **000**: Vnom + 3% **001**: Vnom + 2% **010**: Vnom + 1% **011**: Vnom + 0% **100**: Vnom - 1% **101**: Vnom - 2% **110**: Vnom - 3% **111**: Vnom -4%
3:2	AOACCNTV1P2U[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: no change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV1P2U[1:0]	RW	10	Mode control (V10) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.26 V100ACNT Register (address = 0x37) [reset = 00011010]

Figure 6-48. V100ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V100ALVSEL[1]	V100ALVSEL[0]	V100AVSEL[1]	V100AVSEL[0]	AOACCNTV100A[1]	AOACCNTV100A[0]	CTLV100A[1]	CTLV100A[0]
0	0	0	1	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-29. V100ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V100ALVSEL[1:0]	RW	00	V100A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V100AVSEL[1:0] **01**: Vnom - 4% **10**: Vnom - 3% **11**: Vnom - 2%
5:4	V100AVSEL[1:0]	RW	01	Output voltage select **00**: Vnom + 5% (1.05 V) **01**: Vnom (1 V) **10**: Vnom - 2.5% (0.975 V) **11**: Vnom - 5% (0.95V)
3:2	AOACCNTV100A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV100A[1:0]	RW	10	Mode control (V11) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.27 V085ACNT Register (address = 0x38) [reset = 00101010]

Figure 6-49. V085ACNT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V085ALVSEL[1]	V085ALVSEL[0]	V085AVSEL[1]	V085AVSEL[0]	AOACCNTV085A[1]	AOACCNTV085A[0]	CTLV085A[1]	CTLV085A[0]
0	0	1	0	1	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-30. V085ACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V085ALVSEL[1:0]	RW	00	V085A low power mode output voltage set point - set at assertion of SLP_S0# **00**: Disabled, voltage stays at value set by V085AVSEL[1:0] **01**: 0.70 V **10**: 0.75 V **11**: 0.80 V
5:4	V085AVSEL[1:0]	RW	00	Output voltage select **00**: 0.95 V **01**: 0.90 V **10**: 0.85 V **11**: 0.80 V
3:2	AOACCNTV085A[1:0]	RW	10	Mode control for exit standby (rising edge of SLP_S0#) - changes bits D[1:0] on exit **00**: No change in bits D[1:0] - fast change mode disabled **01**: Bits D[1:0] set to 01, Auto Mode, (automatic transition from PFM to PWM) **10**: Bits D[1:0] set to 10, Auto Mode, (automatic transition from PFM to PWM) **11**: Bits D[1:0] set to 11, forced PWM operation
1:0	CTLV085A[1:0]	RW	10	Mode control (V12) **00**: Converter disabled **01**: Auto Mode, (automatic transition from PFM to PWM) **10**: Auto Mode, (automatic transition from PFM to PWM) **11**: Forced PWM operation

6.6.1.28 VRMODECTRL Register (address = 0x3B) [reset = 00111111]

Figure 6-50. VRMODECTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VRMODECTRL[1]	RESERVED_VRMODECTRL[0]	V33ADSW_LPM	VCCIO_LPM	V085A_LPM	V12U_LPM	V100A_LPM	V5ADS3_LPM
0	0	1	1	1	1	1	1
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-31. VRMODECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_VRMODECTRL[1:0]	R	00	
5	V33ADSW_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLV33ADSW [1:0] bits of V33ADSWCNT register. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register V33ADSWCNT, bits CTLV33ADSW [1:0] when STANDBY# is low} **1**: Mode set by CTLV33ADSW [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLV33ADSW [1:0] when STANDBY# is low}
4	VCCIO_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLVCCIO [1:0] bits of VCCIOCNT register. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register VCCIOCNT, bits CTLVCCIO [1:0] when STANDBY# is low} **1**: Mode set by CTLVCCIO [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLVCCIO [1:0] when STANDBY# is low}
3	V085A_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLV085A [1:0] register. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register V085ACNT, bits CTLV085A [1:0] when STANDBY# is low} **1**: Mode set by CTLV085A [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLV085A [1:0] when STANDBY# is low}
2	V12U_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLV12U [1:0] bits in V12UCNT register. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register V12UCNT, bits CTLV12U [1:0] when STANDBY# is low} **1**: Mode set by CTLV12U [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLV12U [1:0] when STANDBY# is low}
1	V100A_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLV100A [1:0] bits in V100ACNTregister. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register V100ACNT, bits CTLV100A [1:0] when STANDBY# is low} **1**: Mode set by CTLV100A [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLV100A[1:0] when STANDBY# is low}
0	V5ADS3_LPM	RW	1	Force low power mode (Auto mode). This is only used if forcing PWM in CTLV5ADS3 [1:0] bits in V5ADS3CNT register. **0**: Force Auto mode when STANDBY# (SLP_S0#) is asserted (low) {Over-rides setting of register V5ADS3,CNT bits CTLVV33ADSW [1:0] when STANDBY# is low} **1**: Mode set by CTLV5ADS3 [1:0] bits when STANDBY# (SLP_S0#) {Does what is setting of register bits CTLV5ADS3 [1:0] when STANDBY# is low}

6.6.1.29 DISCHCNT1 Register (address = 0x3C) [reset = 00000000]

Figure 6-51. DISCHCNT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_DISCHCNT1[5]	RESERVED_DISCHCNT1[4]	RESERVED_DISCHCNT1[3]	RESERVED_DISCHCNT1[2]	RESERVED_DISCHCNT1[1]	RESERVED_DISCHCNT1[0]	VCCIODISCHG[1]	VCCIODISCHG[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-32. DISCHCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_DISCHCNT1[5:0]	R	000000	
1:0	VCCIODISCHG[1:0]	RW	00	VCCIO discharge resistance at VSD, (TPS650831 at FBVR3P) **00**: >1000 kΩ **01**: 125 Ω **10**: 225 Ω **11**: 550 Ω

6.6.1.30 DISCHCNT2 Register (address = 0x3D) [reset = 00000000]

Figure 6-52. DISCHCNT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V5ADS3DISCHG[1]	V5ADS3DISCHG[0]	V33ADSWDISCHG[1]	V33ADSWDISCHG[0]	V33PCHDISCHG[1]	V33PCHDISCHG[0]	V18ADISCH[1]	V18ADISCH[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-33. DISCHCNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V5ADS3DISCHG[1:0]	RW	00	V5ADS3 discharge resistance at FBVR5P, (TPS650831 at VSC) **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5:4	V33ADSWDISCHG[1:0]	RW	00	V33A_DSW discharge resistance at FBVR3P, (TPS650831 at VSD) **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3:2	V33PCHDISCHG[1:0]	RW	00	V33A_PCH discharge resistance at VSA **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1:0	V18ADISCH[1:0]	RW	00	V18A discharge resistance at FBVR2P, (TPS650831 at FBVR5P) **00**: 860 Ω **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

6.6.1.31 DISCHCNT3 Register (address = 0x3E) [reset = 00000000]

Figure 6-53. DISCHCNT3 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V18U25UDISCHG[1]	V18U25UDISCHG[0]	V12UDISCHG[1]	V12UDISCHG[0]	V100ADISCHG[1]	V100ADISCHG[0]	V085ADISCH[1]	V085ADISCH[0]
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-34. DISCHCNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	V18U25UDISCHG[1:0]	RW	00	V1.8U_2.5U discharge resistance at VSB **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5:4	V12UDISCHG[1:0]	RW	00	V1.2U discharge resistance at FBVR4P **00**: >1000 kΩ **01**: 125 Ω **10**: 225 Ω **11**: 550 Ω
3:2	V100ADISCHG[1:0]	RW	00	V100A discharge resistance at FBVR1P **00**: >1000 kΩ **01**: 125 Ω **10**: 225 Ω **11**: 550 Ω
1:0	V085ADISCH[1:0]	RW	00	V085A discharge resistance, (TPS650831 at FBVR2P) **00**: >1000 kΩ **01**: 150 Ω **10**: 250 Ω **11**: 575 Ω

6.6.1.32 DISCHCNT4 Register (address = 0x3F) [reset = 00000000]

Figure 6-54. DISCHCNT4 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_DISCHCNT4[1]	RESERVED_DISCHCNT4[0]	V33SDISCHG[1]	V33SDISCHG[0]	V18SDISCHG[1]	V18SDISCHG[0]	V100SDISCH[1]	V100SDISCH[0]
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-35. DISCHCNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_DISCHCNT4[1:0]	R	00	
5:4	V33SDISCHG[1:0]	RW	00	V3.3S discharge resistance at VSE **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3:2	V18SDISCHG[1:0]	RW	00	V18S discharge resistance at VSF **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1:0	V100SDISCH[1:0]	RW	00	V100S discharge resistance at VSG **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

6.6.1.33 PWRGDCNT1 Register (address = 0x40) [reset = 01011111]

Figure 6-55. PWRGDCNT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PWRGDCNT1	RSMRSTN_PWRGD[1]	RSMRSTN_PWRGD[0]	PCH_PWROK[1]	PCH_PWROK[0]	DEL_ALL_SYS_PWRGD[2]	DEL_ALL_SYS_PWRGD[1]	DEL_ALL_SYS_PWRGD[0]
0	1	0	1	1	1	1	1
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-36. PWRGDCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_PWRGDCNT1	R	0	
6:5	RSMRSTN_PWRGD[1:0]	RW	10	Delay of RSMRSTN_PWRGD, [RTC = 30.5 µs ±10%] **00**: No Delay **01**: 164x RTC (5.5 ms) **10**: 360x RTC (11 ms) **11**: 721x RTC (22 ms)
4:3	PCH_PWROK[1:0]	RW	11	Delay of PCH_PWROK compared to ALL_SYS_PWRGD, [RTC = 30.5 µs ±10%] **00**: 82x RTC (2.5 ms) **01**: 164x RTC (5 ms) **10**: 328x RTC (10 ms) **11**: 656x RTC (20 ms)
2:0	DEL_ALL_SYS_PWRGD[2:0]	RW	111	Delay of SYS_PWR_OK compared to ALL_SYS_PWRGD, [RTC = 30.5 µs ±10%] **000**: 82x RTC (2.5 ms) **001**: 164x RTC (5 ms) **010**: 328x RTC (10 ms) **011**: 492x RTC (15 ms) **100**: 656x RTC (20 ms) **101**: 1640x RTC (50 ms) **110**: 2460x RTC (75 ms) **111**: 3280x RTC (100 ms)

6.6.1.34 VREN Register (address = 0x41) [reset = 00000000]

Figure 6-56. VREN Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VREN[5]	RESERVED_VREN[4]	RESERVED_VREN[3]	RESERVED_VREN[2]	RESERVED_VREN[1]	RESERVED_VREN[0]	EC_SLP_S4	EC_DS4
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-37. VREN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_VREN[5:0]	RW	000000	
1	EC_SLP_S4	RW	0	**0**: Disable **1**: Enable
0	EC_DS4	RW	0	**0**: Disable **1**: Enable

6.6.1.35 REGLOCK Register (address = 0x42) [reset = 00000000]

Figure 6-57. REGLOCK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED[6]	RESERVED[5]	RESERVED[4]	RESERVED[3]	RESERVED[2]	RESERVED[1]	RESERVED[0]	CNTLOCK
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-38. REGLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED[6:0]	R	0000000	
0	CNTLOCK	RW	0	Locks all V*CNT registers **0**: All V*CNT registers are unlocked and can be overwritten **1**: All V*CNT registers are locked and cannot be overwritten

6.6.1.36 VRENPINMASK Register (address = 0x43) [reset = 00000000]

Figure 6-58. VRENPINMASK Register Format

B7	B6	B5	B4	B3	B2	B1	B0
MV12EN	MV11EN	MV10EN	MV9EN	MV8EN	MV7EN	MV5EN	MV4EN
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-39. VRENPINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MV12EN	RW	0	V12 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
6	MV11EN	RW	0	V11 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
5	MV10EN	RW	0	V10 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
4	MV9EN	RW	0	V9 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
3	MV8EN	RW	0	V8 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
2	MV7EN	RW	0	V7 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
1	MV5EN	RW	0	V5 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
0	MV4EN	RW	0	V4 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable

6.6.1.37 RSTCTRL Register (address = 0x48) [reset = 00011100]

Figure 6-59. RSTCTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_RSTCTRL[2]	RESERVED_RSTCTRL[1]	RESERVED_RSTCTRL[0]	TRST[1]	TRST[0]	VTHRST[2]	VTHRST[1]	VTHRST[0]
0	0	0	1	1	1	0	0
R	R	R	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-40. RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED_RSTCTRL[2:0]	R	000	
4:3	TRST[1:0]	RW	11	Reset time duration **00**: 20 ms **01**: 40 ms **10**: 80 ms **11**: 200 ms
2:0	VTHRST[2:0]	RW	100	Reset voltage threshold **000**: 1.4 V **001**: 1.5 V **010**: 1.6 V **011**: 1.7 V **100**: 2.4 V **101**: 2.6 V **110**: 2.8 V **111**: 3.0 V

6.6.1.38 SDWNCTRL Register (address = 0x49) [reset = 00000000]

Figure 6-60. SDWNCTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_SDWNCTRL[6]	RESERVED_SDWNCTRL[5]	RESERVED_SDWNCTRL[4]	RESERVED_SDWNCTRL[3]	RESERVED_SDWNCTRL[2]	RESERVED_SDWNCTRL[1]	RESERVED_SDWNCTRL[0]	SDWN
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-41. SDWNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED_SDWNCTRL[6:0]	R	0000000	
0	SDWN	RW	0	Forced emergency reset, bit is self clearing **0**: No action **1**: Force emergency reset

6.6.1.39 VDLMTCRT Register (address = 0x51) [reset = 00000101]

Figure 6-61. VDLMTCRT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_VDLMTCRT	VDLMTCOMP	TDBNCVDLMTCRT[1]	TDBNCVDLMTCRT[0]	VDLMTCRTH[3]	VDLMTCRTH[2]	VDLMTCRTH[1]	VDLMTCRTH[0]
0	0	0	0	0	1	0	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-42. VDLMTCRT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED_VDLMTCRT	RW	0	
6	VDLMTCOMP	RW	0	Critical supply voltage comparator for VDCSNS pin input voltage sense. Connect voltage divider resistors from VIN to detect when input voltage is low **0**: disable **1**: enable
5:4	TDBNCVDLMTCRT[1:0]	RW	00	Supply voltage monitor debounce of VDCSNS input voltage sense pin **00**: No Deglitch **01**: 10 µs **10**: 1x RTC (30us) **11**: 2x RTC (60us)
3:0	VDLMTCRTH[3:0]	RW	0101	Critical supply voltage falling threshold on VDCSNS pin. Connect voltage divider resistors from VIN to detect when input voltage is low. For 2S should be 4X top resistor, X bottom resistor. [rising hysteresis = 20 mV] **0000**: no limit **0001**: 1.2 V **0010**: 1.18 V **0011**: 1.16 V **0100**: 1.14 V **0101**: 1.12 V **0110**: 1.10 V **0111**: 1.08 V **1xxx**: NA

6.6.1.40 ACOKDBDM Register (address = 0x69) [reset = 00001111]

Figure 6-62. ACOKDBDM Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_ACOKDBDM[3]	RESERVED_ACOKDBDM[2]	RESERVED_ACOKDBDM[1]	RESERVED_ACOKDBDM[0]	ACOKDB[1]	ACOKDB[0]	ACOKDM[1]	ACOKDM[0]
0	0	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-43. ACOKDBDM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED_ACOKDBDM[3:0]	RW	0000	
3:2	ACOKDB[1:0]	RW	11	Adapter detection debounce time **00**: 81 µs **01**: 10 ms **10**: 20 ms **11**: 30 ms
1:0	ACOKDM[1:0]	RW	11	Adapter detection mode **00**: reserved **01**: low-to-high **10**: high-to-low **11**: both, low-to-high and high-to-low

6.6.1.41 LOWBATTDET Register (address = 0x6A) [reset = 11111000]

Figure 6-63. LOWBATTDET Register Format

B7	B6	B5	B4	B3	B2	B1	B0
LOWBATTDB[1]	LOWBATTDB[0]	LOWBATT2_EN	LOWBATT1_EN	ACIN_EN	RESERVED_LOWBATTDET[2]	RESERVED_LOWBATTDET[1]	RESERVED_LOWBATTDET[0]
1	1	1	1	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-44. LOWBATTDET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	LOWBATTDB[1:0]	RW	11	Low battery detection debounce time **00**: 4 RTC periods (120 µs) **01**: 32 RTC periods (960 µs) **10**: 64 RTC periods (1920 µs) **11**: 128 RTC periods (3840 µs)
5	LOWBATT2_EN	RW	1	Low battery Two detection Enable **0**: Disable **1**: Enable
4	LOWBATT1_EN	RW	1	Low battery One detection Enable **0**: Disable **1**: Enable
3	ACIN_EN	RW	1	AC IN Comparator **0**: Disable **1**: Enable
2:0	RESERVED_LOWBATTDET[2:0]	RW	000	

6.6.1.42 SPWRSRCINT Register (address = 0x6F) [reset = 00000000]

Figure 6-64. SPWRSRCINT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED1_SPWRSRCINT	SLOWBATT2	SLOWBATT1	SACOK	RESERVED_SPWRSRCINT[3]	RESERVED_SPWRSRCINT[2]	RESERVED_SPWRSRCINT[1]	RESERVED_SPWRSRCINT[0]
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-45. SPWRSRCINT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED1_SPWRSRCINT	R	0	
6	SLOWBATT2	R	0	LOWBATT2 detection status **0**: BATT2 above threshold **1**: BATT2 below threshold
5	SLOWBATT1	R	0	LOWBATT1 detection status **0**: BATT1 above threshold **1**: BATT1 below threshold
4	SACOK	R	0	AC adapter (ACOK) detection status **0**: Adapter removed **1**: Adapter inserted
3:0	RESERVED_SPWRSRCINT[3:0]	R	0000	

6.6.1.43 CLKCTRL1 Register (address = 0xD0) [reset = 00000000]

Figure 6-65. CLKCTRL1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_CLKCTRL1[6]	RESERVED_CLKCTRL1[5]	RESERVED_CLKCTRL1[4]	RESERVED_CLKCTRL1[3]	RESERVED_CLKCTRL1[2]	RESERVED_CLKCTRL1[1]	RESERVED_CLKCTRL1[0]	ECWAKEEN
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-46. CLKCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED_CLKCTRL1[6:0]	RW	0000000	
0	ECWAKEEN	RW	0	**1** Hz clock **0**: clock OFF **1**: Clock ON

6.6.1.44 COMPA_REF Register (address = 0xDD) [reset = 00000000]

Figure 6-66. COMPA_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPA_MODE	COMPA_DVS[3]	COMPA_DVS[2]	COMPA_DVS[1]	COMPA_DVS[0]	COMPA_VSEL[2]	COMPA_VSEL[1]	COMPA_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-47. COMPA_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPA_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPA_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPA_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.45 COMPB_REF Register (address = 0xDE) [reset = 00000000]

Figure 6-67. COMPB_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPB_MODE	COMPB_DVS[3]	COMPB_DVS[2]	COMPB_DVS[1]	COMPB_DVS[0]	COMPB_VSEL[2]	COMPB_VSEL[1]	COMPB_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-48. COMPB_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPB_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPB_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPB_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.46 COMPC_REF Register (address = 0xDF) [reset = 00000000]

Figure 6-68. COMPC_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPC_MODE	COMPC_DVS[3]	COMPC_DVS[2]	COMPC_DVS[1]	COMPC_DVS[0]	COMPC_VSEL[2]	COMPC_VSEL[1]	COMPC_VSEL[0]
1	0	0	0	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-49. COMPC_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPC_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPC_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPC_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.47 COMPD_REF Register (address = 0xE0) [reset = 00000000]

Figure 6-69. COMPD_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPD_MODE	COMPD_DVS[3]	COMPD_DVS[2]	COMPD_DVS[1]	COMPD_DVS[0]	COMPD_VSEL[2]	COMPD_VSEL[1]	COMPD_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-50. COMPD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPD_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPD_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPD_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.48 COMPE_REF Register (address = 0xE1) [reset = 00000000]

Figure 6-70. COMPE_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPE_MODE	COMPE_DVS[3]	COMPE_DVS[2]	COMPE_DVS[1]	COMPE_DVS[0]	COMPE_VSEL[2]	COMPE_VSEL[1]	COMPE_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-51. COMPE_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPE_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPE_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPE_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.49 COMPF_REF Register (address = 0xE2) [reset = 00000000]

Figure 6-71. COMPF_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPF_MODE	COMPF_DVS[3]	COMPF_DVS[2]	COMPF_DVS[1]	COMPF_DVS[0]	COMPF_VSEL[2]	COMPF_VSEL[1]	COMPF_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-52. COMPF_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPF_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPF_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPF_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.50 COMPG_REF Register (address = 0xE3) [reset = 00000000]

Figure 6-72. COMPG_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPG_MODE	COMPG_DVS[3]	COMPG_DVS[2]	COMPG_DVS[1]	COMPG_DVS[0]	COMPG_VSEL[2]	COMPG_VSEL[1]	COMPG_VSEL[0]
X	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-53. COMPG_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPG_Mode	RW	0	Comparator Mode: **0**: PGOOD Mode **1**: Comparator Mode
6:3	COMPG_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPG_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.51 COMPH_REF Register (address = 0xE4) [reset = 00000000]

Figure 6-73. COMPH_REF Register Format

B7	B6	B5	B4	B3	B2	B1	B0
COMPH_DISCHG	COMPH_DVS[3]	COMPH_DVS[2]	COMPH_DVS[1]	COMPH_DVS[0]	COMPH_VSEL[2]	COMPH_VSEL[1]	COMPH_VSEL0]
0	X	X	X	X	X	X	X
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-54. COMPH_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	COMPH_DISCHG	RW	0	Comparator H Discharge value **0**: No discharge **1**: 100 Ω
6:3	COMPH_DVS[3:0]	RW	0000	Comparator Window Voltage Shifting: % deviation from VSEL if VSEL >1.05V or second voltage option if VSEL = 1 V 0000 = + 3% or 1.05 V 0001 = + 2% or 1 V 0010 = + 1% or 0.975 V 0011 = + 0% or 0.95 V 0100 = - 1% or 0.9 V 0101 = - 2% or 0.875 V 0110 = - 3% or 0.85 V 0111 = - 4% or 0.8 V 1000 = 0.75 V 1001 = 0.7 V
2:0	COMPH_VSEL[2:0]	RW	000	Comparator Window Voltage Select: 000 = 1 V 001 = 1.2 V 010 = 1.5 V 011 = 1.8 V 100 = 1.1 V 101 = 1.35 V 110 = 3.3 V 111 = 2.5 V / 5 V

6.6.1.52 PWFAULT_MASK1 Register (address = 0xE5) [reset = 00000000]

Figure 6-74. PWFAULT_MASK1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V4_FLTmsK	V5_FLTmsK	V6_FLTmsK	V7_FLTmsK	V8_FLTmsK	V9_FLTmsK	V10_FLTmsK	V13_FLTmsK
0	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-55. PWFAULT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V4_FLTmsK	RW	0	V4 Power Fault Masked **0**: Not Masked **1**: Masked
6	V5_FLTmsK	RW	0	V5 Power Fault Masked **0**: Not Masked **1**: Masked
5	V6_FLTmsK	RW	0	V6 Power Fault Masked **0**: Not Masked **1**: Masked
4	V7_FLTmsK	RW	0	V7 Power Fault Masked **0**: Not Masked **1**: Masked
3	V8_FLTmsK	RW	0	V8 Power Fault Masked **0**: Not Masked **1**: Masked
2	V9_FLTmsK	RW	0	V9 Power Fault Masked **0**: Not Masked **1**: Masked
1	V10_FLTmsK	RW	0	V10 Power Fault Masked **0**: Not Masked **1**: Masked
0	V13_FLTmsK	RW	0	V13 Power Fault Masked **0**: Not Masked **1**: Masked

6.6.1.53 PWFAULT_MASK2 Register (address = 0xE6) [reset = 00000000]

Figure 6-75. PWFAULT_MASK2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PWFAULT_MASK2[5]	RESERVED_PWFAULT_MASK2[4]	RESERVED_PWFAULT_MASK2[3]	RESERVED_PWFAULT_MASK2[2]	RESERVED_PWFAULT_MASK2[1]	RESERVED_PWFAULT_MASK2[0]	V11_FLTmsK	V12_FLTmsK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-56. PWFAULT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED_PWFAULT_MASK2[5:0]		000000	Read Always Returns '1'
1	V11_FLTmsK		0	V11 Power Fault Masked **0**: Not Masked **1**: Masked
0	V12_FLTmsK		0	V12 Power Fault Masked **0**: Not Masked **1**: Masked

6.6.1.54 PGOOD_STAT1 Register (address = 0xE7) [reset = 00000000]

Figure 6-76. PGOOD_STAT1 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V13_PGOOD	V10_PGOOD	V9_PGOOD	V8_PGOOD	V7_PGOOD	V6_PGOOD	V5_PGOOD	V4_PGOOD
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-57. PGOOD_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V13_PGOOD	R	0	V13 PGOOD STATUS **0**: Fail **1**: Pass
6	V10_PGOOD	R	0	V10 PGOOD STATUS **0**: Fail **1**: Pass
5	V9_PGOOD	R	0	V9 PGOOD STATUS **0**: Fail **1**: Pass
4	V8_PGOOD	R	0	V8 PGOOD STATUS **0**: Fail **1**: Pass
3	V7_PGOOD	R	0	V7 PGOOD STATUS **0**: Fail **1**: Pass
2	V6_PGOOD	R	0	V6 PGOOD STATUS **0**: Fail **1**: Pass
1	V5_PGOOD	R	0	V5 PGOOD STATUS **0**: Fail **1**: Pass
0	V4_PGOOD	R	0	V4 PGOOD STATUS **0**: Fail **1**: Pass

6.6.1.55 PGOOD_STAT2 Register (address = 0xE8) [reset = 00000000]

Figure 6-77. PGOOD_STAT2 Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_PGOOD_STAT2[2]	RESERVED_PGOOD_STAT2[1]	RESERVED_PGOOD_STAT2[0]	V12_PGOOD	V11_PGOOD	V11_SPGD	V8_SPGD	V6_SPGD
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-58. PGOOD_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED_PGOOD_STAT2[2:0]	R	000	Read Always Returns '1'
4	V12_PGOOD	R	0	V12 PGOOD STATUS **0**: Fail **1**: Pass
3	V11_PGOOD	R	0	V11 PGOOD STATUS **0**: Fail **1**: Pass
2	V11_SPGD	R	0	V11S PGOOD STATUS **0**: Fail **1**: Pass
1	V8_SPGD	R	0	V8S PGOOD STATUS **0**: Fail **1**: Pass
0	V6_SPGD	R	0	V6S PGOOD STATUS **0**: Fail **1**: Pass

6.6.1.56 MISC_BITS Register (address = 0xE9) [reset = 00010000]

Figure 6-78. MISC_BITS Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V13_PIN_OVR	MV13EN	V6_PIN_OVR	MV6EN	msLP_S3ZPG	msLP_SUSZPG	BC_ACOK_EN	V13DISCHG
0	0	0	0	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-59. MISC_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V13_PIN_OVR	RW	0	V13 ENABLE PIN Over Ride **0**: V13 is OFF if MV13EN is '1' **1**: V13 is ON if MV13EN is '1'
6	MV13EN	RW	0	V13 Enable Pin Mask **0**: DDR_VT_CTRL Pin controls V13 **1**: V13_EN_PIN Bit [Bit(3)] controls V13
5	V6_PIN_OVR	RW	0	V6 ENABLE PIN Over Ride **0**: V6 Pin controls V6 **1**: V6 is ON if VREN PIN MASK = '0'
4	MV6EN	RW	1	V6 Enable Pin Mask **0**: VR Enable Pin controls VR enable **1**: VR Enable Pin masked V*CTLV controls VR enable
3	msLP_S3ZPG	RW	0	SLP_S3Z is part of the power good tree **0**: SLP_S3Z is part of Power Good Tree **1**: SLP_S3Z is masked and set to 1 (not part of the Power Good tree)
2	msLP_SUSZPG	RW	0	SLP_SUSZ is part of the power good tree **0**: SLP_SUSZ is part of Power Good Tree **1**: SLP_SUSZ is masked and set to 1 (not part of the Power Good tree)
1	BC_ACOK_EN	RW	1	Enables BC_ACOK output out of LVA pin. The in put is ACOK pin, instead of ENLVA pin. **0**: LVA pin is not BC_ACOK, and ENLVA is the input for LVA output, behaving as a general purpose level-shifter. **1**: LVA pin is BC_ACOK, and ACOK is the input, and ENLVA is not functional. BC_ACOK is a level-shifted version of ACOK.
0	V13DISCHG	RW	0	V0.6DX discharge resistance (V13) **0**: No discharge **1**: 100 Ω

6.6.1.57 STDBY_CTRL Register (address = 0xEA) [reset = 11111110]

Figure 6-79. STDBY_CTRL Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_STDBY_CTRL[4]	RESERVED_STDBY_CTRL[3]	RESERVED_STDBY_CTRL[2]	RESERVED_STDBY_CTRL[1]	RESERVED_STDBY_CTRL[0]	EN_VCOMP_10U	VCOMPEN	QLSLPS0_ACTIVE
1	1	1	1	1	1	1	0
R	R	R	R	R	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-60. STDBY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED_STDBY_CTRL[4:0]	R	11111	Read Always Returns '1'
2	EN_VCOMP_10U	RW	1	VCOMP Current Source Control bit: **0**: Disable **1**: Enable
1	VCOMPEN	RW	1	VCOMP Enable Control bit: **0**: Disable **1**: Enable
0	QLSLPS0_ACTIVE	RW	0	SLP_S0 & DDR_VTT_CTRL Detect logic Control **0**: Normal Operation DELAY_ALL_SYS_PG is used in QSTANDBY# (SLP_S0#) **1**: DELAY_ALL_SYS_PG is ignored for QSTANDBY# (SLP_S0#)

6.6.1.58 TEMPCRIT Register (address = 0xEB) [reset = 00000000]

Figure 6-80. TEMPCRIT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_TEMPCRIT[1]	RESERVED_TEMPCRIT[0]	LDO1_CRIT	VR5_CRIT	VR4_CRIT	VR3_CRIT	VR2_CRIT	VR1_CRIT
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-61. TEMPCRIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_TEMPCRIT[1:0]	R	00	Read Always Returns '0'
5	LDO1_CRIT	RW	0	LDO1 CRITTEMP **0**: Not asserted, **1**: Asserted, Regulator at critical temperature, write '1' to clear
4	VR5_CRIT	RW	0	VR5 CRITTEMP **0**: Not asserted **1**: Asserted, Regulator at critical temperature, write '1' to clear
3	VR4_CRIT	RW	0	VR4 CRITTEMP **0**: Not asserted **1**: Asserted, Regulator at critical temperature, write '1' to clear
2	VR3_CRIT	RW	0	VR3 CRITTEMP **0**: Not asserted **1**: Asserted, Regulator at critical temperature, write '1' to clear
1	VR2_CRIT	RW	0	VR2 CRITTEMP **0**: Not asserted **1**: Asserted, Regulator at critical temperature, write '1' to clear
0	VR1_CRIT	RW	0	VR1 CRITTEMP **0**: Not asserted **1**: Asserted, Regulator at critical temperature, write '1' to clear

6.6.1.59 TEMPHOT Register (address = 0xEC) [reset = 00000000]

Figure 6-81. TEMPHOT Register Format

B7	B6	B5	B4	B3	B2	B1	B0
RESERVED_TEMPHOT[1]	RESERVED_TEMPHOT[0]	LDO1_HOT	VR5_HOT	VR4_HOT	VR3_HOT	VR2_HOT	VR1_HOT
0	0	0	0	0	0	0	0
R	R	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-62. TEMPHOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED_TEMPHOT[1:0]	R	00	Read Always Returns '1'
5	LDO1_HOT	RW	0	LDO1 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear
4	VR5_HOT	RW	0	VR5 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear
3	VR4_HOT	RW	0	VR4 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear
2	VR3_HOT	RW	0	VR3 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear
1	VR2_HOT	RW	0	VR2 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear
0	VR1_HOT	RW	0	VR1 HOT TEMP **0**: Not asserted **1**: Asserted, write '1' to clear

6.6.1.60 VREN_PIN_OVR Register (address = 0xEE) [reset = 00000000]

Figure 6-82. VREN_PIN_OVR Register Format

B7	B6	B5	B4	B3	B2	B1	B0
V12_PIN_OVR	V11_PIN_OVR	V10_PIN_OVR	V9_PIN_OVR	V8_PIN_OVR	V7_PIN_OVR	V5_PIN_OVR	V4_PIN_OVR
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6-63. VREN_PIN_OVR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	V12_PIN_OVR	RW	0	V12 ENABLE PIN Over Ride **0**: V12 Pin controls V12 **1**: V12 is ON if VREN PIN MASK = '0'
6	V11_PIN_OVR	RW	0	V11 ENABLE PIN Over Ride **0**: V11 Pin controls V11 **1**: V11 is ON if VREN PIN MASK = '0'
5	V10_PIN_OVR	RW	0	V10 ENABLE PIN Over Ride **0**: V10 Pin controls V10 **1**: V10 is ON if VREN PIN MASK = '0'
4	V9_PIN_OVR	RW	0	V9 ENABLE PIN Over Ride **0**: V9 Pin controls V9 **1**: V9 is ON if VREN PIN MASK = '0'
3	V8_PIN_OVR	RW	0	V8 ENABLE PIN Over Ride **0**: V8 Pin controls V8 **1**: V8 is ON if VREN PIN MASK = '0'
2	V7_PIN_OVR	RW	0	V7 ENABLE PIN Over Ride **0**: V7 Pin controls V7 **1**: V7 is ON if VREN PIN MASK = '0'
1	V5_PIN_OVR	RW	0	V5 ENABLE PIN Over Ride **0**: V5 Pin controls V5 **1**: V5 is ON if VREN PIN MASK = '0'
0	V4_PIN_OVR	RW	0	V4 ENABLE PIN Over Ride **0**: V4 Pin controls V4 **1**: V4 is ON if VREN PIN MASK = '0'

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPS65083x can be used in several different applications from computing, industrial interfacing and much more. This section describes the general application information and provides more detailed description on the TPS65083x powering the Intel SkyLake and Kabylake system.

7.2 Typical Application

The TPS65083x can be used in any system that needs multiple voltage rails. A DC supply voltage in between 5.4 V and 21 V is required. If the supply voltage is less than this range then a small boost can be added to supply the VIN and VINLDO3.

Along with the 5 DCDCs and 1 LDO, the TPS65083x has 8 general purpose comparators, 2 level shifters, board temperature monitoring system and 3 power path comparators. Latter 2 can be used as simple comparators if desired increasing the total comparators available for use to 12 on the TPS65083x.

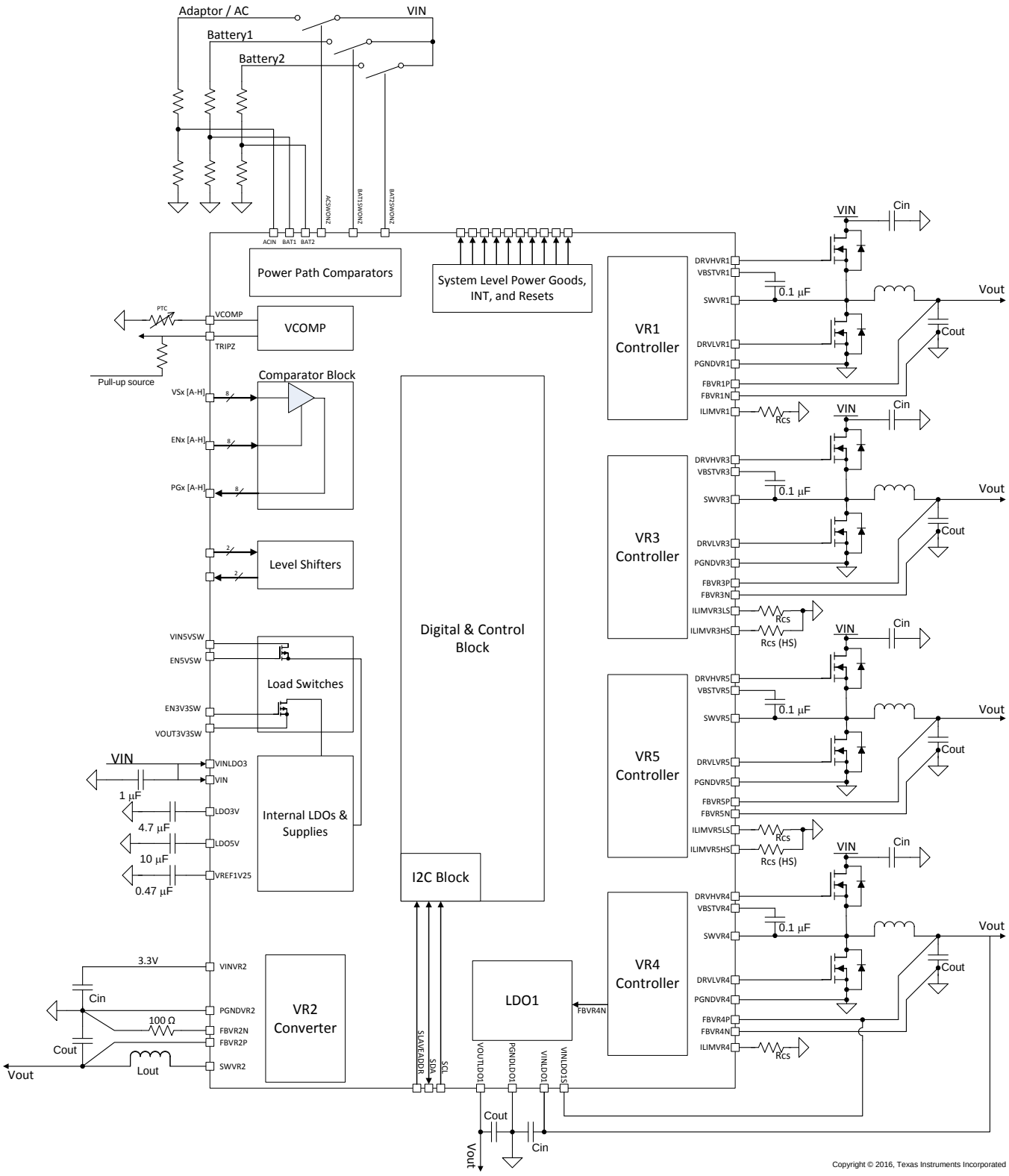


Figure 7-1. Simplifed General Block Diagram

7.2.1 Design Requirements

The TPS65083x requires decoupling caps on the supply pins. Refer to the Electrical Characteristics for recommended capacitance on these supplies.

The controllers, converter, LDO, and some other features can be adjusted to meet the application needs. The following describes how to design and adjust the external components to achieve desired performances.

7.2.2 Detailed Design Procedure

7.2.2.1 Controller Design Procedure

Designing the controller breaks down into several steps: designing the output filter, selecting the FETs, bootstrap capacitor, and input capacitors and setting the current limits.

Controllers VR1 and VR4 require VREG supply and capacitors. VREG should be connected to the 5-V LDO and a 1-µF, X5R, 20%, 10-V or similar capacitor should be used for decoupling.

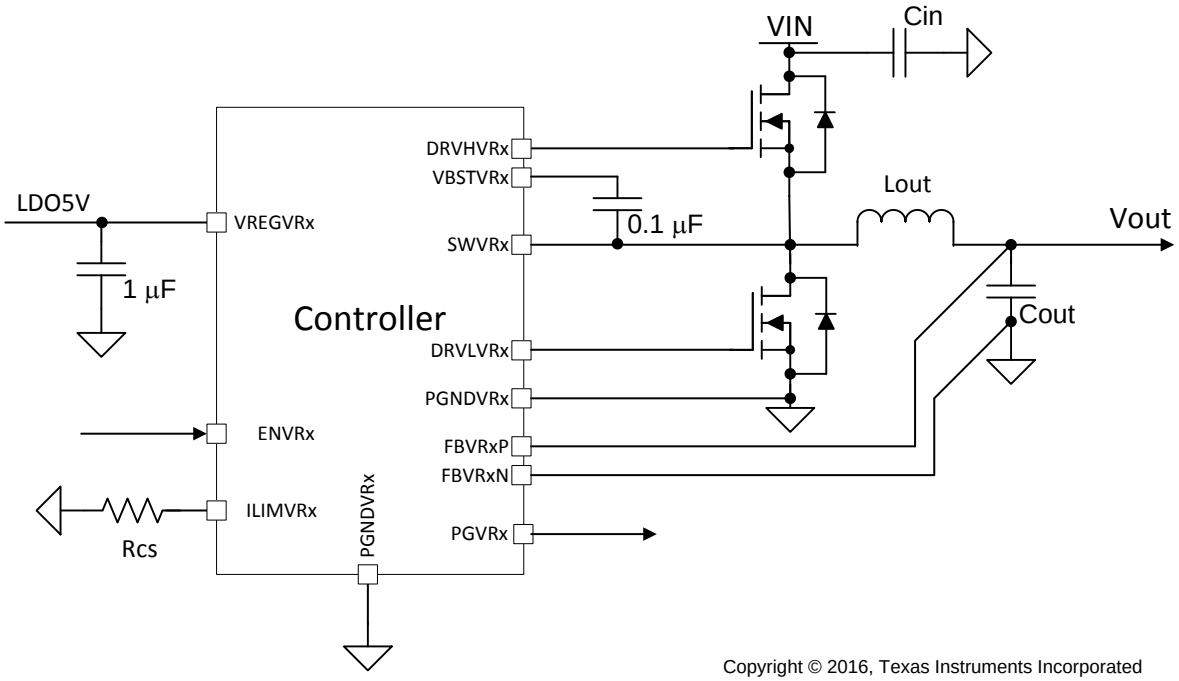


Figure 7-2. Controller Diagram

7.2.2.1.1 Selecting the Inductor

An inductor is required to be placed between the external FETs and the output capacitors. The inductor and output capacitors together make the double-pole which contributes towards stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. With an increase in inductance used the ripple current decreases which, typically increases efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected has to be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Use the equation below to calculate the recommended inductance for the controller. Let K_{IND} be the ratio of $I_{Lripple}$ to the $Iout_{MAX}$. It is recommended that K_{IND} is set to a value between 0.2 and 0.4.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \quad (1)$$

With the chosen inductance value, the peak current for the inductor in steady state operation, I_{Lmax}, can be calculated using the equation below. The rated saturation current of the inductor must be higher than the I_{Lmax} current.

$$I_{Lmax} = Iout_{max} + \left\{ \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right\} \quad (2)$$

Following these equations the preferred inductor selected for the controllers are listed below in Table 7-1.

Table 7-1. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIME031B	0.47 µH - 1 µH	3.3 mm x 3.7 mm	1.2 mm
Cyntec	PIMB041B	0.33 µH - 2.2 µH	4.45 mm x 4.75 mm	1.2 mm
Cyntec	PIMB051B	1 µH - 3.3 µH	5.4 mm x 5.75 mm	1.2 mm
Cyntec	PIME051E	0.33 µH - 4.7 µH	5.4 mm x 5.75 mm	1.5 mm
Cyntec	PIMB051H	0.47 µH - 4.7 µH	5.4 mm x 5.75 mm	1.8 mm
Cyntec	PIME061B	0.56 µH - 3.3 µH	6.8 mm x 7.3 mm	1.2 mm
Cyntec	PIME061E	0.33 µH - 4.7 µH	6.8 mm x 7.3 mm	1.5 mm
Cyntec	PIMB061H	0.1 µH - 4.7 µH	6.8 mm x 7.3 mm	1.8 mm

7.2.2.1.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitors of the DCDC controller the use of a small ceramic capacitors placed as close as possible to the inductor and the respective PGND pins of the IC is recommended. This solution typically, provides the smallest and lowest cost solution available for DCAP2 controllers.

7.2.2.1.3 Selecting the FETs

This controller is designed to drive NMOS FETs. Typically, the lower R_{DSon} for the high and low side FETs the better but, be sure to size the FETs, inductor and output capacitors appropriately as the R_{DSon} for the low side FET decreases, the minimum current limit increases. The Texas Instruments CSD87381P is recommended for the controllers.

7.2.2.1.4 Bootstrap Capacitor

To make sure that the internal high side gate drivers are supplied with a stable low noise supply voltage, a capacitor must be connected between the VBSTVRx pins and the respective SWVRx pins. Using ceramic capacitors with the value of 0.1 µF are recommended for the converters and the controllers, respectfully. For testing, a 0.1-µF, size 0402, 10-V capacitor was used for the controllers.

It is recommended to reserve a small resistor in series with the bootstrap capacitor in case the turn on / off of the FETs need to be slowed in order to reduce voltage ringing on the switch node. This is common practice for controller design.

7.2.2.1.5 Setting the Current Limits

The controller has a Valley Current Limit topology, also known as a Low Side Current Limit. This type of current limit works by limiting the current only when the low side FET is on. If the current being sourced by the low side FET is greater than the set low side current limit, I_{LS}, the controller will hold the low side FET on and the high side off until the current through the low side FET decreases below the set I_{LS}. Only if the current through the low side FET is less than the I_{LS} will the low side FET be allowed to turn off and the high side FET to turn on.

A fast current increase is limited by the maximum on time for the high side FET. This forces the low side FET to turn on every period. Once the low side FET turns on, the Low Side Current Limit can control the FETs until the current decreases below the I_{LS}. The maximum on time for the high side FET limits the current increase to maximum on time multiplied by the di/dt of the inductor until the low side FET is switched on.

I_{OCL} is the average current when the valley current is consistently the I_{LS}.

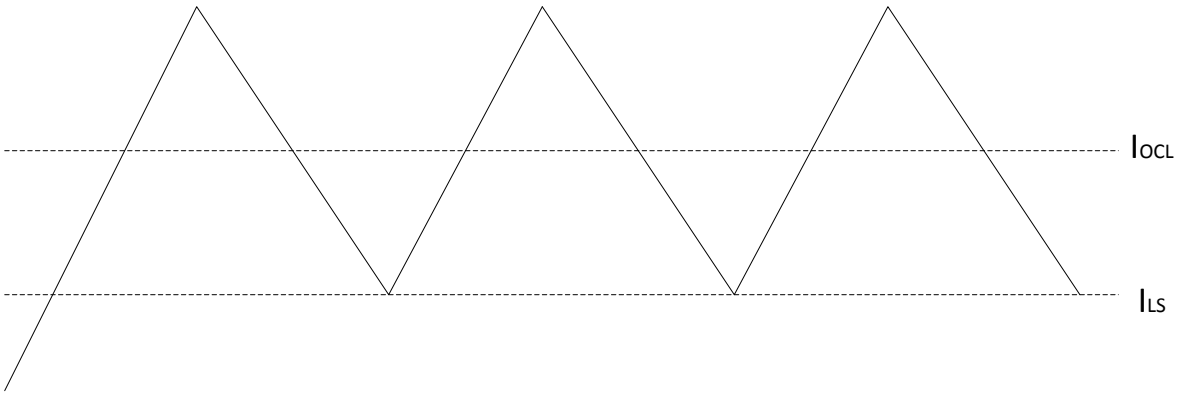


Figure 7-3. I_{OCL} Depiction

The low side current limit for the controllers is set by a resistor, R_{CS}, at the I_{LIMx} pin. A current, I_{TRIP}, is sourced across the R_{CS} to set the voltage for the current limit comparator. Use the equation below to determine the R_{CS} resistor. It is recommended to set I_{OCL} to 130% of I_{OUTmax} and use a resistor with ±1% or less tolerance for best results. Since the current limit is when the inductor current is near its maximum it is recommended to use the saturation derating of the inductor when calculating the R_{CS}.

$$R_{CS} = \frac{8 \times R_{DSon} \times 1.3 \times \left(I_{OCL} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \right)}{I_{TRIP}} \quad (3)$$

There is a minimum and a maximum I_{OCL} that can be achieved for the given parameters used in the equation above. To ensure that the R_{CS} has been sized correctly, the following equation must be true across the application temperature range.

$$V_{CSmin} < I_{TRIP} \times R_{CS} < V_{CSmax} \quad (4)$$

If the controller has high side current limit then, use Equation 5 to calculate the high side R_{CS} resistor. The high side current limit must be set higher than the low side current limit. Again, since the current limit is when the inductor current is near its maximum it is recommended to use the saturation derating of the inductor when calculating the R_{CS}.

$$R_{CS\,(HS)} = \frac{\left(\frac{\left(R_{DSon} \times \left(I_{OCL} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}\right)\right)}{3200\Omega} - 8\mu A\right) \times 20k\Omega}{I_{TRIP}} \quad (5)$$

7.2.2.1.6 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For the controller, 12 µF of input capacitance is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. A ceramic capacitor placed as close as possible to the respective VINx and PGNDx pins of the FETs is recommended.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, ±20% or similar.

7.2.2.2 Converter Design Procedure

Designing the converter has only 2 steps: designing the output filter and selecting the input capacitors. The converter must be supplied by a 3.3-V source which can be provided by one of the TPS65083x controllers.

The converter requires VREG supply and capacitors. VREG should be connected to the 5-V LDO and a 1-µF, X5R, 20%, 10-V or similar capacitor should be used for decoupling.

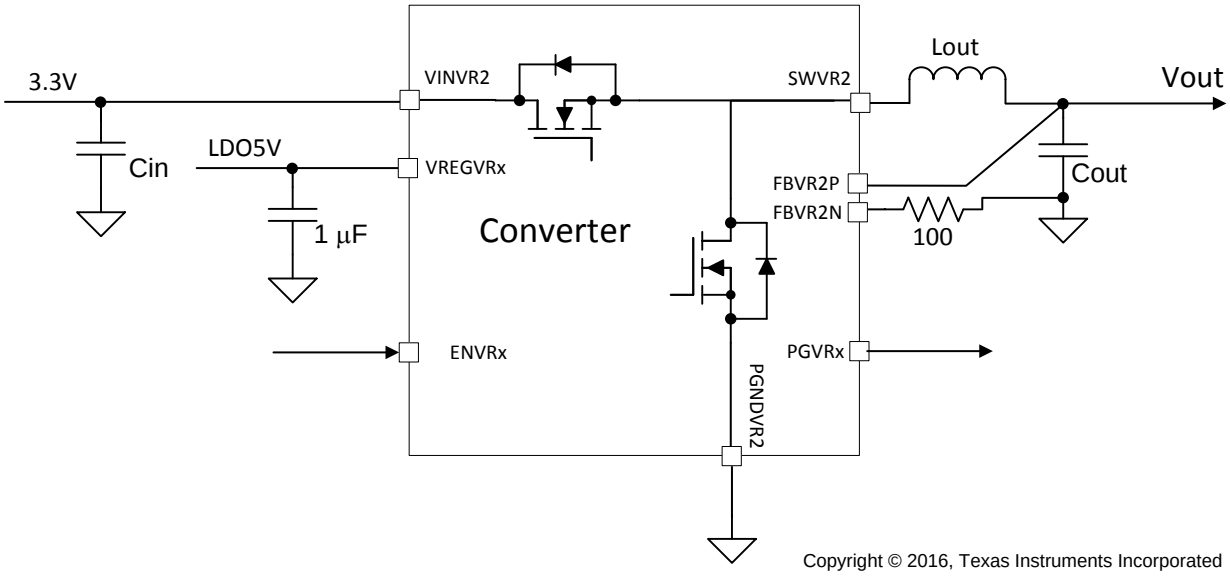


Figure 7-4. Converter Diagram

7.2.2.2.1 Selecting the Inductor

An inductor is required to be placed between the SWVRx and the output capacitors. The inductor and output capacitors together make the double-pole which contributes towards stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. With an increase in inductance used the ripple current decreases which, typically increases efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected has to be rated for appropriate saturation current, core losses and DC resistance (DCR).

Use the equation below to calculate the recommended inductance for the controller. Let K_{IND} be the ratio of $I_{Lripple}$ to the $Iout_{MAX}$. It is recommended that K_{IND} is set to a value between 0.2 and 0.4.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times Iout_{MAX} \times K_{IND}} \quad (6)$$

With the chosen inductance value, the peak current for the inductor in steady state operation, I_{Lmax}, can be calculated using the equation below. The rated saturation current of the inductor must be higher than the I_{Lmax} current.

$$I_{Lmax} = Iout_{max} + \left\{ \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L} \right\} \quad (7)$$

Following these equations the preferred inductors selected for the converter are listed below in Table 7-2.

Table 7-2. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIFE32251B-R68MS	0.68 µH	3.2 mm x 2.5 mm	1.2 mm
Würth	744383230068	0.68 µH	2.5 mm x 2 mm	1.0 mm

7.2.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitors of the DCDC converters the use of a small ceramic capacitors placed as close as possible to the inductor and the respective PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the inductor and the respective PGND pins of the IC.

At the DCDC converters the recommended capacitor for use is the muRata GRM188R60J226MEAO: 22 µF, 0603, 6.3 V, ±20% or similar. This capacitor was selected to achieve the highest derated capacitance in a small 0603 package. If the selected output voltage is greater than 3.3 V then the muRata GRM21BR61A226ME44: 22 µF, 0805, 10 V, ±20%, or similar is recommended for use. This capacitor is recommended to maintain the actual capacitance as DC bias increases.

7.2.2.2.3 Selecting the Input Capacitors

Because of the nature of the switching converter and controller with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For the controller, 12 µF of input capacitance is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. A ceramic capacitor placed as close as possible to the respective VINx and PGNDx pins of the IC is recommended.

The preferred capacitors for the controllers are two muRata GRM21BR61E106MA73: 10 µF, 0805, 25 V, ±20% or similar.

7.2.2.3 LDO Design Procedure

The LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is important to maintain a high amount of capacitance with low ESR on the LDO outputs and inputs. Ceramic capacitors are ideal for this. Below is the recommended capacitors.

The preferred output capacitor for the LDO is muRata GRM188R60J476M: 47 µF, 0603, 6.3 V, ±20% or similar.

The preferred input capacitor for the LDO is muRata GRM155R60J106ME44: 10 µF, 0402, 6.3 V, ±20% or similar.

7.2.2.4 Board Temperature Monitoring Design Procedure

Board temperature monitoring requires only 1 thermistor if only 1 sense point is desired. It can be scaled by adding as many thermistors as sense points desired. Simply connect a PTC thermistor that has an exponential coefficient curve from the VCOMP pin to GND and a pull up to desired voltage source on the TRIPZ pin. Place thermistor where desired. If multiple sense points are desired string the thermistors together in a series connection while placing the thermistors where desired.

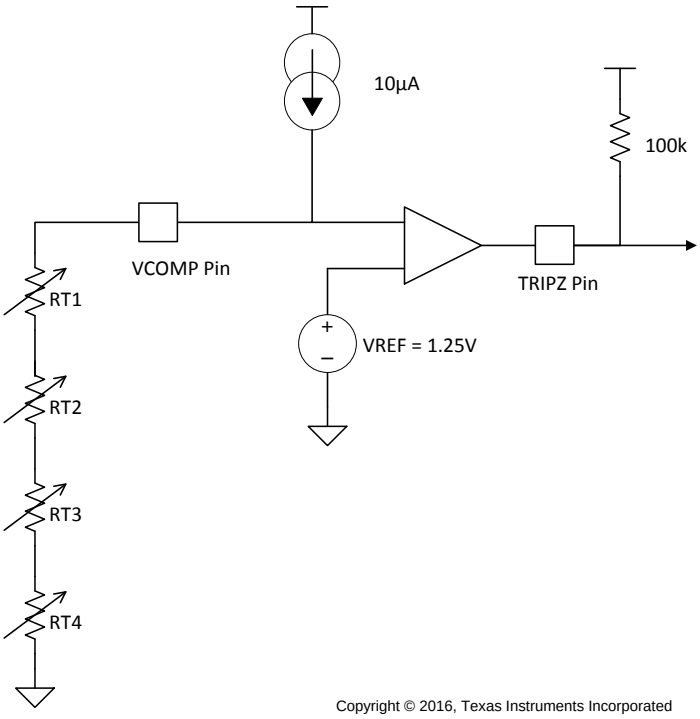


Figure 7-5. Board Temperature Monitoring Circuit Example

The thermistors should have low room and mid temperature resistances in the range of 1 kΩ to 10 kΩ. The hot point resistance should be roughly 10x mid temperature resistance in the range of 100 kΩ to 200 kΩ. There is an internal 10-µA current source that provides a voltage across the thermistors. Once this voltage exceeds the comparator threshold of 1.25 V the TRIPZ pin switches to LOW indicating a HOT board temperature. Therefore, the resistance required for HOT board temperature is 125 kΩ. Select thermistors that align this resistance with the desired HOT temperature setpoint.

The recommended thermistors for this feature is the muRata PRF15BG102RB6RC.

7.2.2.5 Power Path Design Procedure

The TPS65083x has power path comparators and outputs to control the power path switches. Simply connect a voltage divider to the adaptor and batteries to set the threshold to the desired value. The outputs of the comparators require a pull up since they are open-drain outputs. In-order for the power path comparators to work without VIN supplied connect the VINPP to the power rails that are being monitored by using a diode to select the highest voltage among the sources.

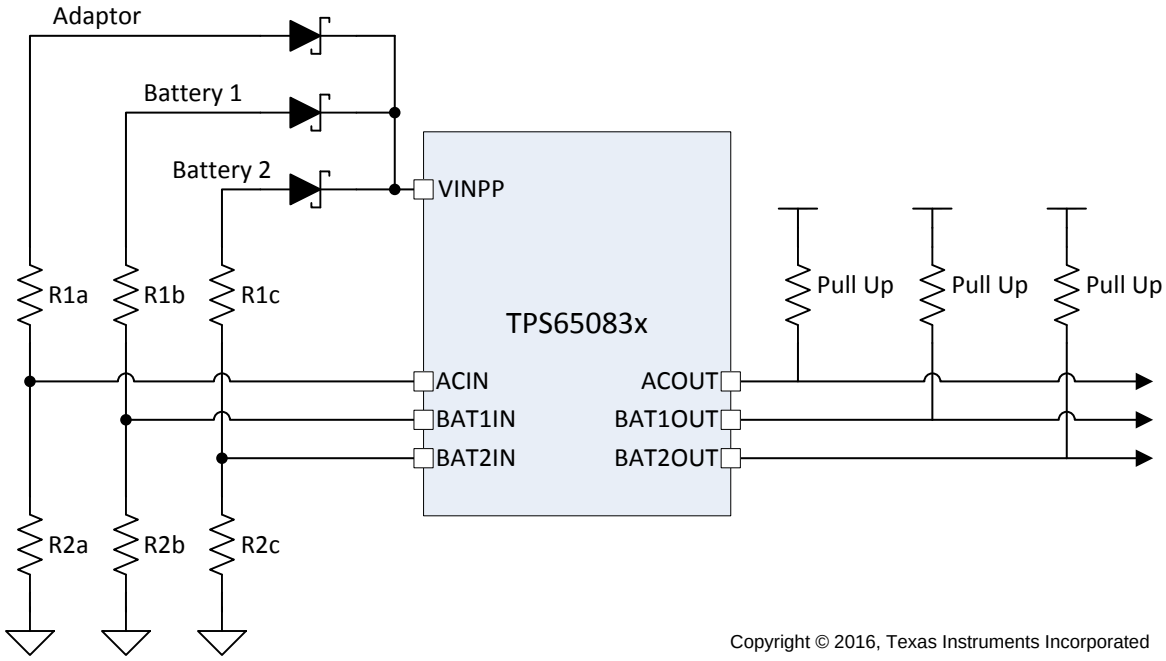


Figure 7-6. Power Path Comparators and VINPP Supply

Example:

Desired is to measure a battery and an adaptor to decide when to switch over from battery to adaptor. The voltages desired for thresholds are 9 V and 6 V respectively. Using Equation 8 the resistors required to set the 9-V threshold are R1a = and R2a = . The resistors required to set the 6-V threshold are R1b = and R2b = .

$$R_1 = R_2 \times \left(\frac{V_{IN}}{V_{Threshold}} - 1\right) \quad (8)$$

7.2.3 Application Performance Curves

Table 7-3. Application Curves Overview

TYPE	DESCRIPTION AND ASSUMPTIONS	FIGURE NUMBER
Efficiency VR1	Using CSD87381P FET Block, PIME051H-1R0MS, 3 x GRM31CR60G227ME11 + 1 x GRM21BR60J107M, NDVCZ = HIGH, **Vout = 1 V**	Figure 7-7
Efficiency VR2	Using PIFE32251B-R68MS, 4 x ZRB18AR60G476ME01, NDVCZ = HIGH, **Vout = 1.8 V**	Figure 7-8
Efficiency VR3	Using CSD87381P FET Block, PIMB061H-1R5MS, 3 x GRM21BR60J107M , NDVCZ = HIGH, **Vout = 3.3 V**	Figure 7-9
Efficiency VR4	Using CSD87381P FET Block, PIME051H-1R0MS, 2 x GRM31CR60G227ME11 + 1 x GRM21BR60J107M, NDVCZ = HIGH, **Vout = 1.2 V**	Figure 7-10
Efficiency VR5	Using CSD87381P FET Block, PIMB051H-3R3MS, 11 x GRM21BR61A476ME15, NDVCZ = HIGH, **Vout = 5 V**	Figure 7-11

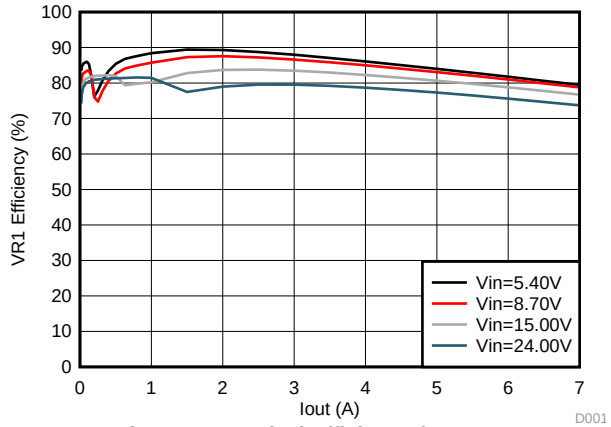


Figure 7-7. Typical Efficiency for VR1

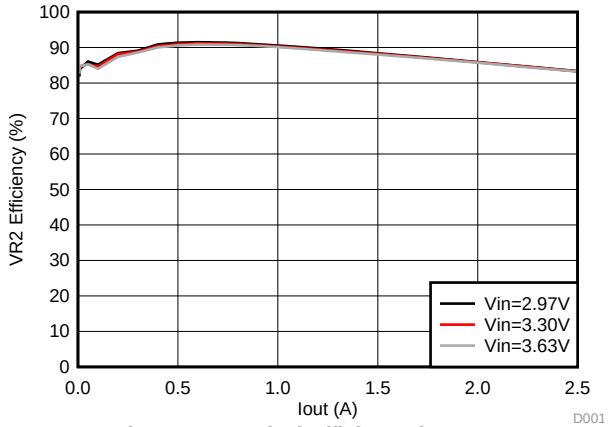


Figure 7-8. Typical Efficiency for VR2

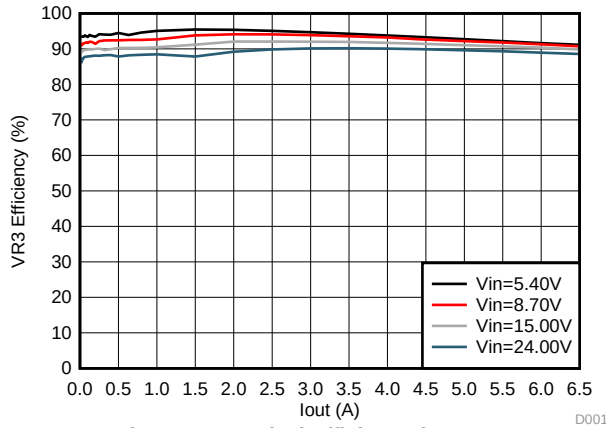


Figure 7-9. Typical Efficiency for VR3

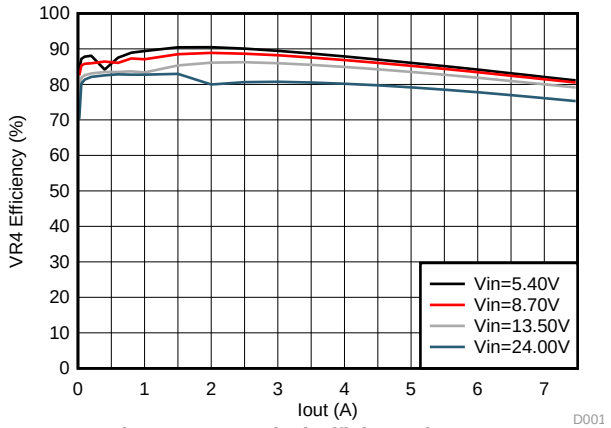


Figure 7-10. Typical Efficiency for VR4

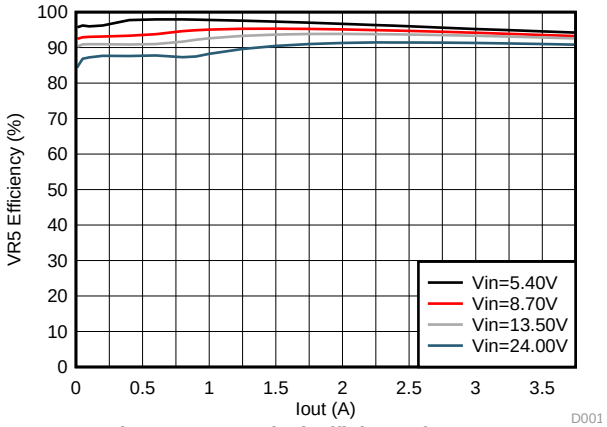


Figure 7-11. Typical Efficiency for VR5

7.2.4 Specific Application - TPS650830 Powering the Intel SkyLake and Kabylake Platform Volume Configuration

Volume configuration is the lowest cost and smallest solution for SkyLake and Kabylake power. It combines multiple same voltage rails into one rail reducing cost and size. Load switches are utilized to separate the rails and power the system with correct sequencing. The PMIC controls these load switches with the power good comparators. The TPS65083x also supports Premium configurations, see TPS650831 and TPS650832 or literature numbers: SLVSCS5 and SLVSCS6.

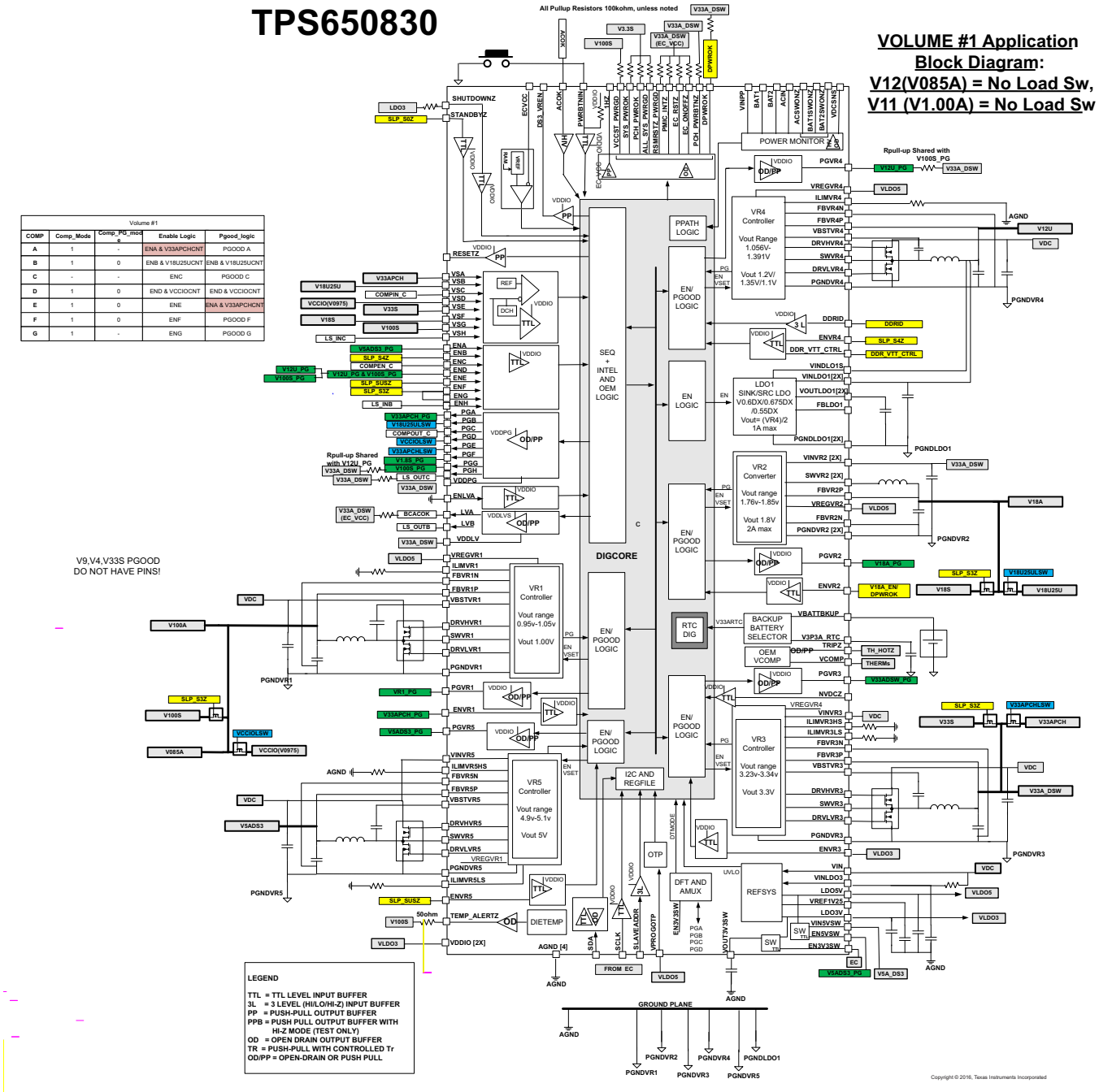


Figure 7-12. TPS650830 Volume Application Diagram

7.2.4.1 Design Requirements

The deisgn requirements are set by the Intel SkyLake and Kabylake Platform. Below are the requirements of the power supply system. This procedure assumes the system is a 2S NVDC system but, the TPS65083x supports 3S NVDC, as well as non-NVDC systems. 2S NVDC system has an input voltage range of 5.4 V to 8.7 V.

- There must be 9 separate voltage rails:
  - V5A_DS3 - 5 V, I_{MAX} = 3.5 A
  - V3.3A_DSW - 3.3 V, I_{MAX} = 3.5 A
  - V3.3A_PCH - 3.3 V, I_{MAX} = 3 A
  - V1.00A - 1.0 V, I_{MAX} = 4.9 A
  - VCCIO - 1.0 V, I_{MAX} = 2.9 A
  - V1.8A - 1.8 V, I_{MAX} = 1 A
  - V1.8U - 1.8 V, I_{MAX} = 1 A
  - VDDQ - 1.2 V, I_{MAX} = 7.5 A
  - VTT - 0.6 V, I_{MAX} = ±1A
- All rails must have maximum tolerance of ±5% of the nominal voltage at all times with load transients.
  - Load Transients are defined as 0% to 70%, 70% to 0%, 30% to 100% and 100% to 30% load current steps relative of the I_{MAX} current defined for each rail.
- Maximum height of components = 1.8 mm.
- Sequence in the order below:
  - V3.3A_DSW with VIN supplied
  - V1.8A with VIN supplied
  - V5A_DS3 with SLP_SUS# transition to HIGH
  - V3.3A_PCH with SLP_SUS# transition to HIGH
  - V1.00A with SLP_SUS# transition to HIGH
  - VDDQ with SLP_S4# transition to HIGH
  - V1.8U with SLP_S4# transition to HIGH
  - VCCIO with SLP_S3# transition to HIGH
  - VTT with DDR_VTT_CTRL / SLP_S0# transition to HIGH

7.2.4.2 Detailed Design Procedure

The TPS650830 supplies 6 voltage rails and controls 3 load switches to meet the sequence order for the V3.3A_PCH, V1.8U, and VCCIO rails.

- VR1 supplies the V1.00A rail and the VCCIO rail with a load switch.
- VR2 supplies the V1.8A rail and the V1.8U rail with a load switch.
- VR3 supplies the V3.3A_DSW rail and the V3.3A_PCH rail with a load switch.
- VR4 supplies the VDDQ rail and the VINLDO1 for termination.
- VR5 supplies the V5A_DS3 rail.
- VLDO1 supplies the VTT rail.

To meet the sequencing requirement the power goods of the VRs and PG comparators are feed back into the enables for the VRs and comparators. The 5 external control signals SLP_SUS#, _S4#, _S3#, _S0#, and DDR_VTT_CTRL are responsible for transitioning the system from sleep state to sleep state and the reverse sequencing.

Since, the requirements are for a 2S NVDC system the NVDCZ pin should be tied LOW.

7.2.4.2.1 Output Inductance and Capacitance

Following the recommend design procedure in Section 7.2.2 will yield output inductance and capacitance similar to Table 7-4.

Table 7-4. SkyLake and Kabylake Volume Configuration Output L and C

VRx	OUTPUT INDUCTANCE	MINIMUM OUTPUT CAPACITANCE	RECOMMENDED OUTPUT CAPACITORS	CAPACITOR MANUFACTURER
VR1	0.56 µH	160 µF	1 x GRM31CR60G227ME11 and 1 x ZRB18AR60G476ME01	muRata
VR2	0.68 µH	47 µF	4 x ZRB18AR60G476ME01	muRata
VR3	1 µH	87 µF	2 x GRM31CR60G227ME11	muRata
VR4	0.56 µH	117 µF	1 x GRM31CR60G227ME11	muRata
VR5	2.2 µH	76 µF	8 x GRM21BR61A476ME15	muRata

7.2.4.3 Application Performance Curves

Table 7-5. Application Curves Overview

TYPE	DESCRIPTION AND ASSUMPTIONS	FIGURE NUMBER
Efficiency VR1	Using CSD87381P FET Block, PIMB051H-0R56M, 1 x GRM31CR60G227ME11 + 1 x ZRB18AR60G476ME01, NDVCZ = LOW, **Vout = 1 V**	Figure 7-13
Efficiency VR2	Using PIFE32251B-R68MS, 4 x ZRB18AR60G476ME01, NDVCZ = LOW, **Vout = 1.8 V**	Figure 7-14
Efficiency VR3	Using CSD87381P FET Block, PIME051H-1R0MS, 2 x GRM31CR60G227ME11, NDVCZ = LOW, **Vout = 3.3 V**	Figure 7-15
Efficiency VR4	Using CSD87381P FET Block, PIMB051H-0R56M, 1 x GRM31CR60G227ME11, NDVCZ = LOW, **Vout = 1.2 V**	Figure 7-16
Efficiency VR5	Using CSD87381P FET Block, PIME051B-2R2MS, 8 x GRM21BR61A476ME15, NDVCZ = LOW, **Vout = 5 V**	Figure 7-17

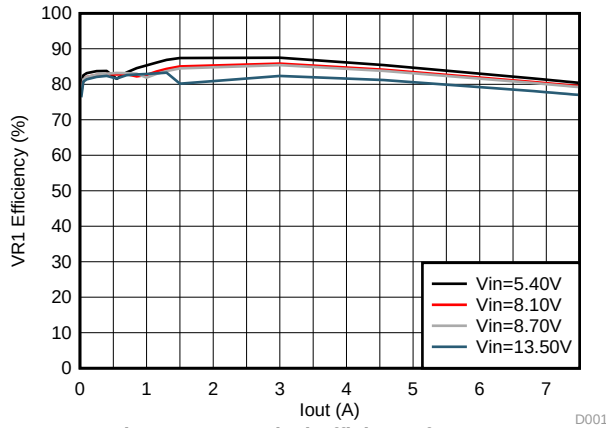


Figure 7-13. Typical Efficiency for VR1

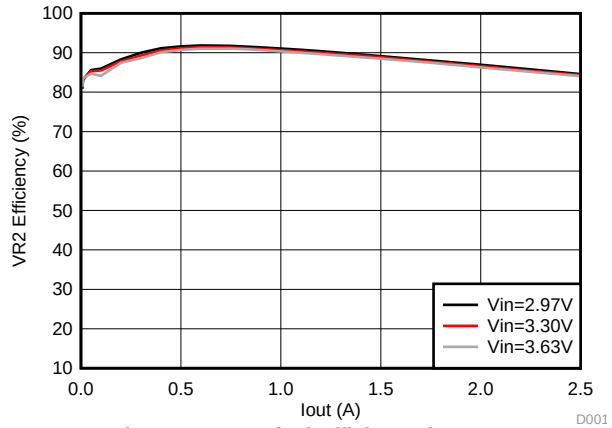


Figure 7-14. Typical Efficiency for VR2

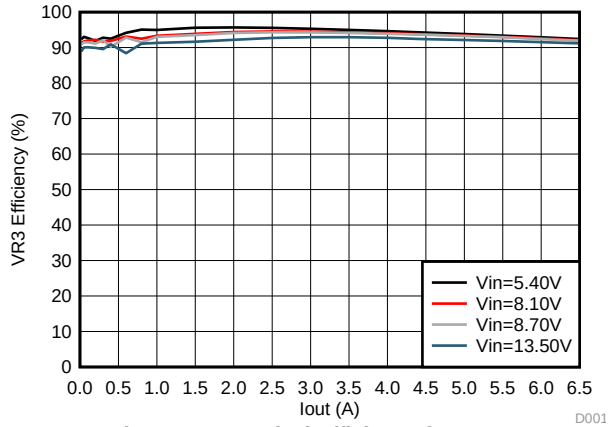


Figure 7-15. Typical Efficiency for VR3

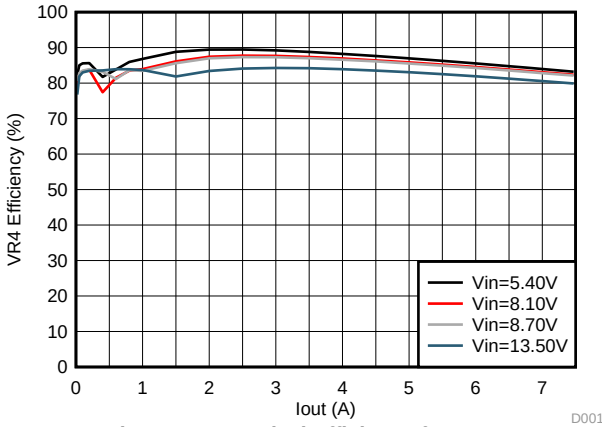


Figure 7-16. Typical Efficiency for VR4

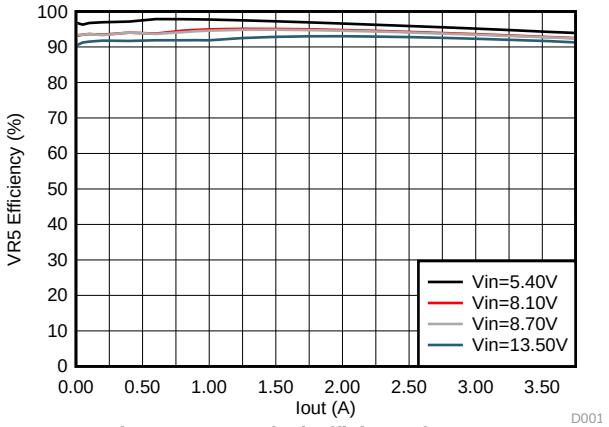


Figure 7-17. Typical Efficiency for VR5

7.3 System Example

Below is a diagram of the SkyLake and Kabylake Platform System Power Delivery. The PMIC is flexible and adjusts well across SkyLake and Kabylake platforms.

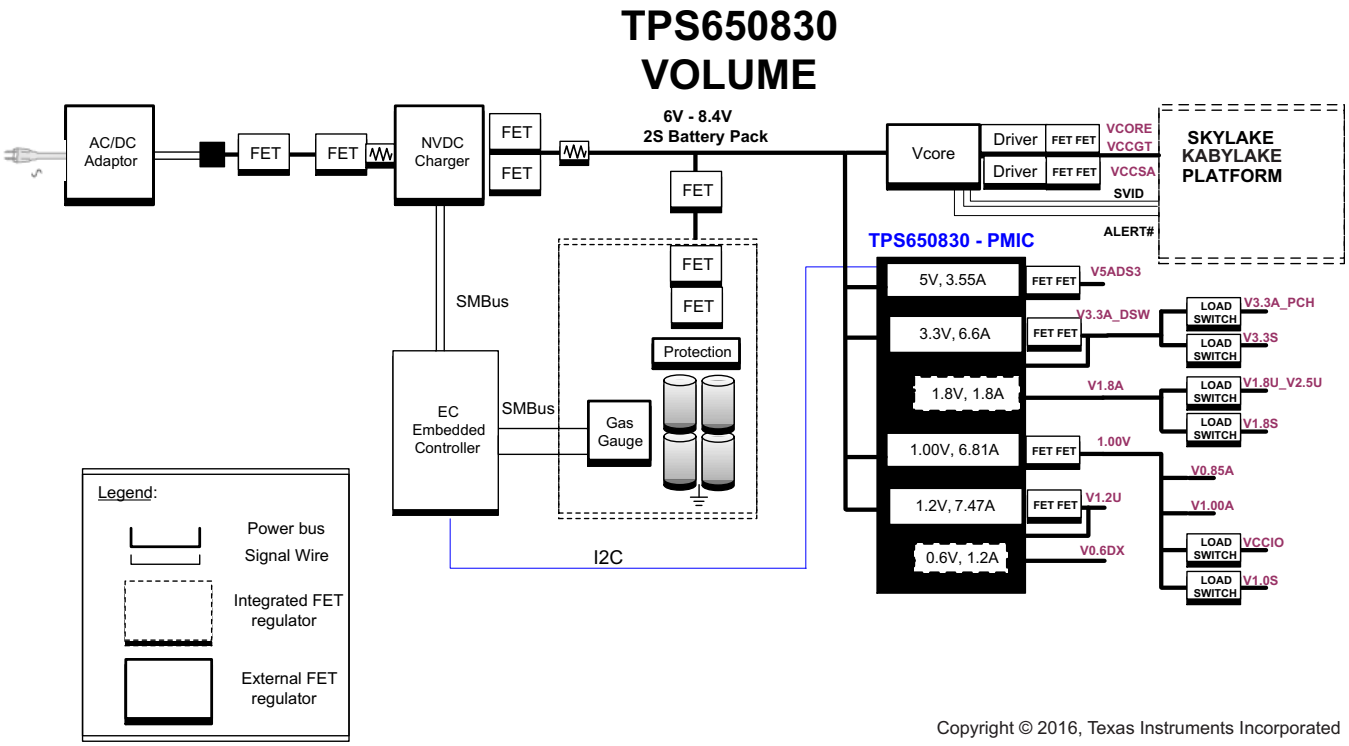


Figure 7-18. TPS650830 Volume Simplified System Power Configuration Diagram

7.4 Do's and Don'ts

- Always either float or connect the VINPP to the same voltage as VIN. Never ground VINPP.
- If not using a voltage regulator connect the enable to ground and float the output.

8 Power Supply Recommendations

Any power supply capable of delivering the required input power is acceptable provided that there is a source within the recommended operating conditions for VIN and VINLDO3. The input voltage for the VR2 converter must be 3.3 V always. The input voltage of the controllers may vary from the VIN and VINLDO3 voltage. Ensure that VINPP is connected to the VIN or floated but not grounded.

9 Layout

9.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

There are 2 packages available for the TPS65083x, the ZAJ and ZCG. The ZAJ is a 7-mm x 7-mm BGA with 0.5-mm ball pitch. The ZCG is a 9-mm x 9-mm BGA with 0.5-mm ball pitch but, some of the inner balls have been removed for easier routing. Both packages preform relatively the same and the decision between which package is best for the application depends on the space constraints and routing technology used.

9.1.1 Fanout for ZAJ using Type 4 Routing

This small 7-mm x 7-mm package utilizes the Type 4 routing technique to decrease system board area as much as possible. This Type 4 routing has vias in pad, blind and buried vias, and minimum trace width / spacing of 4 mils.

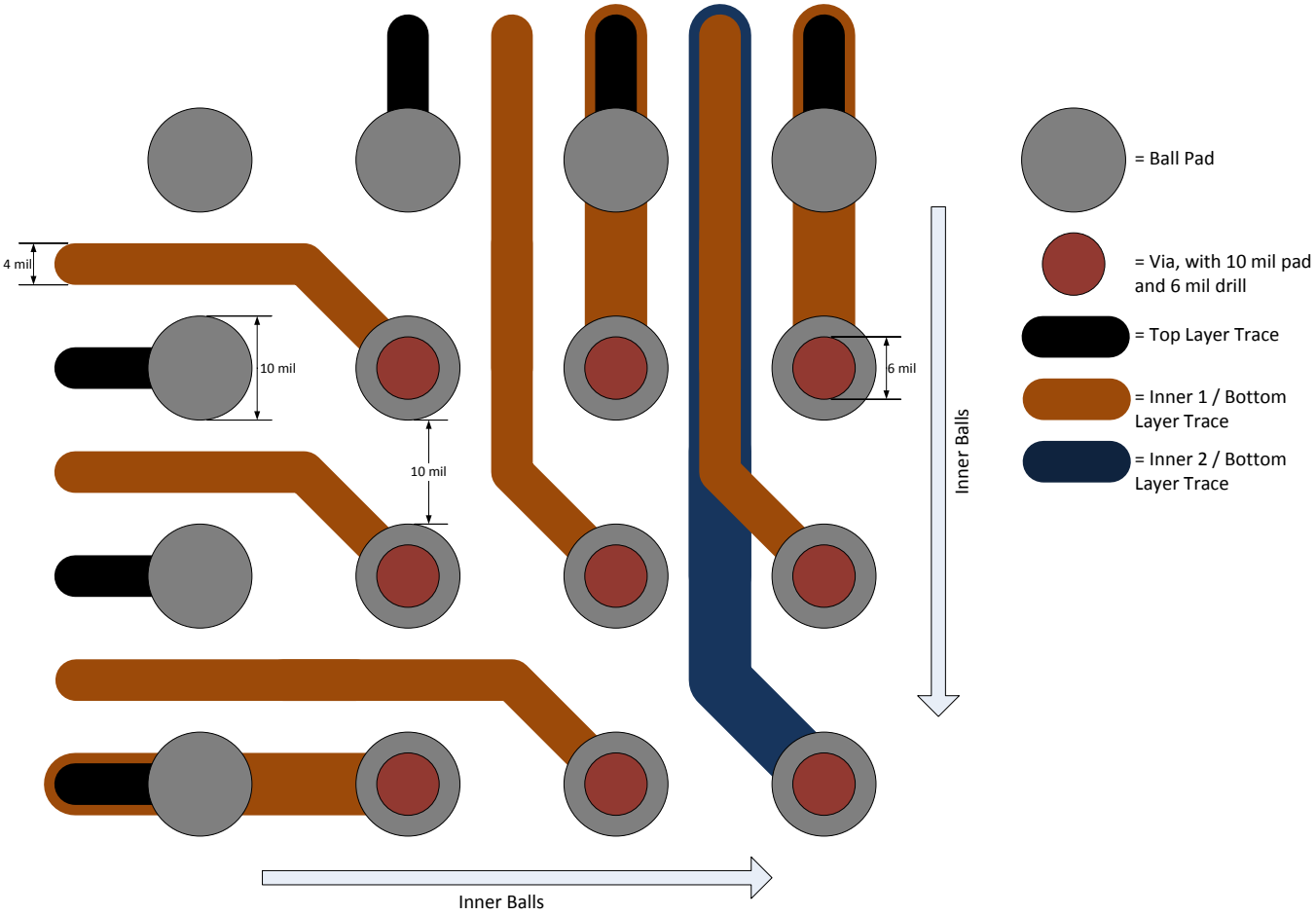


Figure 9-1. Fanout for ZAJ Package Using Type 4 Routing

9.1.2 Fanout for ZCG using Type 3 Routing

The ZCG has some of the inner balls removed to essentially create a 0.1-mm ball pitch for the inner balls of the package. This feature allows for Type 3 routing of the board. This Type 3 routing has no vias in pad, no blind and buried vias, and minimum trace width / spacing of 4 mils.

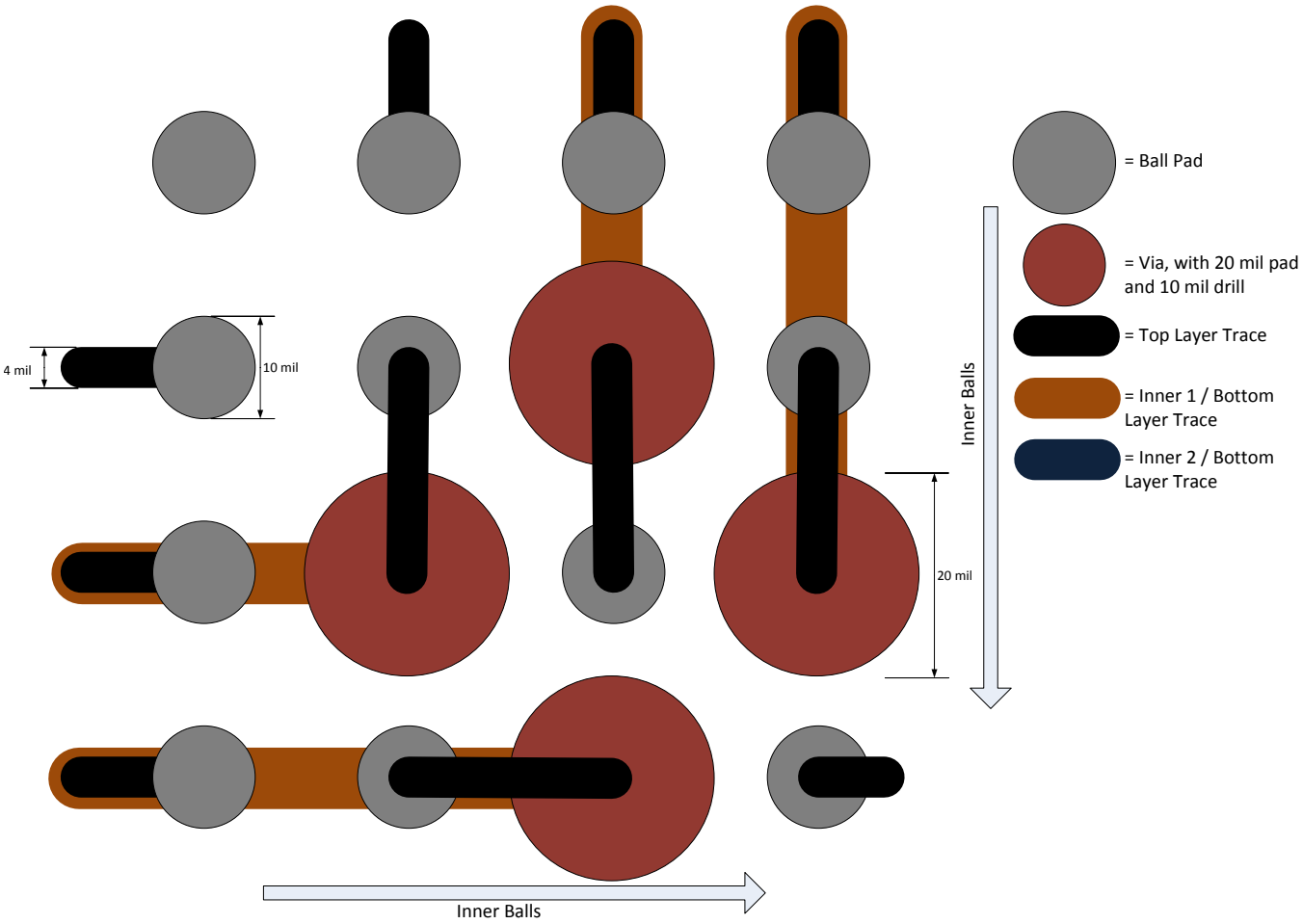


Figure 9-2. Fanout for ZCG Package using Type 3 Routing

9.1.3 Layout Checklist

- All inductors, input/output caps and FETs for the converters and controller should be on the same board layer as the IC.
- Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.
- Bootstrap capacitors must be place close to the IC from the SWVRx to VBSTVRx pins.
- DRVLVRx signals must be routed on the same layer as the IC and the FETs and minimize the length and parasitic inductance of the trace as much as possible.
- Each converter and controller should have their own separate ground and each ground should connect to the common ground separately. The input capacitors, output capacitors, and FET grounds for each VRx converter and controller must be connected to the ground plane for the respective VRx rail. Since, the PGNDs for each rail are not connect to each other or AGND, it is required to use the PGNDVRx pins for the input and output capacitors for each VRx rail. This ground plane should connect in one place to the common ground close to the input and output capacitor ground pads. See the figure below for a visual representation of the converter layout scheme.
- The internal reference regulators must have their input and output caps close to the IC pins.
- Route the FBVRxP and FBVRxN signals as a differential pair.

9.2 Layout Example

9.2.1 Controller Layout

The routing of the controllers is critical to the performance of the power supply. To reduce the risk of the controller effecting other sensitive circuits on the board, it is recommended to place all of the controller components on the same layer are the PMIC. In addition to component placement, the DRV, SW, and PGND signals should be routed on the same layer or as few of layers possible. It is recommended to place the FETs as close as possible to the PMIC but, it is imperative that the input capacitors are placed with minimal distance from the VIN and PGND pads of the FETs. The feedback signals should be routed differentially to the furthest output capacitor, which should be placed close to the load. Be sure to not route the feedback or any analog sensitive signals under the inductor, next to the SW node, or between the CIN and the FETs due to the high frequency switching from the edges.

If the FETs of the controller are to be place far away from the PMIC the layout of the DRV, SW and PGND signals becomes extremely critical. The loop inductance of the the traces must be minimized as much as possible. In-order to do this, pair the DRVH and SW traces together and pair the DRVL and PGND traces together. PGND is best routed as a plane. To reduce the loop inductance of the DRVL, DRVL trace should be routed one layer above the PGND. Generally, the SW, DRVL and DRVH traces should be 20 mils or larger assuming the PGND is a plane underneath the DRVL trace.

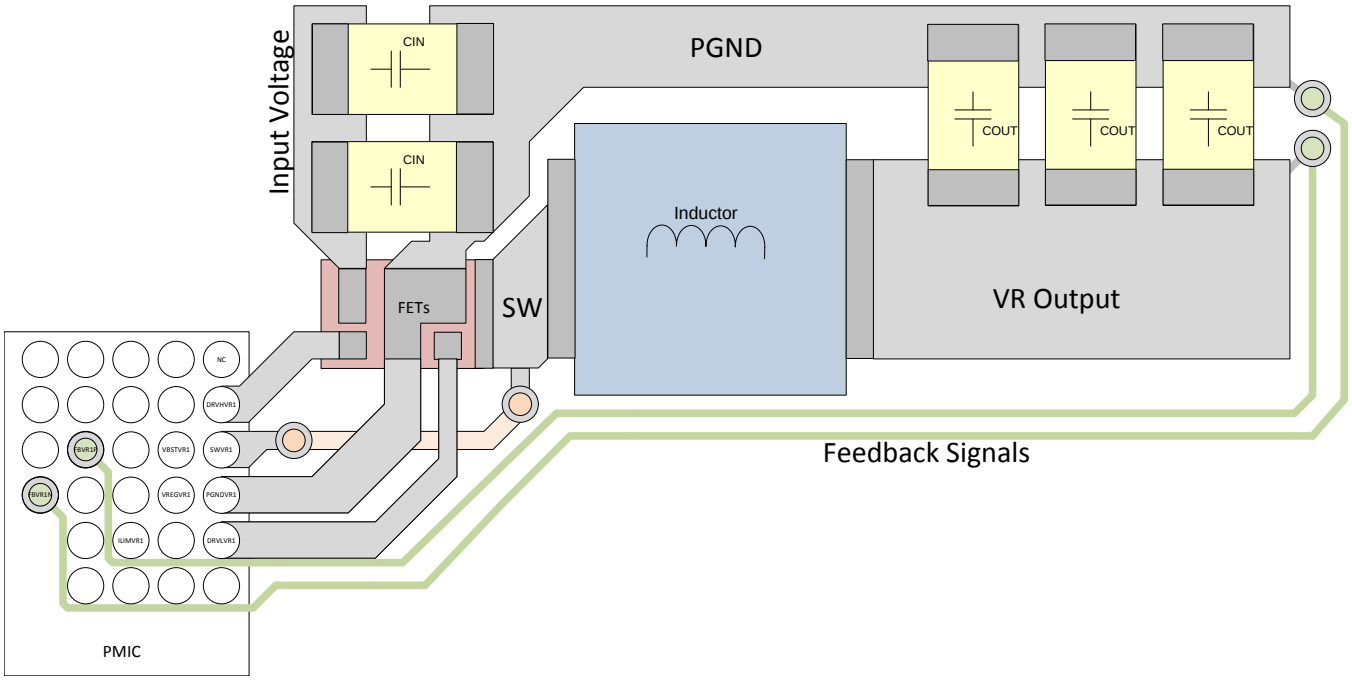


Figure 9-3. Controller Layout Diagram

9.2.2 ZAJ Package

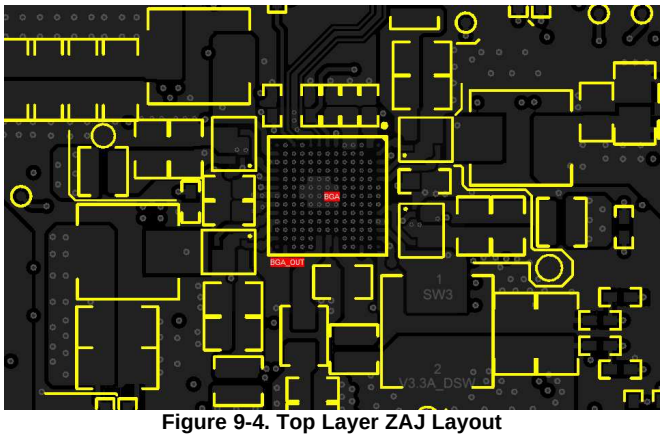


Figure 9-4. Top Layer ZAJ Layout

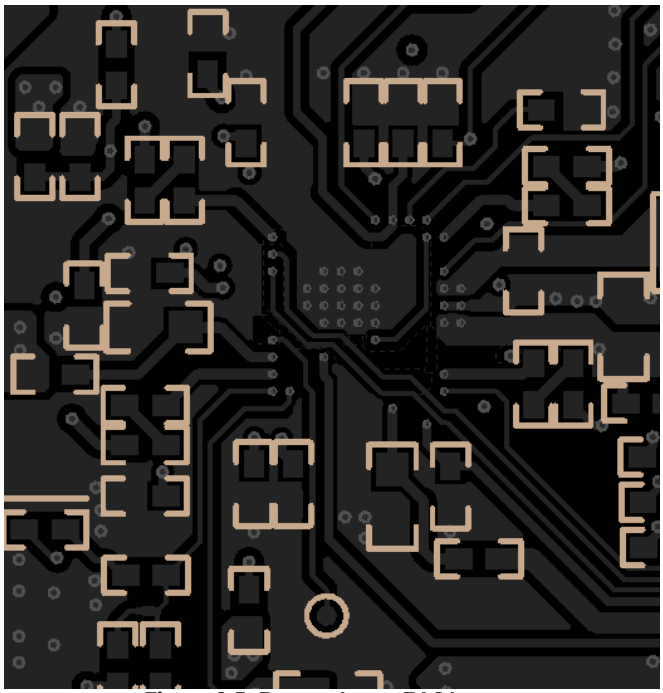


Figure 9-5. Bottom Layer ZAJ Layout

9.2.3 ZCG Package

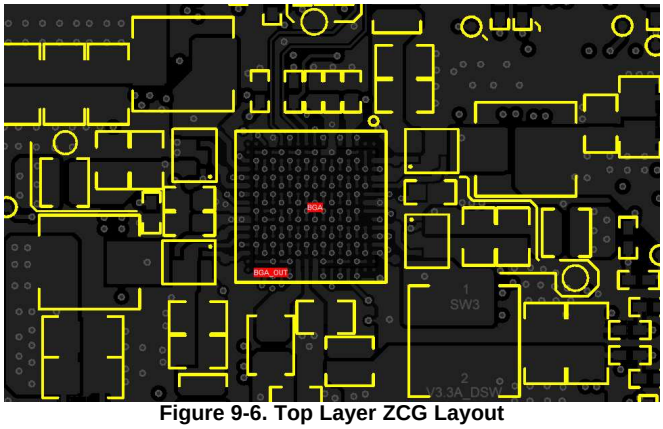


Figure 9-6. Top Layer ZCG Layout

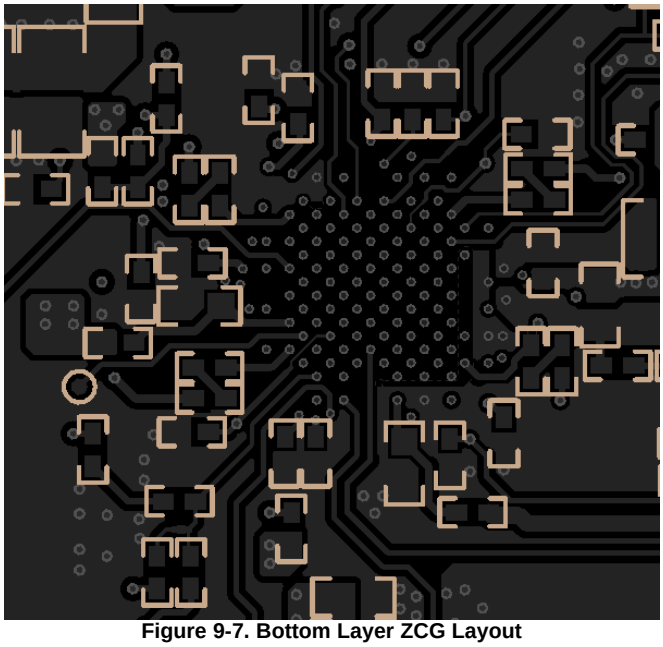


Figure 9-7. Bottom Layer ZCG Layout

9.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

10 Device and Documentation Support

10.1 Device Support

For device support, please submit questions to the E2E forum here:e2e.ti.com

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.1.2 Development Support

For frequently asked questions, FAQs, on the TPS65083x, please refer to the FAQ here: http://e2e.ti.com/support/power_management/pmu/w/design_notes/2898.tps65083x-faqs

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report* SZZA017
- *Semiconductor and IC Package Thermal Metrics Application Report* SPRA953

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support.*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS650830ZAJR	Active	Production	NFBGA (ZAJ) | 168	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJR.A	Active	Production	NFBGA (ZAJ) | 168	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJT	Active	Production	NFBGA (ZAJ) | 168	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZAJT.A	Active	Production	NFBGA (ZAJ) | 168	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGR	Active	Production	NFBGA (ZCG) | 159	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGR.A	Active	Production	NFBGA (ZCG) | 159	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGT	Active	Production	NFBGA (ZCG) | 159	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830
TPS650830ZCGT.A	Active	Production	NFBGA (ZCG) | 159	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS650830

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

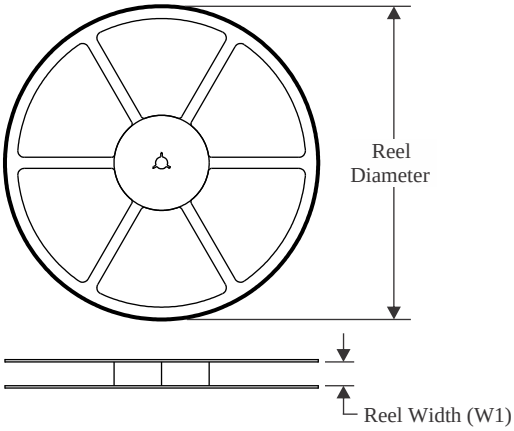
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

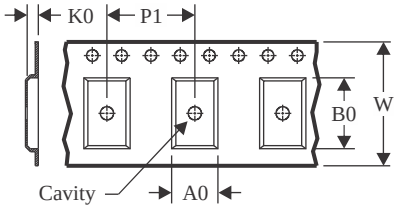
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

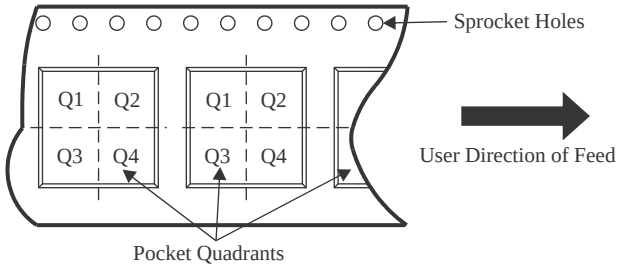


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

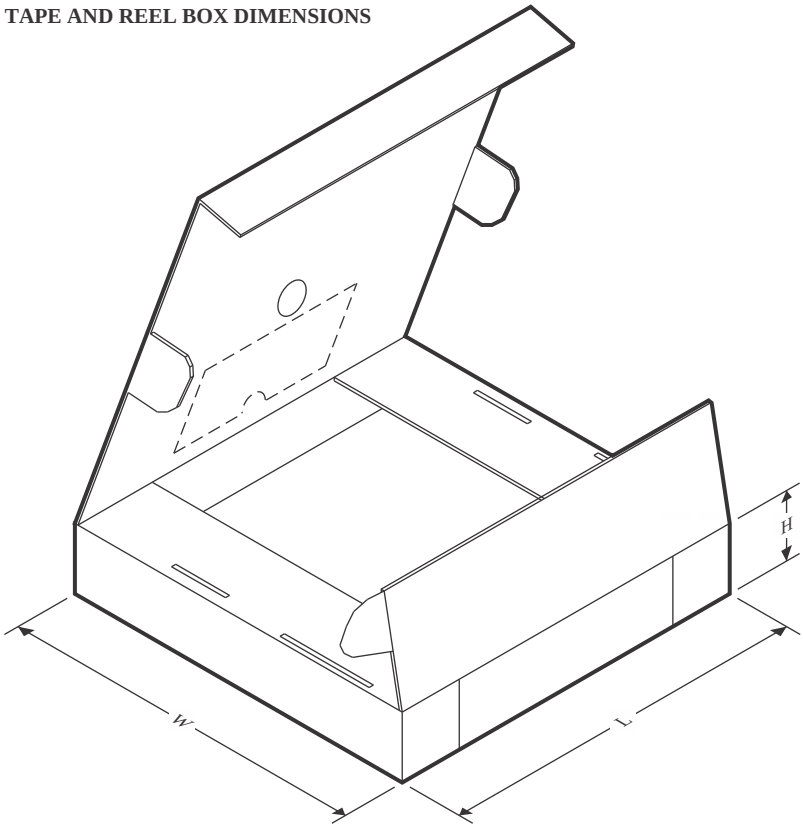
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650830ZAJR	NFBGA	ZAJ	168	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TPS650830ZAJT	NFBGA	ZAJ	168	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TPS650830ZCGR	NFBGA	ZCG	159	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
TPS650830ZCGT	NFBGA	ZCG	159	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1

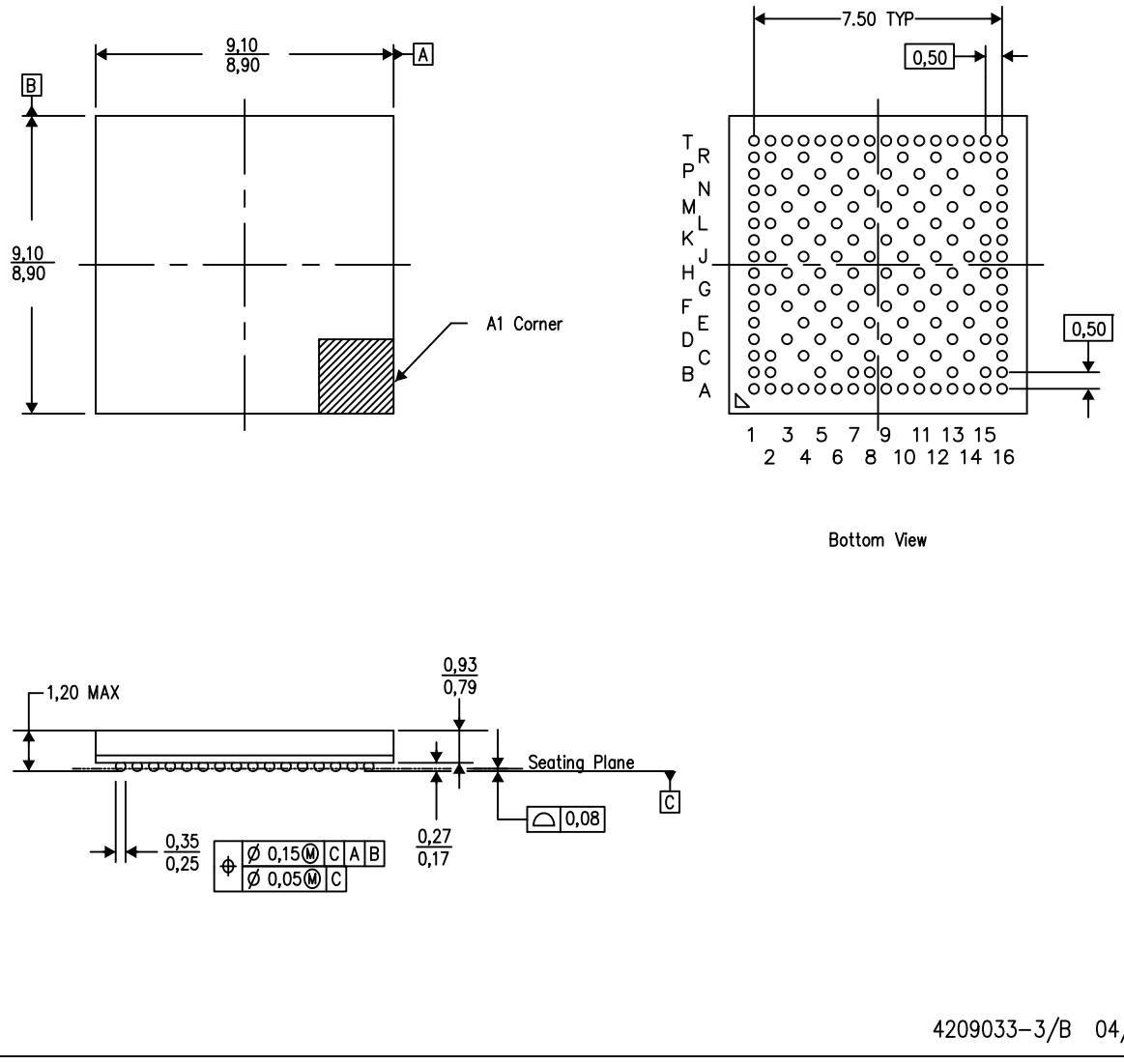
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

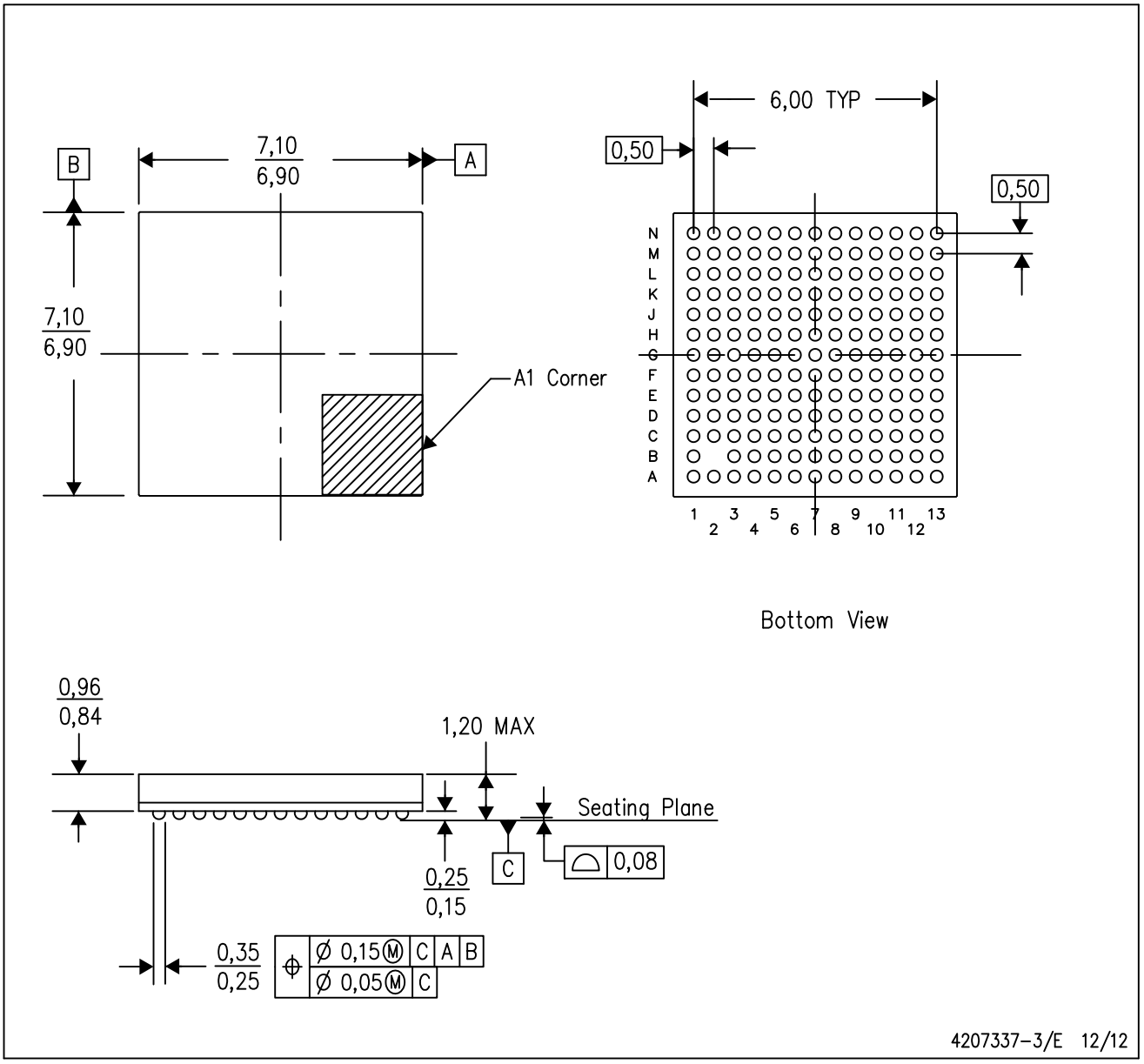
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650830ZAJR	NFBGA	ZAJ	168	2000	336.6	336.6	31.8
TPS650830ZAJT	NFBGA	ZAJ	168	250	336.6	336.6	31.8
TPS650830ZCGR	NFBGA	ZCG	159	1000	336.6	336.6	31.8
TPS650830ZCGT	NFBGA	ZCG	159	250	336.6	336.6	31.8

ZCG (S–PBGA–N159) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

ZAJ (S–PBGA–N168) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265