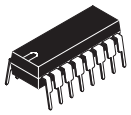


SLUS314C − JANUARY 2000 − REVISED JUNE 2003

LOW VOLTAGE DIFFERENTIAL (LVD) SCSI 9-LINE TERMINATOR

FEATURES

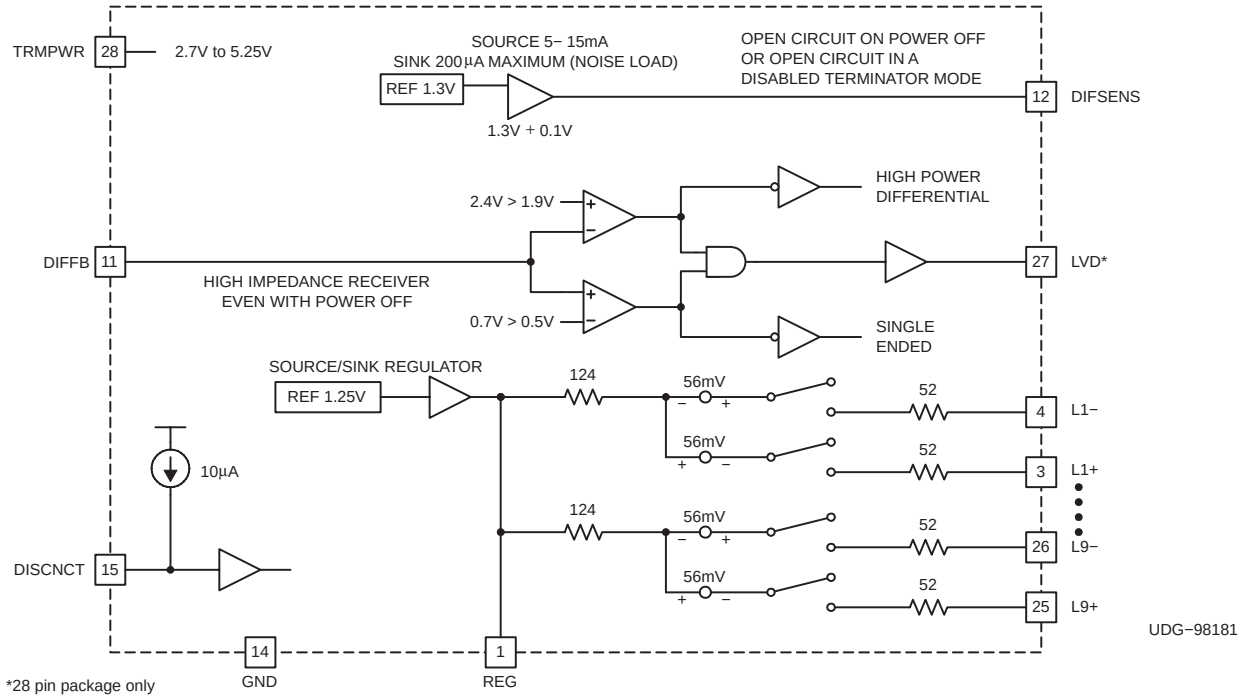
- **First LVD only Active Terminator**
- **Meets SCSI SPI-2 Ultra2 (Fast-40), SPI-3 Ultra3 / Ultra160 (Fast-80) and SPI-4 (Fast-160) Ultra320 Standards**
- **2.7-V to 5.25-V Operation**
- **Differential Failsafe Bias**

DESCRIPTION

The UCC5640 is an active terminator for low voltage differential (LVD) SCSI networks. This LVD only design allows the user to reach peak bus performance while reducing system cost. The device is designed as an active Y-terminator to improve the frequency response of the LVD bus. Designed with a 1.5-pF channel capacitance, the UCC5640 allows for minimal bus loading for a maximum number of peripherals. With the UCC5640, the designer will be able to comply with the Fast-40 SPI-2, Fast-80 SPI-3 and Fast-160 SPI-4 specifications. The UCC5640 also provides a much needed system migration path for ever improving SCSI system standards. This device is available in the 24-pin TSSOP and 28-pin TSSOP for ease of layout use.

The UCC5640 is not designed for use in single ended (SE) or high voltage differential (HVD) systems.

BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

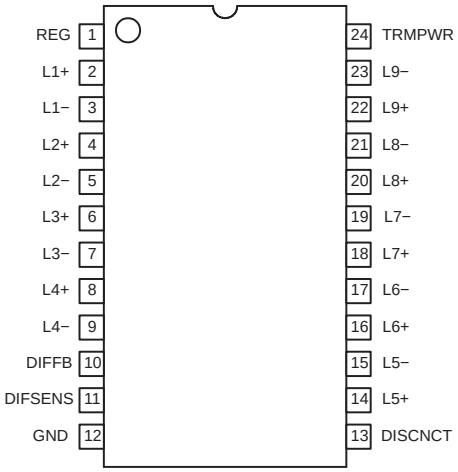
ORDERING INFORMATION

T_A	PACKAGED DEVICE†	
	TSSOP-24 (PW)	TSSOP-28 (PW)
0°C to 70°C	UCC5640PW24	UCC5640PW28

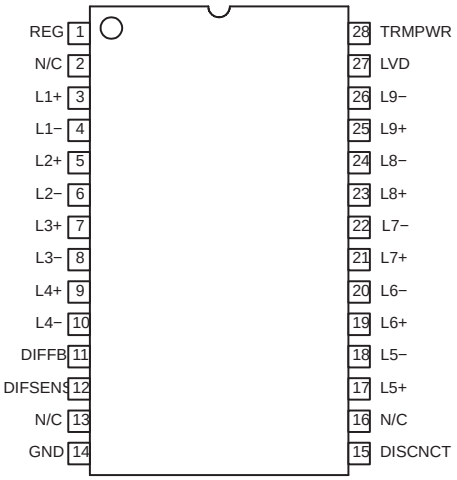
† The TSSOP packages are available taped and reeled. Add TR suffix to device type (e.g. UCC5640PW24TR) to order quantities of 2,000 devices per reel.

CONNECTION DIAGRAM

TSSOP−24 (Top View)
PW Package



TSSOP−28 (Top View)
PW Package



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
TRMPWR voltage	2.7		5.25	V
Signal line voltage	0		3.6	
Disconnect input voltage	0		TRMPWR	°C

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

	UCC5640	UNIT
TRMPWR voltage	6	V
Signal line voltage	0 to 3.6	
Package dissipation	1	W
Storage temperature, T_{stg}	−65 to 150	°C
Operating junction temperature, T_J	–55 to 150	
Lead temperature (soldering, 10 sec.)	300	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, T_A = T_J, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR supply current	No load			25	mA
	Disabled terminator			400	µA
TRMPWR voltage		2.7		5.25	V
Regulator Section					
1.25V regulator	DIFSENS connected to DIFFB	1.15	1.25	1.35	V
1.25V regulator source current	DIFSENS connected to DIFFB		–100	–80	mA
1.25V regulator sink current	DIFSENS connected to DIFFB	80	100		
1.3V regulator	DIFFB connected to GND	1.2	1.3	1.4	V
1.3V regulator source current	DIFSENS to GND	–15		–5	mA
1.3V sink current	DIFSENS to 3.3 V	50		200	µA
Differential Termination Section					
Differential impedance	–2.5 mA to 4.5 mA	100	105	110	Ω
Common mode impedance	L+ connected to L–	110	150	165	
Differential bias voltage	No load, L+ or L–	100		125	mV
Common mode bias		1.15	1.25	1.35	V
Output leakage, disconnect	DISCNCT, TRMPWR = 0 V to 5.25 V, V_{LINE} = 0.2 V to 5.25 V		10	400	nA
Output capacitance	Single ended measurement to ground (1)			3	pF
Low Voltage Differential (LVD) Status Bit Section					
I_{SOURCE}	VLOAD = 2.4 V		–6	–4	mA
I_{SINK}	VLOAD = 0.4 V	2	5		
Disconnect & Differential Sense Input Section					
DISCNCT threshold		0.8		2	V
Input current	At 0 V and 3.3 V	–30	–10		µA
Differential sense SE to LVD threshold		0.5		0.7	V
Differential sense LVD to HPD threshold		1.9		2.4	

NOTE: (1) Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL(1)		I/O	DESCRIPTION
NAME	NO.		
DIFFB	10		Differential sense filter pin should be connected to a 4.7-µF capacitor and 50-kΩ resistor to diff sense.
DIFSENS	11		The SCSI bus differential sense line to detect what type of devices are connected to the SCSI bus.
DISCNCT	13		Disconnect pin shuts down the terminator when it is not at the end of the bus.
GND	12	I	Ground reference for the device.
Ln−		I	Negative line in differential applications for the SCSI bus.
Ln+		I	Positive line in differential applications for the SCSI bus.
LVD		I	Indicates that the bus is in LVD mode (28-pin package only).
REG	1	I	Regulator bypass; must be connected to a 4.7-µF capacitor to ground.
TRMPWR	24	I	V_{IN} 2.7-V to 5.25-V power supply.

NOTE: (1) 24-pin package.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI driver devices are present on the bus. The UCC5640 is a low-voltage differential only device. It senses which types of drivers are present on the bus. If it detects the presence of a single-ended or high-voltage differential driver, the UCC5640 will place itself in a high-impedance input state, effectively disconnecting the chip from the bus.

The UCC5640 senses what drivers are present on the bus by the voltage on SCSI bus control line DIFFSENS, which is monitored by the DIFFB input pin. The DIFSENS output pin on the UCC5640 attempts to drive a DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFFSENS line will be successfully driven to that voltage. If HVD drivers are present, they will pull the DIFFSENS line high. If any single-ended drivers are present, they pull the DIFSENS line to ground (even if HVD drivers are also present on the bus). If the voltage on the DIFFB is below 0.5 V or above 2.4 V, the UCC5640 enters the high-impedance SE/HVD state. If it is between 0.7 V and 1.9 V, the UCC5640 enters the LVD mode. These thresholds accommodate differences in ground potential that can occur between the ends of long bus lines.

Three UCC5640 devices are required at each end of the SCSI bus to terminate 27 lines (18 data, 9 control). Every UCC5640 contains a DIFSENS driver, but only one should be used to drive the line at each end. The DIFSENS pin on the other devices should be left unconnected.

On power up, the voltage on the TRMPWR pin rising above 2.7 V, the UCC5640 assumes the SE/HVD mode.

The DIFFB inputs on all three chips at each end of the bus should be connected together. Properly filtered, noise on DIFFB will not cause a false mode change. There should be a shared 50-Hz noise filter implemented on DIFFB at each end of the bus as close as possible to the DIFFB pins. This is implemented with a 50-kΩ resistor between the DIFFB and DIFSENS pins, and a 4.7-µF capacitor from DIFFB to ground. See Figure 1, the typical application diagram on page 6.

In LVD mode, the regulated voltage is switched to 1.25 V and a resistor network is presented to each line pair that provides common-mode impedance of 150 Ω and differential impedance of 105 Ω. The lines in each differential pair are biased so that when not driven, Line(n)+ and Line(n)− are driven 56 mV below and above the common-mode bias voltage of 1.25 V respectively.

In SE/HVD mode, all the terminating resistors are switched off the bus. The 1.25 V and 1.3 V (DIFSENS) regulators are left on.

When the disconnect input (DISCNCT) is active (high), the terminating resistors are switched off the bus and both voltage regulators are turned off to save power. The mode change filter/delay function is still active and the LVD pin in the 28-pin package continues to indicate the correct bus mode.

APPLICATION INFORMATION

The UCC5640 operates down to a TRMPWR voltage of 2.7 V. This accommodates a 3.3-V system with allowance for supply tolerance of +10%, a unidirectional fusing device and cable drop. The UCC3912 or UCC3918 is recommended on a 3.3-V systems and the UCC3916 is recommended on 5-V systems in place of a fuse and diode implementation, as its lower voltage drop provides additional voltage margin for the system.

Layout is important in all SCSI implementations and critical in SPI-3 and SPI-4 systems, which have stringent requirements on both the absolute value of capacitance on differential signal lines and the balancing of capacitance between paired lines and from pair-to-pair.

Feedthroughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multilayer power and ground plane spacing adds about 1 pF to each plane. Each feed-through will add 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes reduces capacitance. Opening up the power and ground planes under a through-hole connector reduces added capacitance in those applications. Capacitance is also affected by components in close proximity on both sides of the board.

Table 1. Maximum Capacitance

SCSI CLASS	TRACE TO GND: REQ, ACK, DATA, PARITY, P_CRCA	TRACE TO TRACE: REQ, ACK, DATA, PARITY, P_CRCAALS	TRACE TO GND: OTHER SIGNALS	TRACE TO TRACE: OTHER SIGNALS
Ultra1	25 pF	N/A	25 pF	N/A
Ultra2	20 pF	10 pF	25 pF	13 pF
Ultra3/Ultra160	15 pF	8 pF	25 pF	13 pF
Ultra320	13 pF	6.5 pF	21 pF (est.)	10 pF (est.)

TI terminators are designed with very tightly controlled capacitance on their signal lines. Between the positive and negative lines in a differential pair the difference is typically no more than 0.1 pF, and only 0.3 pF between pairs.

Multilayer boards need to adhere to the 120-Ω impedance standard, including the connector and feedthroughs. Bus traces are normally run on the outer layers of the board with 4-mil etch and 4-mil spacing between the two lines in each differential pair, and a minimum of 8-mil spacing to adjacent pairs to minimize crosstalk. Microstrip technology is too low in impedance and should not be used, they are designed for 50-Ω rather than 120-Ω differential systems.

Decoupling capacitors should be installed as close as possible to the following input pins of the UCC5640:

1. TRMPWR: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high frequency, low ESR)
2. REG: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high frequency, low ESR)

APPLICATION INFORMATION

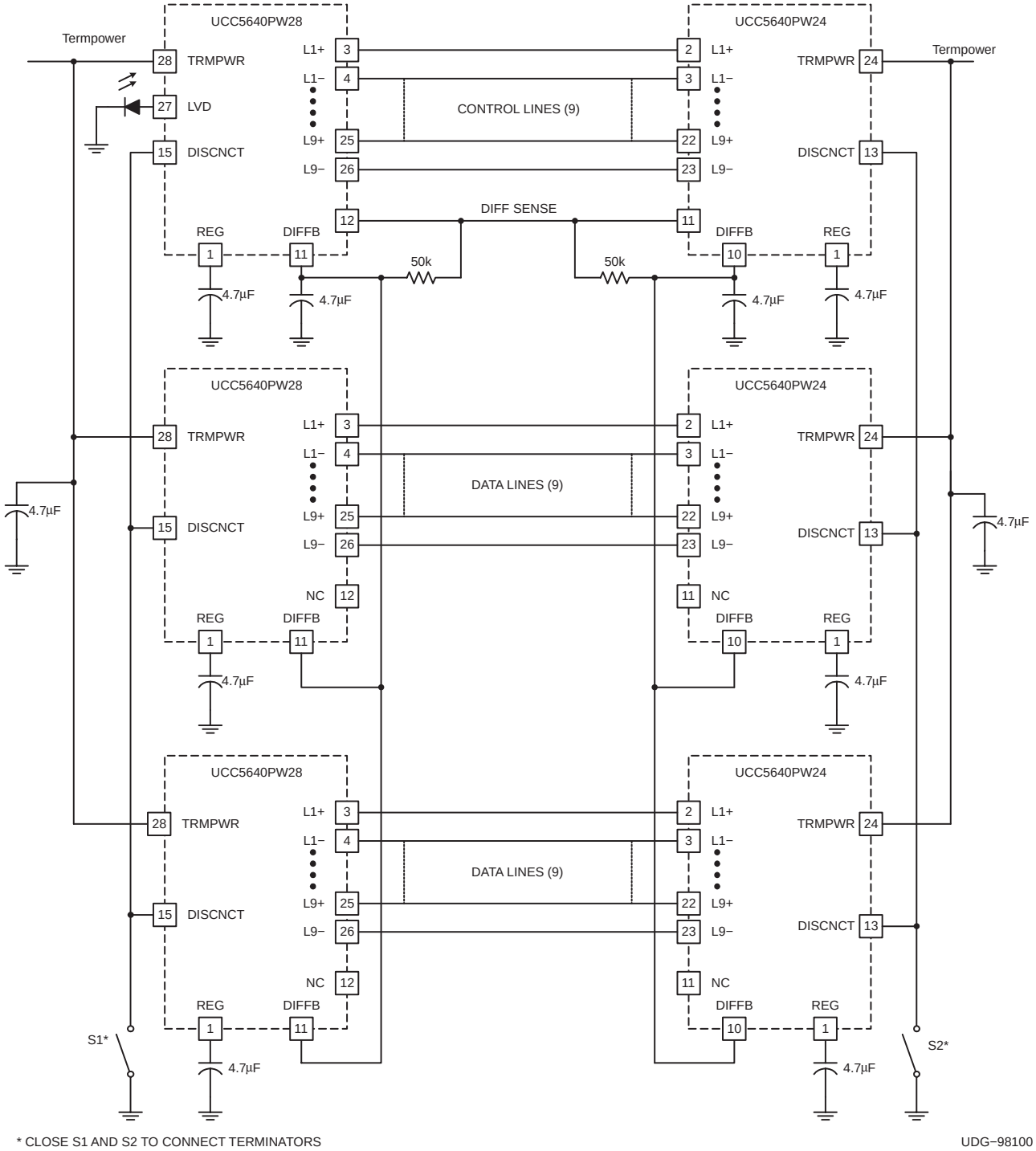


Figure 1. Application Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5640PW24TR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5640PW -24
UCC5640PW24TR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5640PW -24

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

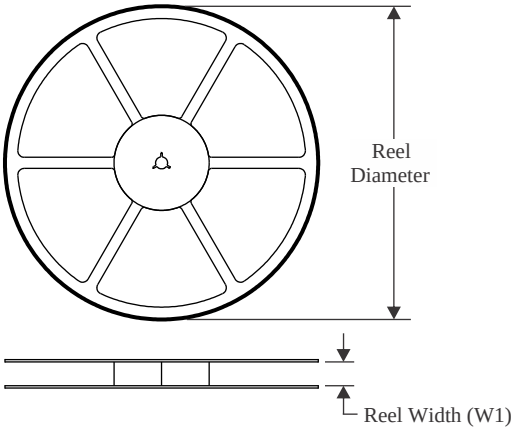
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

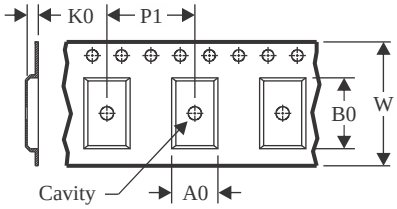
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

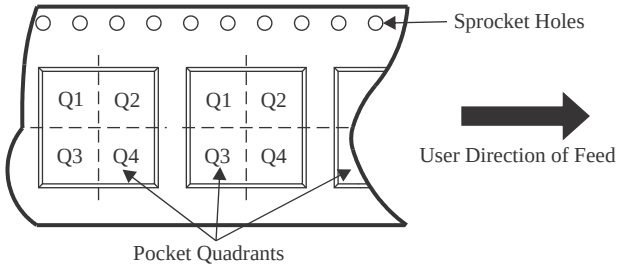


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

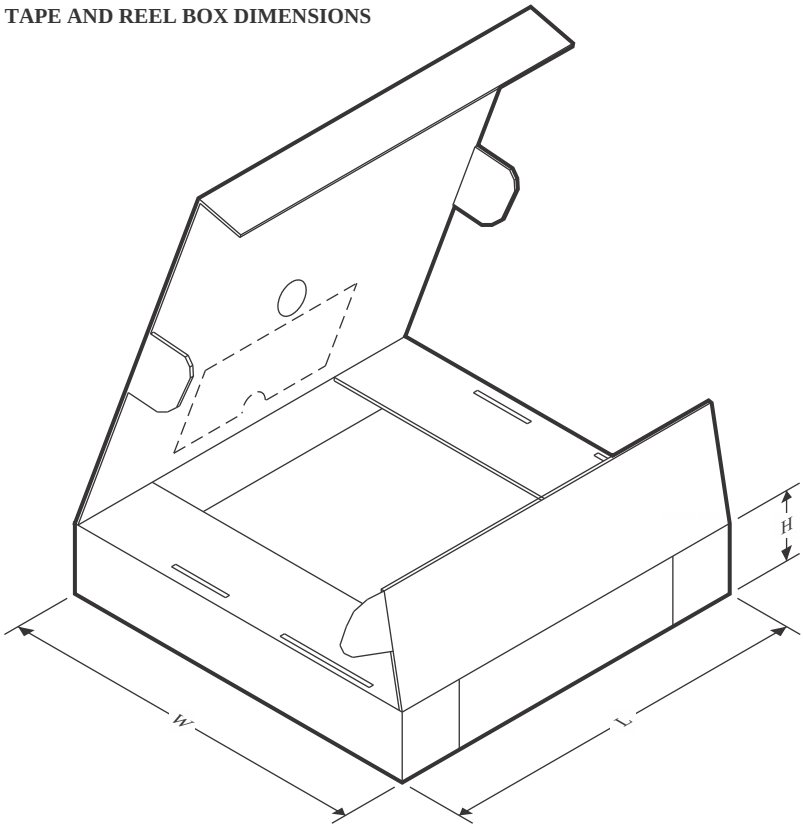
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5640PW24TR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

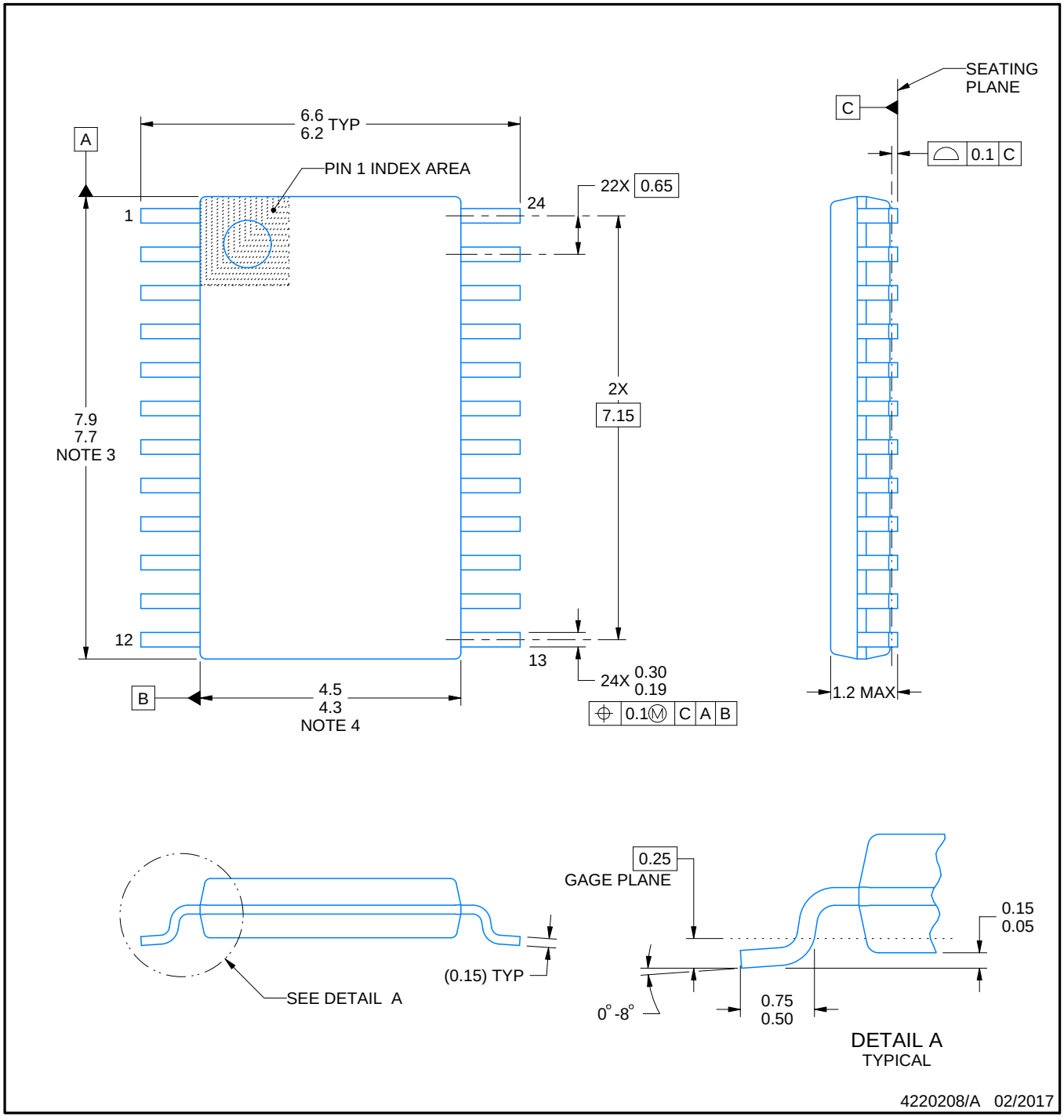
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5640PW24TR	TSSOP	PW	24	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0024A

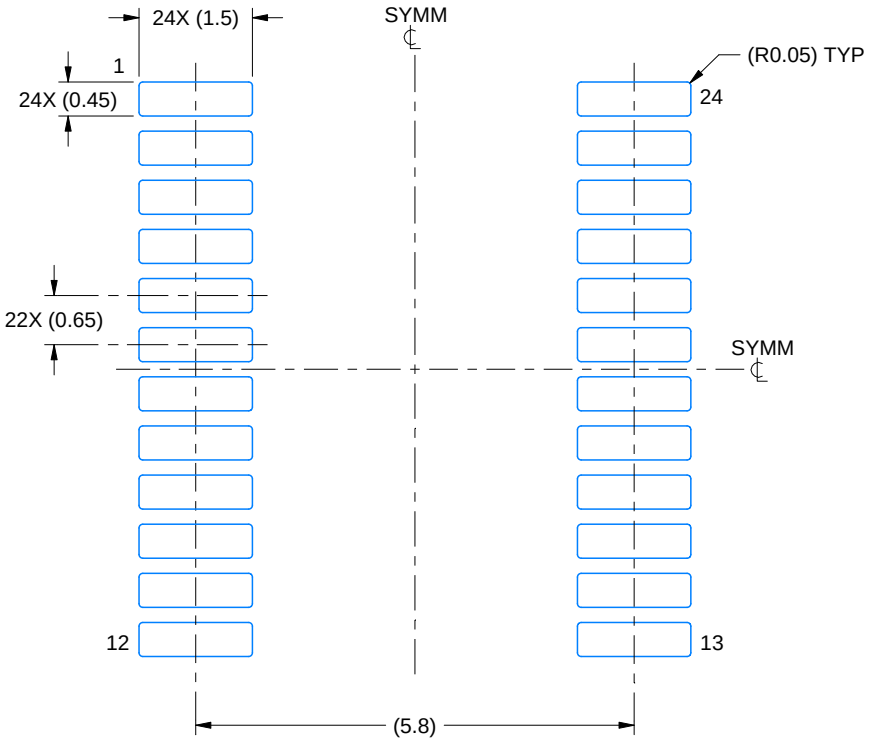
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

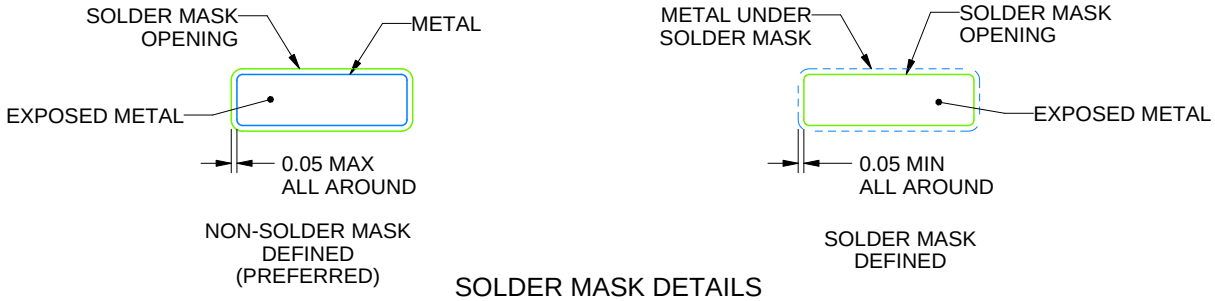


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

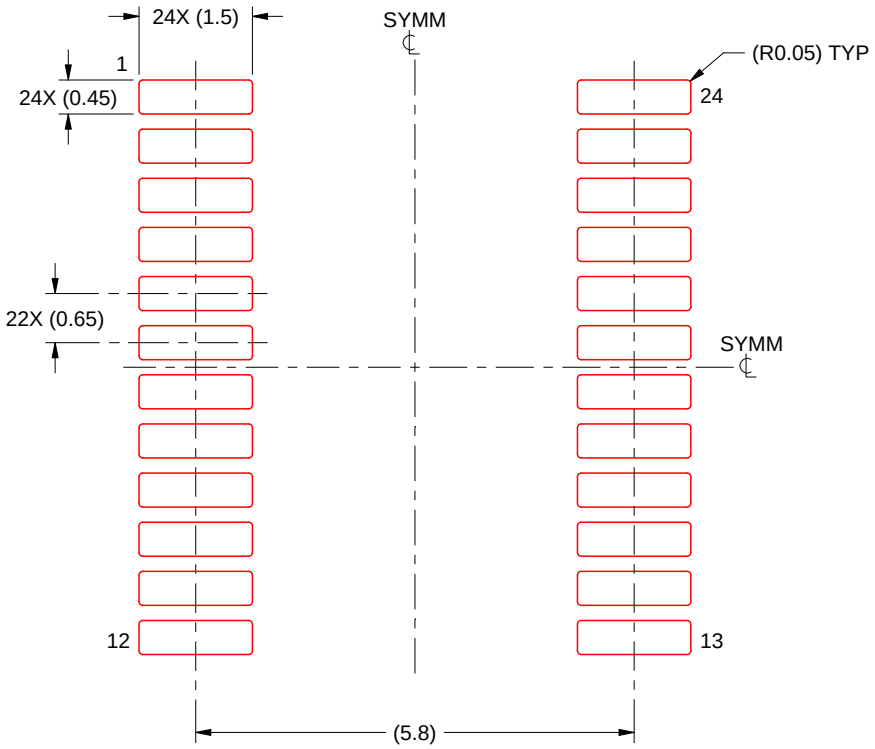


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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