

Multimode (LVD/SE) SCSI 9 Line Terminator

FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter/Delay
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD), Ultra3/Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards
- Supports Active Negation
- 3pF Channel Capacitance

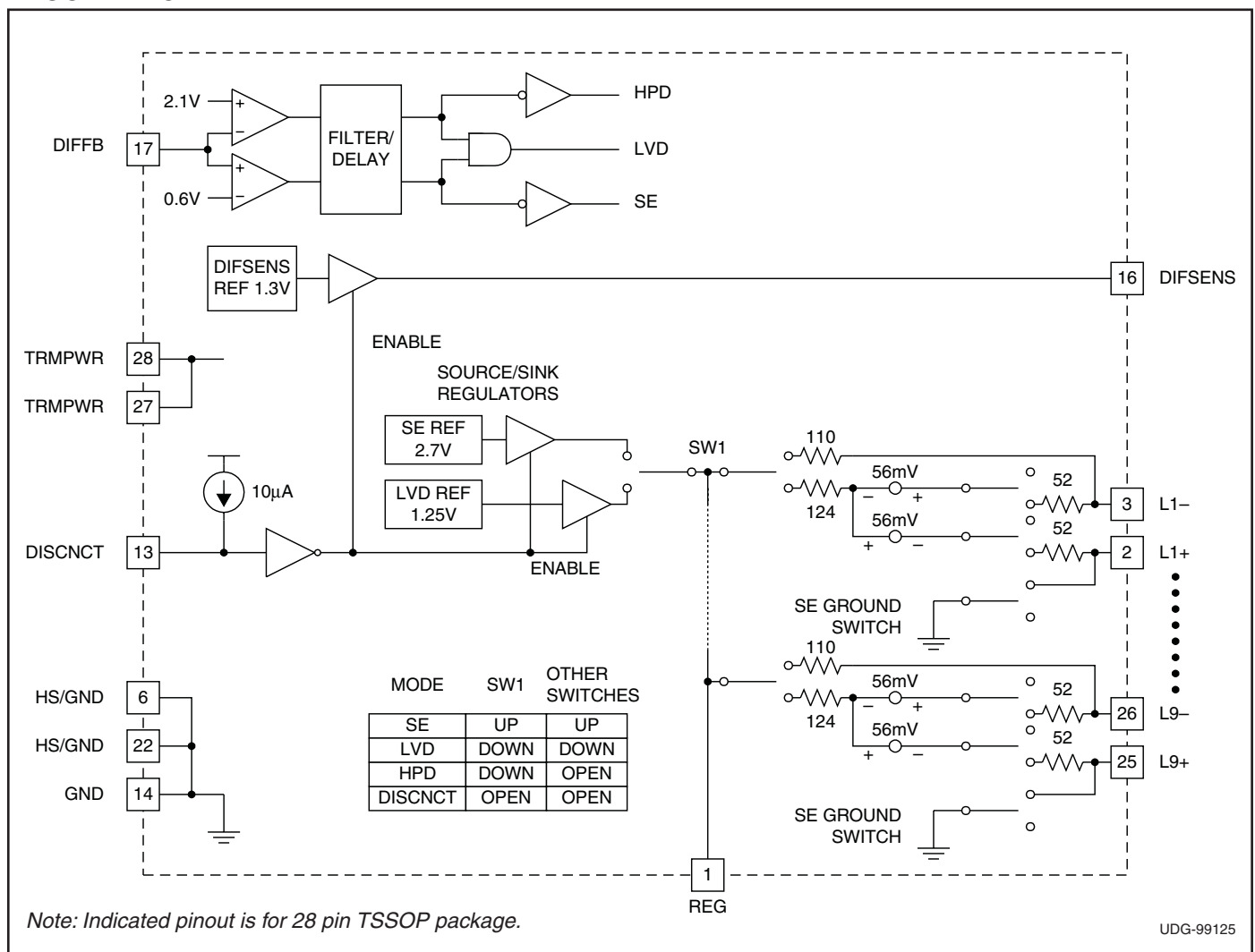
DESCRIPTION

The UCC5672 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets.

The automatic mode select/change feature switches the terminator between Single Ended or LVD SCSI Termination, depending on the bus mode. If the bus is in High Voltage Differential Mode, the terminator lines transition into a High Impedance state.

The UCC5672 is SPI-4, SPI-3, SPI-2, and SCSI-2 compliant. This device is offered in a 28 pin TSSOP package to minimize the footprint. The UCC5672 is also available in a 36 pin MWP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage	6V
Signal Line Voltage	0V to 5V
Storage Temperature	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10sec.)	+300°C

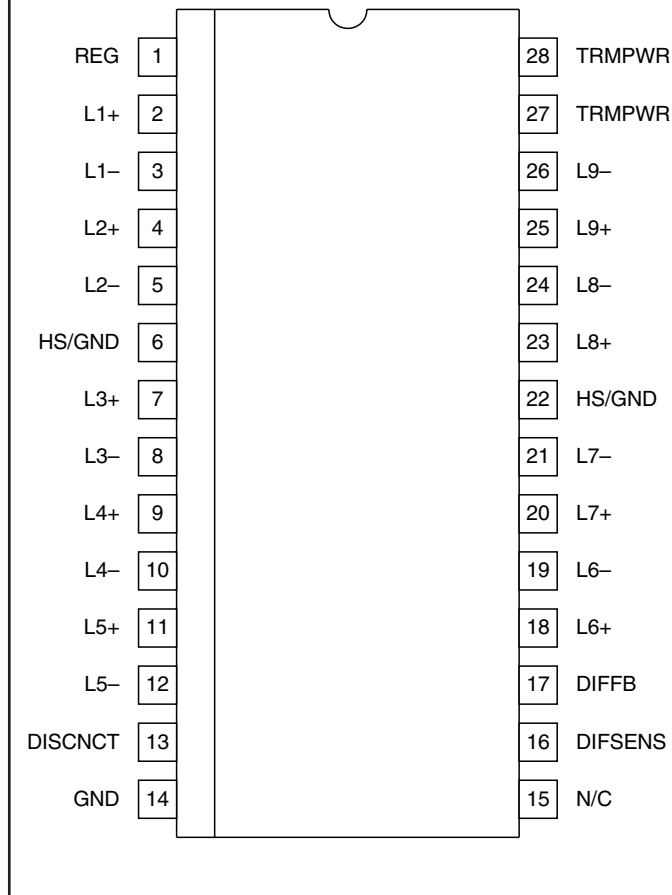
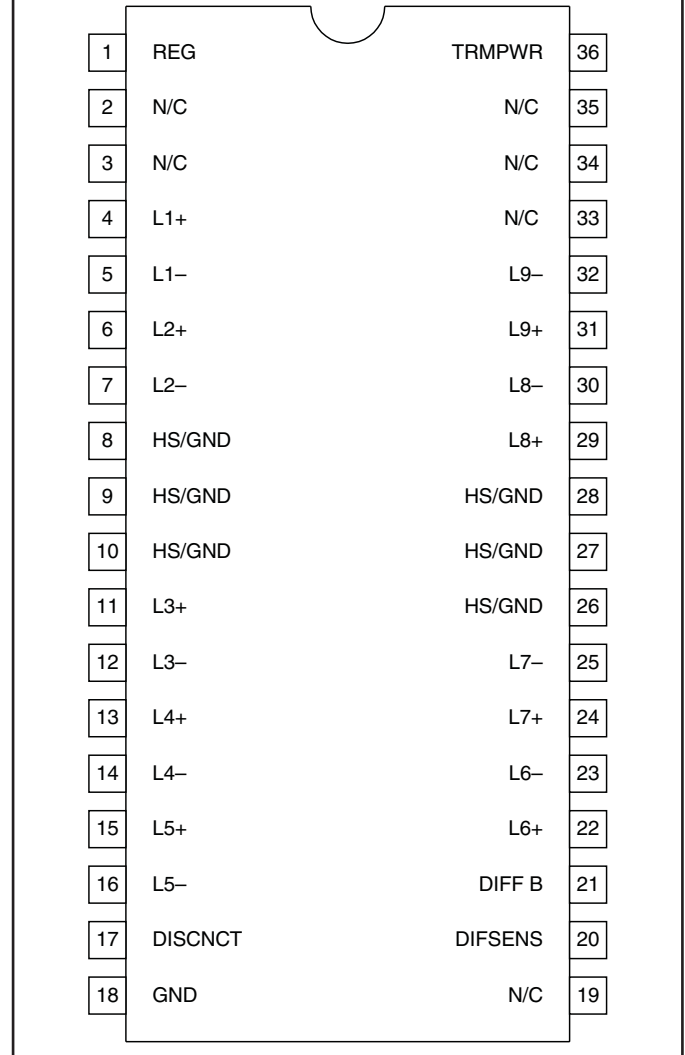
All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage	2.7V to 5.25V
----------------	---------------

AVAILABLE OPTIONS

T _A	Packaged Devices
0°C to 70°C	UCC5672MWP
	UCC5672PWP

CONNECTION DIAGRAM**TSSOP-28 (TOP VIEW)
PWP Package****QSOP-36 (TOP VIEW)
MWP Package**

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C ,
TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD SCSI Mode		23	35	mA
	SE Mode		14	25	mA
	DISCNCT Mode		250	500	μA
Regulator Section					
1.25V Regulator Output Voltage	LVD SCSI Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	-225	-420	-800	mA
1.25V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	100	180	420	mA
2.7V Regulator Output Voltage	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	-225	-420	-800	mA
2.7V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	100	180	420	mA
Diff Sense Driver (DIFSENS) Section					
1.3V DIFSENS Output Voltage	DIFSENS	1.2	1.3	1.4	V
1.3V DIFSENS Source Current	$V_{\text{DIFSENS}} = 0\text{V}$	-5		-15	mA
1.3V DIFSENS Sink Current	$V_{\text{DIFSENS}} = 2.75\text{V}$	50		200	μA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance	$Z = (V_{L_X} - 0.2\text{V}) / I_{L_X}$, (Note 3)	100	108	116	Ω
Termination Current	Signal Level 0.2V, All Lines Low	-20	-23	-25.4	mA
	Signal Level 0.5V	-17		-22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	$I = 10\text{mA}$		20	60	Ω
Disconnect (DISCNCT) and Diff Buffer (DIFFB) Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			-10	-30	μA
DIFFB SE to LVD SCSI Threshold		0.5		0.7	V
DIFFB LVD SCSI to HPD Threshold		1.9		2.4	V
DIFFB Input Current		-1		1	μA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C , TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Time Delay/Filter Section					
Mode Change Delay	A new mode change can start any time after a previous mode change has been detected. (Note4)	100	180	300	ms

Note 1: Guaranteed by design. Not 100% tested in production.

Note 2: $Z_{CM} = \frac{1.2V}{I_{(V_{CM}+0.6V)} - I_{(V_{CM}-0.6V)}}$; Where V_{CM} = Voltage measured with $L+$ tied to $L-$ and zero current applied;

Note 3: V_{LX} = Output voltage for each terminator minus output pin ($L1-$ through $L9-$) with each pin unloaded.
 I_{LX} = Output current for each terminator minus output pin ($L1-$ through $L9-$) with the minus output pin forced to 0.2V.

Note 4: Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to any other mode. Within 300ms after power is applied the mode is defined by the voltage of DIFFB.

PIN DESCRIPTIONS

DIFFB: Input pin for the comparators that select SE, LVD SCSI, or HIPD modes of operation. This pin should be decoupled with a 0.1 μ F capacitor to ground and then coupled to the DIFSENS pin through a 20k Ω resistor.

DIFSENS: Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

DISCNCT: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to activate the terminator or open pin to disable the terminator.

HS/GND: Heat sink ground pins. These should be connected to large ground area PC board traces to increase the power dissipation capability.

GND: Power Supply return.

L1– thru L9–: Termination lines. These are the active lines in SE mode and are the negative lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

L1+ thru L9+: Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

REG: Regulator bypass pin, must be connected to a 4.7 μ F capacitor to ground.

TRMPWR: 2.7V to 5.25V power input pin. Bypass near the terminators with a 4.7 μ F capacitor to ground.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5672 is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) SCSI devices might coexist. The UCC5672 has both SE and LVD SCSI termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5672 DIFSENS drivers will try to de-

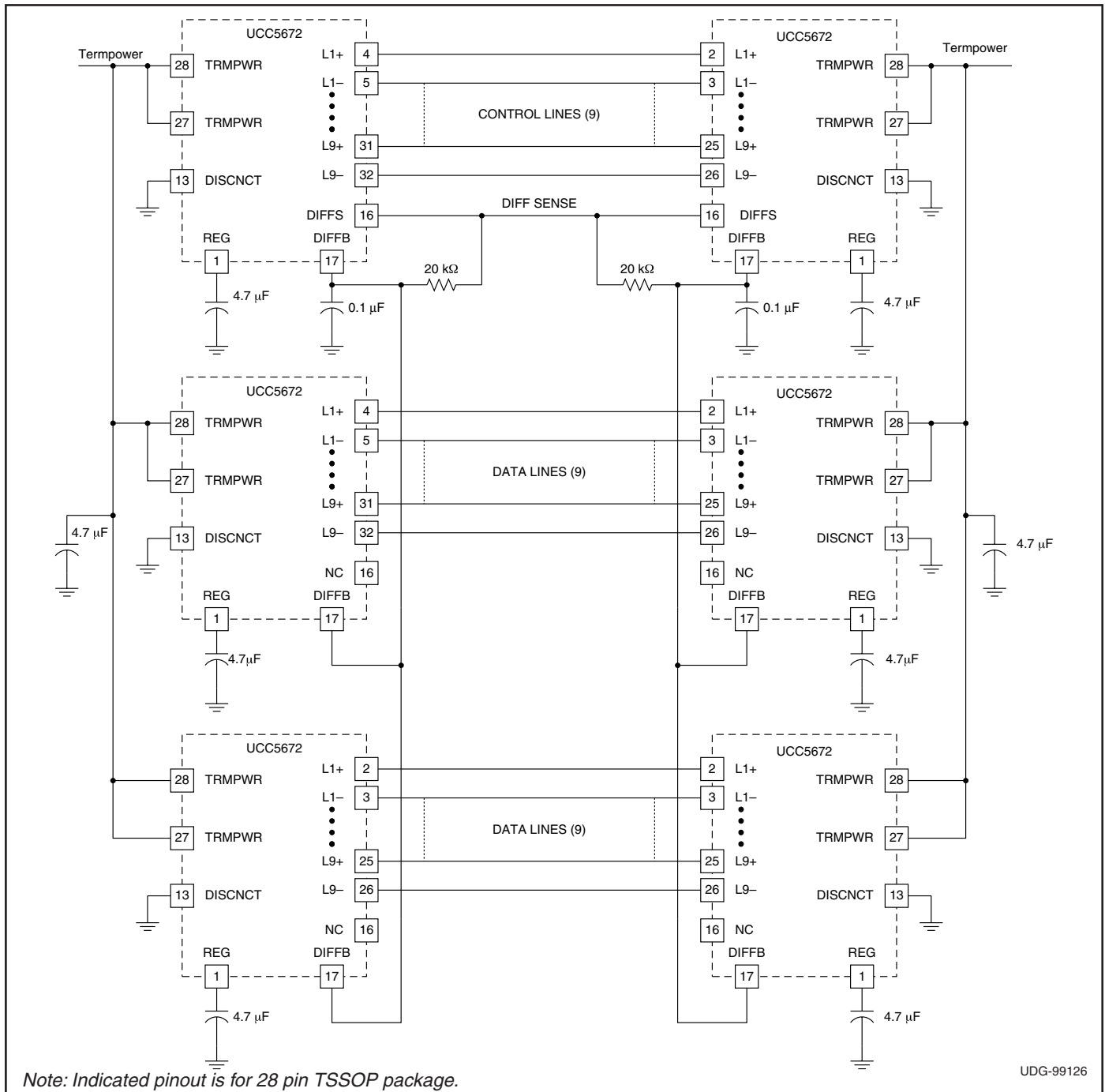
liver 1.3V to the DIFSENS line. If only LVD SCSI devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD SCSI operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5672(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) SCSI devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termi-

APPLICATION INFORMATION (cont.)

nation for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is set for single ended. Between 0.7V and 1.9V, the termination network switches to LVD SCSI, and above 2.4V indicates HVD SCSI, causing the terminators to disconnect from the bus. These thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5672 multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems,



UDG-99126

Figure 1. Application diagram.

APPLICATION INFORMATION (cont.)

with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3918 is recommended in place of the fuse and diode. The UCC3918's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2, Ultra3/Ultra160 and Ultra320 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about

1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD SCSI or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5672 is offered in a 28 pin TSSOP. This package includes two heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. Both of the HS/GND pins need to be connected to etch area or four feed-through per pin connecting to the ground plane layer on a multi-layer board.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5672PWP	Active	Production	TSSOP (PW) 28	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP
UCC5672PWP.A	Active	Production	TSSOP (PW) 28	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP
UCC5672PWPTR	Obsolete	Production	TSSOP (PW) 28	-	-	Call TI	Call TI	0 to 70	UCC5672PWP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

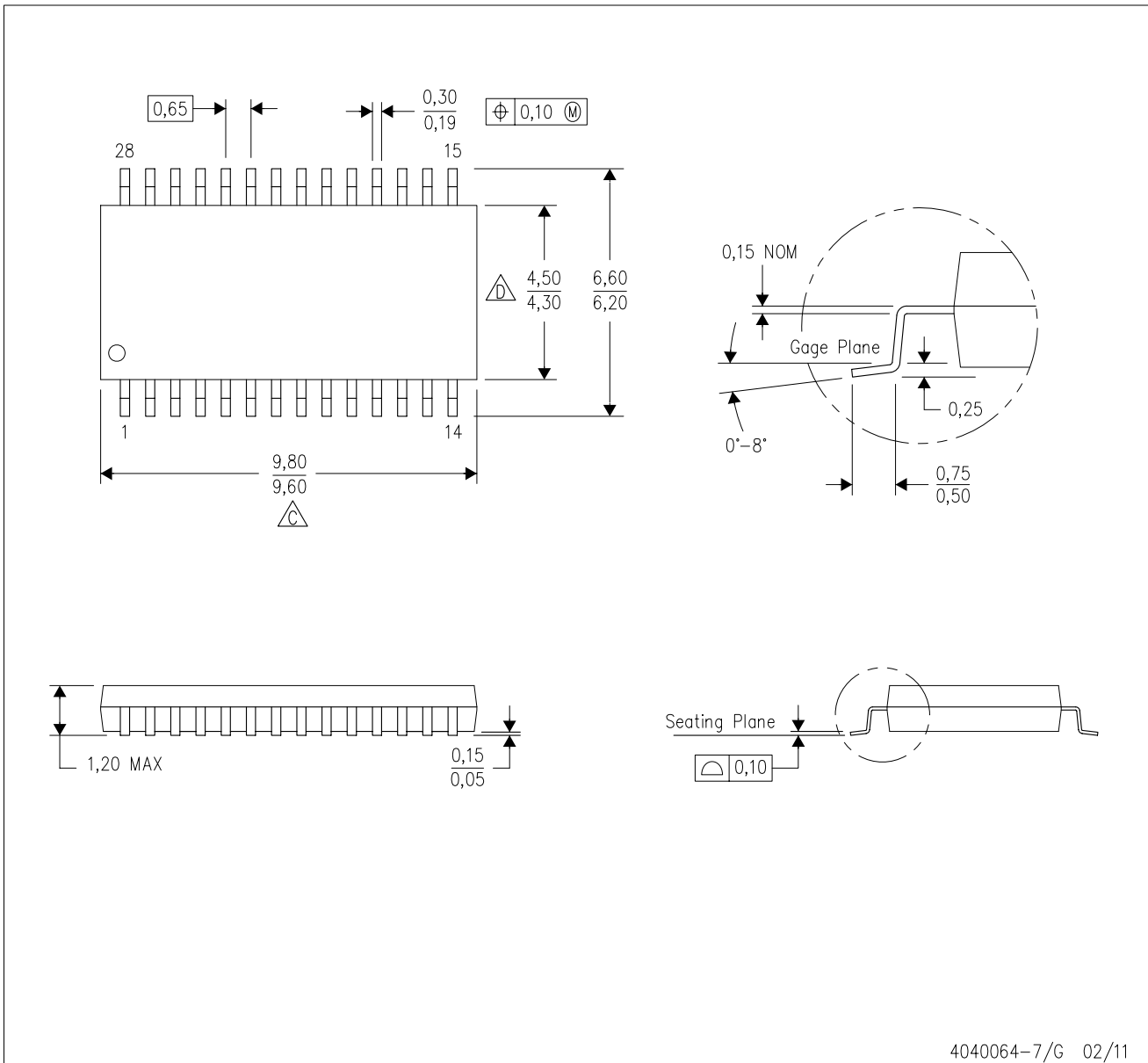


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UCC5672PWP	PW	TSSOP	28	50	530	10.2	3600	3.5
UCC5672PWP.A	PW	TSSOP	28	50	530	10.2	3600	3.5

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated