

Precision Analog Controller

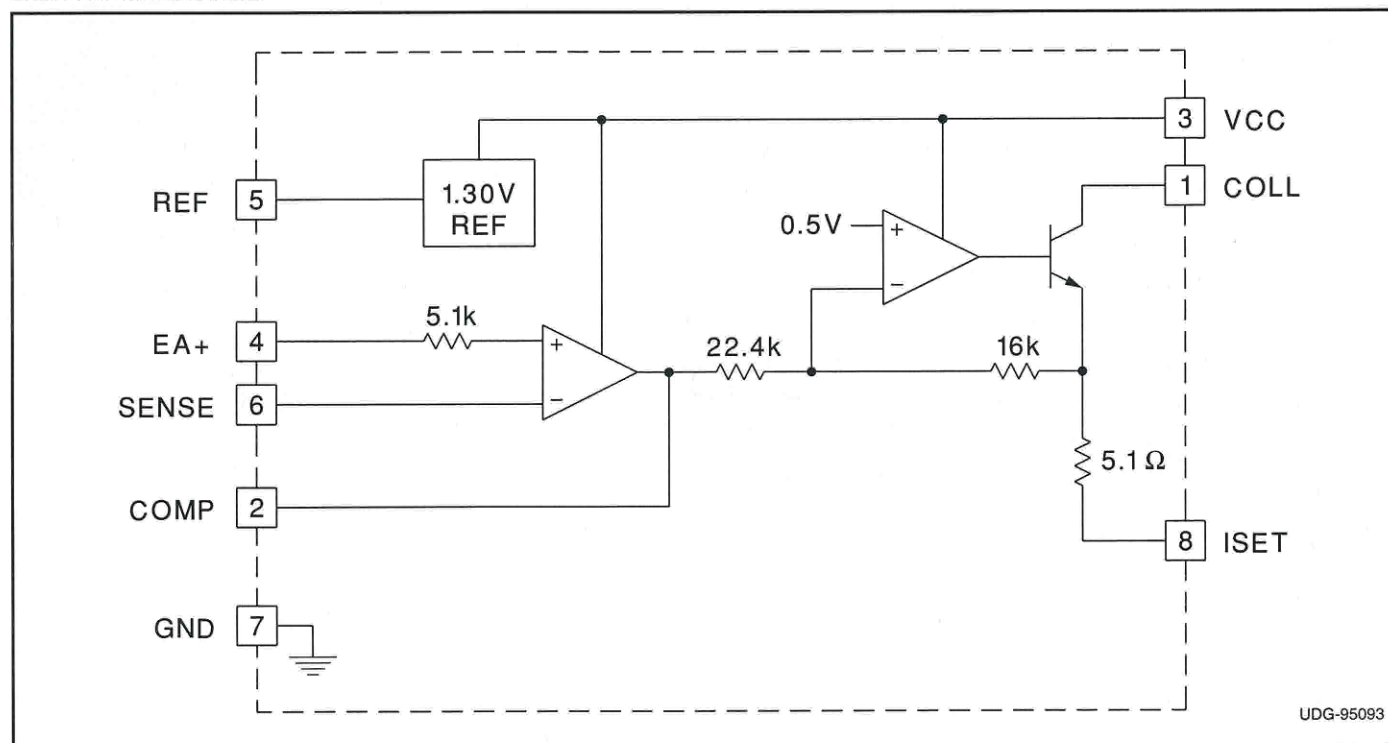
FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.30V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 24.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC39432 is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC39431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as external programming capability.

BLOCK DIAGRAM



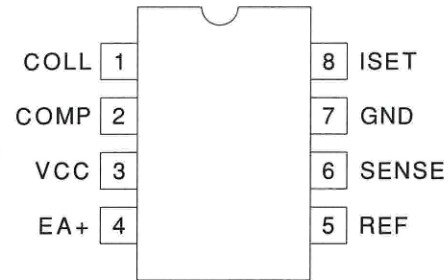
CONNECTION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: VCC 24V
Regulated Output: V_{COLL} 24V
EA Input: SENSE, EA+ 6V
EA Compensation: COMP 6V
Reference Output: REF 6V
Output Sink Current: I_{COLL} 140mA
Output Source Current: ISET -140mA
Power Dissipation at T_A ≤ 25°C (DIL-8) 1W
Derate 8mW/°C for T_A > 25°C
Storage Temperature Range -65°C to +150°C
Junction Temperature -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C and COLL Output = 2.4V to 24.0V for the UC19432, T_A = -25°C to +85°C and COLL Output = 2.3V to 24.0V for the UC29432, and T_A = 0°C to +70°C and COLL Output = 2.3V to 24.0V for the UC39432, VCC = 15V, I_{COLL} = 10mA, T_A = T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	T _A = 25°C	19432*	1.295	1.3	1.305	V
		39432B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V _{COLL} = 5.0V	19432*	1.291	1.3	1.309	V
		39432B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.4V to 24.0V, V _{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Load Regulation	I _{COLL} = 10mA to 50mA, V _{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Sink Current					10	μA
Reference Source Current					-10	μA
EA Input Bias Current			-0.5	-0.2		μA
EA Input Offset Voltage		19432*			4.0	mV
		39432B			4.0	mV
EA+ Operational Voltage Limitations	(Note 1)		0.9		1.6	V
EA Output Current Sink (Internally Limited)					16	μA
EA Output Current Source					-1	mA
Minimum Operating Current	VCC = 24.0V, V _{COLL} = 5V			0.50	0.80	mA
Collector Current Limit (Note)	V _{COLL} = VCC = 24.0V, Ref = 1.35V ISET = GND			130	145	mA
Collector Saturation	I _{COLL} = 20mA		0.7	1.1	1.5	V
Transconductance (gm) (Note)	VCC = 2.4V to 24.0V, V _{COL} = 3V, I _{COLL} = 20mA ISET = GND	19432*	-170	-140	-110	mS
		39432B	-180	-140	-100	mS
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

* Also applies to the UC29432 and UC39432

Note: Programmed transconductance and collector current limit equations are specified in the ISET pin description.

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 24V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is $g_m \cdot R_L$, where g_m is designed to be $-140\text{mS} \pm 30\text{mS}$ and R_L represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

EA+: The non-inverting input to the error amplifier.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET: The current set pin for the transconductance amplifier. The transconductance will be -140mS as specified in the electrical table if this pin is grounded. If a resistance R_L is added to the ISET pin, the resulting new transconductance is calculated using the following equation: $g_m = -0.714\text{V} \cdot (5.1\Omega + R_L)$. The maximum current will be approximately

$$I_{MAX} = \frac{0.6\text{V}}{5.1\Omega + R_L}$$

REF: The output of the trimmed precision reference. It can source or sink $10\mu\text{A}$ and still maintain the 1% temperature specification.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the UC39431 shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 24.0V. The quiescent current is typically 0.50mA.

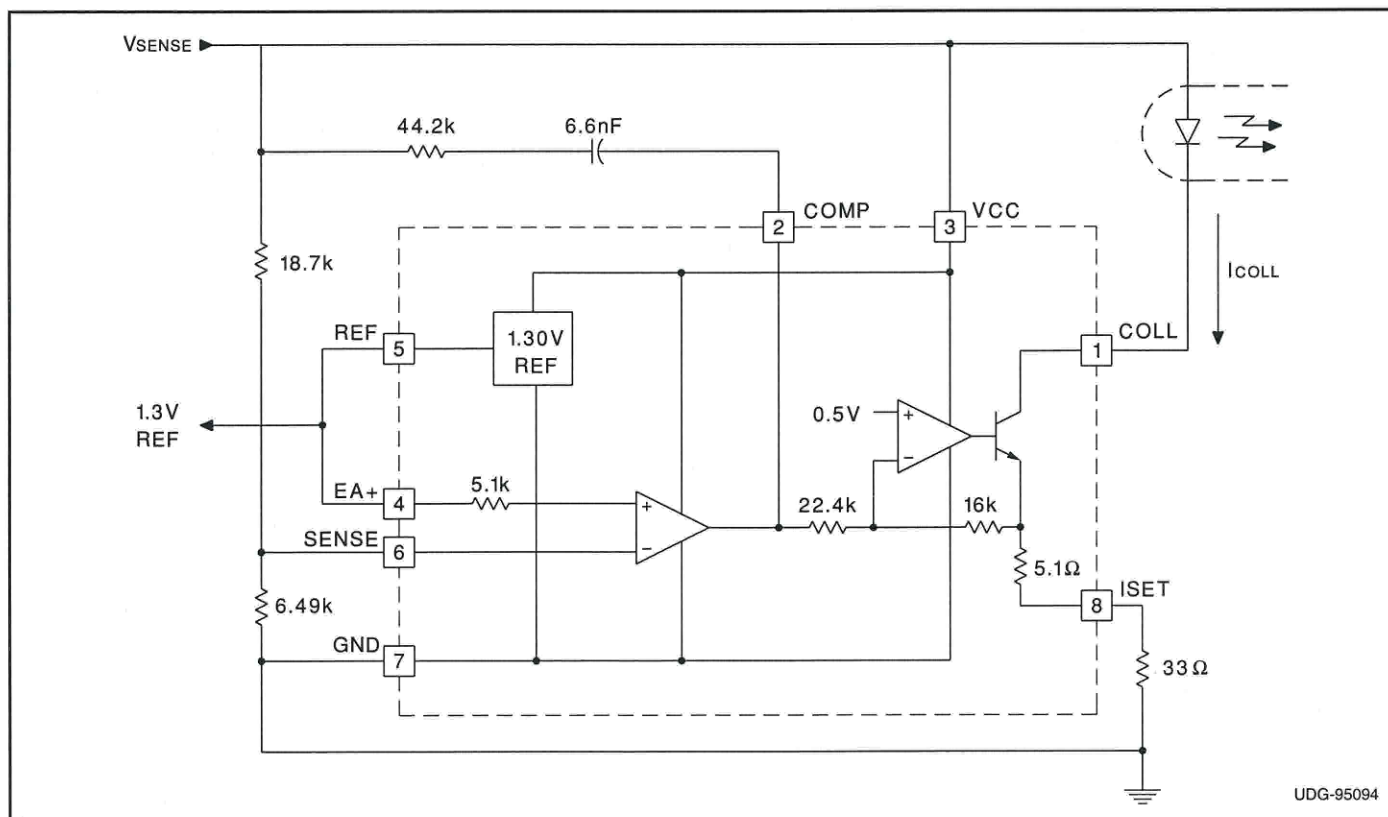


Figure 1. 5.0V Optocoupler application.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC29432D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC29432
UC29432D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC29432
UC29432DTR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC29432
UC29432DTR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC29432
UC29432N	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC29432N
UC29432N.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC29432N
UC39432BD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(39432B, UC39432BD)
UC39432BD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(39432B, UC39432BD)
UC39432D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC39432
UC39432D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC39432
UC39432N	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC39432N
UC39432N.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC39432N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC29432, UC29432M :

- Catalog : [UC29432](#)
- Military : [UC29432M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC29432DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC29432DTR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC29432D	D	SOIC	8	75	506.6	8	3940	4.32
UC29432D.A	D	SOIC	8	75	506.6	8	3940	4.32
UC29432N	P	PDIP	8	50	506	13.97	11230	4.32
UC29432N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC39432BD	D	SOIC	8	75	506.6	8	3940	4.32
UC39432BD.A	D	SOIC	8	75	506.6	8	3940	4.32
UC39432D	D	SOIC	8	75	506.6	8	3940	4.32
UC39432D.A	D	SOIC	8	75	506.6	8	3940	4.32
UC39432N	P	PDIP	8	50	506	13.97	11230	4.32
UC39432N.A	P	PDIP	8	50	506	13.97	11230	4.32

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