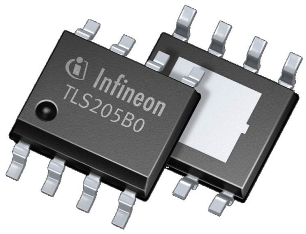
OPTIREG™ linear TLS205B0EJ V50

Datasheet

Family overview | Technical documents | Software and tools | Support | Order now

Low dropout, low noise, linear voltage post regulator, 500 mA



Features

- Low noise down to 42 μV_{RMS} (BW = 10 Hz to 100 kHz)
- 500 mA current capability
- Low quiescent current: 30 µA
- Wide input voltage range up to 20 V
- Internal circuitry working down to 2.3 V
- 2.5% output voltage accuracy (over full temperature and load range)
- Low dropout voltage: 350 mV
- Very low shutdown current: < 1 µA
- No protection diodes needed
- Fixed output voltage: 5.0 V
- Stable with output capacitor ≥ 3.3 µF
- Stable with aluminium, tantalum, or ceramic output capacitors
- Reverse polarity protection
- No reverse current
- Protected against overcurrent and overtemperature
- PG-DSO-8 exposed-pad package
- Green Product (RoHS-compliant)

Potential applications

Suitable for use in automotive electronics as post regulator

Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLS205B0EJ V50 is a micropower, low-noise, low-dropout 5 V voltage regulator capable of supplying an output current of 500 mA with a dropout voltage of 350 mV. With a very low quiescent current of 30 µA, the TLS205B0EJ V50 voltage regulator is perfectly suited for automotive battery-powered systems.

A key feature of the TLS205B0EJ V50 is its low output noise. By adding an external 10 nF bypass capacitor, output noise values down to 42 μV_{RMS} over a bandwidth from 10 Hz to 100 kHz can be reached. The voltage regulator is stable with an output capacitor as small as 3.3 µF. Small ceramic capacitors can be used without the series resistance required by many other linear voltage regulators.

Internal protection circuitry includes reverse battery protection, current limiting, and reverse current protection.

The TLS205B0EJ V50 provides a fixed output voltage of 5 V and is available in a PG-DSO-8 exposed-pad package.

Type	Package	Marking
TLS205B0EJ V50	PG-DSO-8 exposed-pad	205B0V50

Table of contents

1 Block diagram

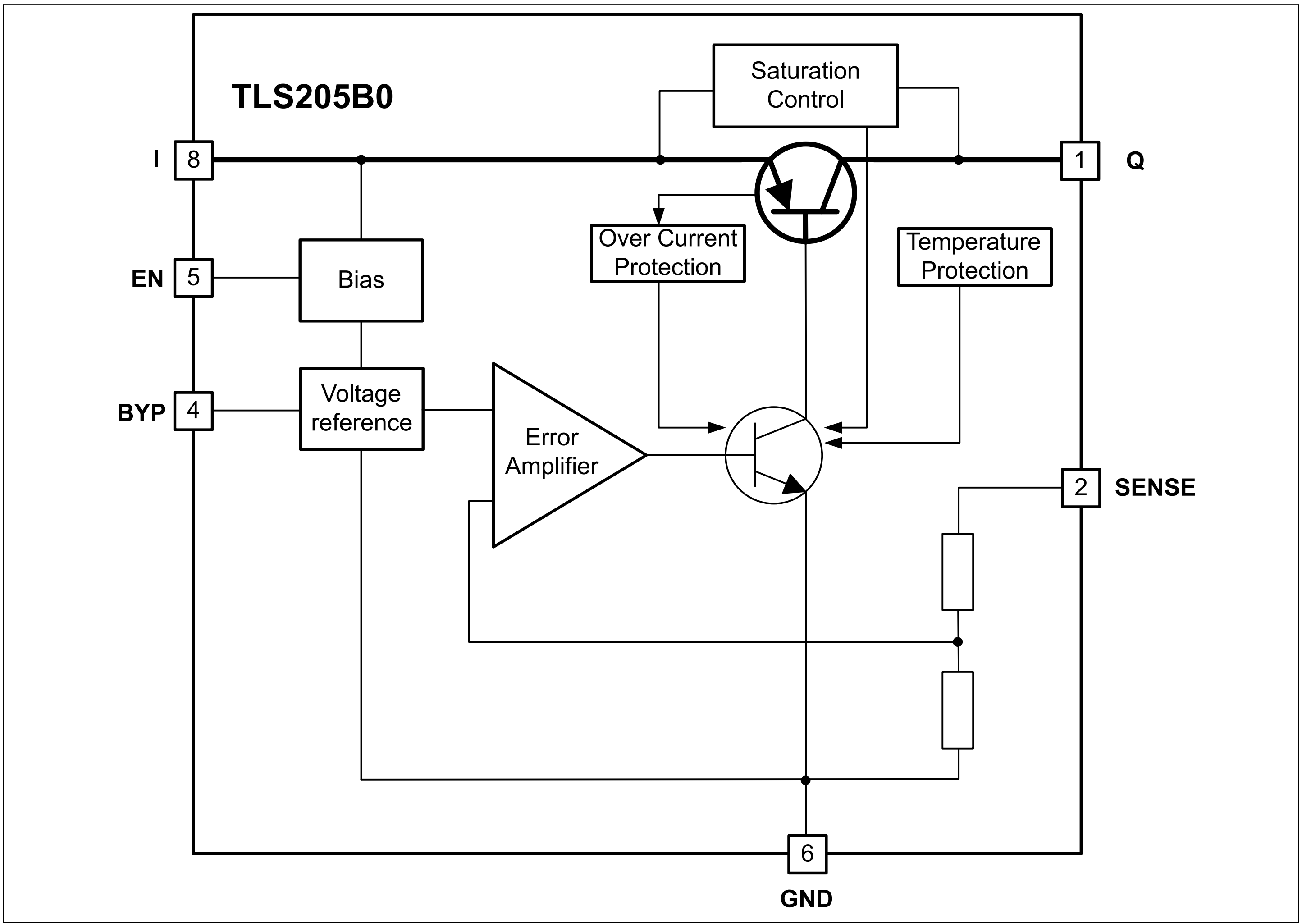


Figure 1 **Block diagram**

2 Pin configuration

2.1 Pin assignment

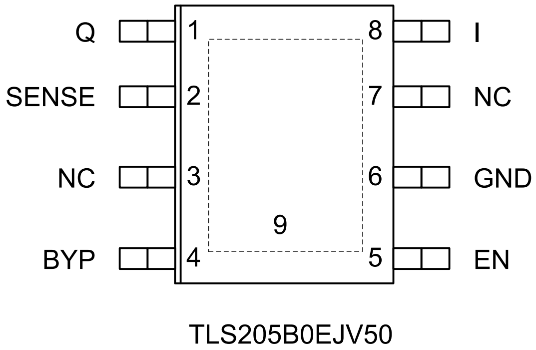


Figure 2 **Pin configuration PG-DSO-8 exposed pad**

2.2 Pin definitions and functions

Table 1 **Pin definitions and functions**

Pin	Symbol	Function
1	Q	**Output.** Supplies power to the load. For this pin, an output capacitor with capacitance of at least 3.3 µF is required to prevent oscillations. Larger output capacitors may be required for applications with large transient loads in order to limit peak voltage transients or when the regulator is applied in conjunction with a bypass capacitor. For more details, refer to Application information.
2	SENSE	**Output sense.** The SENSE pin is the input to the error amplifier. This allows an optimized regulation performance in case of small voltage drops R_p that occur between regulator and load. In applications where such drops are relevant, they can be eliminated by connecting the SENSE pin directly at the load. In standard configurations, the SENSE pin can be connected directly to Q. For further details, refer to the section Kelvin sense connection.
3, 7	NC	**Not connected.** The NC pin has no connection to any internal circuitry. Connect either to GND or leave open.
4	BYP	**Bypass.** The BYP pin is used to bypass the reference of the TLS205B0EJ V50 to achieve low noise performance. The BYP pin is clamped internally to ±0.6 V (that is, one V_{BE}). A small capacitor from the output Q to the BYP pin bypasses the reference to lower the output voltage noise. [1)] If not used, this pin must be left unconnected.
5	EN	**Enable.** Using the EN pin, the TLS205B0EJ V50 can be put into a low-power shutdown state. The output is off when the EN is pulled low. The EN pin can be driven either by 3.3 V or 5 V logic, or by open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate [2)] and the EN pin current.[3)] Note that if the EN pin is not used, it must be connected to V_I. It must not be left floating.
6	GND	**Ground.**

(table continues...)

Table 1 (continued) Pin definitions and functions

Pin	Symbol	Function
8	I	**Input.** The device is supplied by the input pin I. A capacitor at the input pin is required if the device is more than 15 centimeters away from the main input filter capacitor or if a non-negligible inductance is present at the input I. 4) The TLS205B0EJ V50 is designed to withstand reverse voltages on the input pin I with respect to GND and output Q. In case of reverse input (for example, due to an incorrectly attached battery), the device acts as if there were a diode in series with its input. In this way, no reverse current flows into the regulator and no reverse voltage appears at the load. Hence, the device will protect both itself and the load.
9	Tab	**Exposed pad.** To ensure proper thermal performance solder pin 9 (exposed-pad) to the PCB ground and tie directly to pin 6 (GND).

1) A maximum value of 10 nF can be used for reducing output voltage noise over the bandwidth from 10 Hz to 100 kHz.
2) Normally several microamperes.
3) Typical value is 1 µA.
4) In general, the output impedance of a battery rises with the frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. Depending on the specific conditions, an input capacitor in the range of 1 µF to 10 µF is usually sufficient.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage							
Voltage	V_I	-20	–	20	V	–	P_4.1.1
Output voltage							
Voltage	V_Q	-20	–	20	V	–	P_4.1.2
Input-to-output differential voltage	V_I - V_Q	-20	–	20	V	–	P_4.1.3
Sense pin							
Voltage	V_{SENSE}	-20	–	20	V	–	P_4.1.4
BYP pin							
Voltage	V_{BYP}	-0.6	–	0.6	V	–	P_4.1.5
Enable pin							
Voltage	V_{EN}	-20	–	20	V	–	P_4.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.7
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.8
ESD robustness							
ESD robustness all pins (HBM)	$V_{ESD,HBM}$	-2	–	2	kV	[2)]	P_4.1.9
ESD robustness all pins (CDM)	$V_{ESD,CDM}$	-1	–	1	kV	[3)]	P_4.1.10

1) Not subject to production testing, specified by design.
2) Human body model (HBM) robustness according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
3) Charged device model (CDM) robustness according to JEDEC JESD22-C101.

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered to be outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	5.5	–	20	V	–	P_4.2.1
Output capacitor requirements for stability	C_Q	3.3	–	–	µF	1) C_{BYP} = 0 nF	P_4.2.2
Output capacitor requirements for stability	C_Q	6.8	–	–	µF	1) 0 nF < C_{BYP} ≤ 10 nF	P_4.2.3
Output capacitor equivalent series resistance	*ESR*	–	–	3	Ω	1) 2)	P_4.2.4
Operating junction temperature	T_j	-40	–	125	°C	–	P_4.2.5

1) For further details, see the corresponding graph.
2) C_{BYP} = 0 nF, C_Q ≥ 3.3 µF. Note that for cases where a bypass capacitor is used at BYP, depending on the actual applied capacitance of C_Q and C_{BYP}, a minimum requirement for ESR of C_Q may apply.

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical characteristics table.*

3.3 Thermal resistance

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.*

Table 4 Thermal resistance [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	7	–	K/W	–	P_4.3.1
Junction to ambient	R_{thJA}	–	39	–	K/W	[2)] –	P_4.3.2
Junction to ambient	R_{thJA}	–	155	–	K/W	[3)] Footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	66	–	K/W	[3)] 300 mm^2 heatsink area on PCB	P_4.3.4
Junction to ambient	R_{thJA}	–	52	–	K/W	[3)] 600 mm^2 heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design.
2) The specified R_{thJA} value is defined according to JEDEC JESD51-2,-5,-7 with natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 x 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
3) The specified R_{thJA} value is defined according to JEDEC JESD 51-3 with natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with one copper layer (1 × 70 µm Cu).

4 Electrical characteristics

Table 5 Electrical characteristics

-40°C < T_j < 125°C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Minimum operating voltage							
Minimum operating voltage	$V_{I,min}$	–	1.8	2.3	V	1) I_Q = 500 mA	P_5.0.1
Output voltage							
Output voltage	V_Q	4.875	5.00	5.125	V	2) 1 mA < I_Q < 500 mA; 6 V < V_I < 20 V	P_5.0.2
Line regulation							
Line regulation	ΔV_Q	–	1	25	mV	ΔV_I = 5.5 V to 20 V; I_Q = 1 mA	P_5.0.3
Load regulation							
Load regulation	ΔV_Q	–	16	32	mV	T_j = 25°C; V_I = 6.0 V; ΔI_Q = 1 to 500 mA	P_5.0.4
Load regulation	ΔV_Q	–	–	57	mV	V_I = 6.0 V; ΔI_Q = 1 to 500 mA	P_5.0.5
Dropout voltage							
Dropout voltage	V_{DR}	–	130	190	mV	3) I_Q = 10 mA; V_I = $V_{Q,nom}$; T_j = 25°C	P_5.0.6
Dropout voltage	V_{DR}	–	–	250	mV	3) I_Q = 10 mA; V_I = $V_{Q,nom}$	P_5.0.7
Dropout voltage	V_{DR}	–	170	220	mV	3) I_Q = 50 mA; V_I = $V_{Q,nom}$; T_j = 25°C	P_5.0.8
Dropout voltage	V_{DR}	–	–	320	mV	3) I_Q = 50 mA; V_I = $V_{Q,nom}$	P_5.0.9
Dropout voltage	V_{DR}	–	200	240	mV	3) I_Q = 100 mA; V_I = $V_{Q,nom}$; T_j = 25°C	P_5.0.10
Dropout voltage	V_{DR}	–	–	340	mV	3) I_Q = 100 mA; V_I = $V_{Q,nom}$	P_5.0.11
Dropout voltage	V_{DR}	–	350	380	mV	3) I_Q = 500 mA; V_I = $V_{Q,nom}$; T_j = 25°C	P_5.0.12
Dropout voltage	V_{DR}	–	–	480	mV	3) I_Q = 500 mA; V_I = $V_{Q,nom}$	P_5.0.13
Quiescent current							
Quiescent current (active-mode, EN pin high)	I_q	–	30	60	µA	V_I = $V_{Q,nom}$; I_Q = 0 mA	P_5.0.14
Quiescent current (off-mode, EN pin low)	I_q	–	0.1	1	µA	V_I = 6 V; V_{EN} = 0 V; T_j = 25°C	P_5.0.15
GND pin current							
GND pin current	I_{GND}	–	50	100	µA	4) V_I = $V_{Q,nom}$; I_Q = 1 mA	P_5.0.16

(table continues...)

Table 5 (continued) Electrical characteristics

-40°C < T_j < 125°C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
GND pin current	I_{GND}	–	300	850	µA	[4] $V_I = V_{Q,nom}$; $I_Q = 50$ mA	P_5.0.17
GND pin current	I_{GND}	–	0.7	2.2	mA	[4] $V_I = V_{Q,nom}$; $I_Q = 100$ mA	P_5.0.18
GND pin current	I_{GND}	–	3	8	mA	[4] $V_I = V_{Q,nom}$; $I_Q = 250$ mA	P_5.0.19
GND pin current	I_{GND}	–	11	22	mA	[4] $V_I = V_{Q,nom}$; $I_Q = 500$ mA; $T_j \geq 25$°C	P_5.0.20
GND pin current	I_{GND}	–	11	31	mA	[4] $V_I = V_{Q,nom}$; $I_Q = 500$ mA; $T_j < 25$°C	P_5.0.21
Enable							
Enable threshold high	$V_{th,EN}$	–	0.8	2.0	V	V_Q from off to on	P_5.0.22
Enable threshold low	$V_{tl,EN}$	0.25	0.65	–	V	V_Q from on to off	P_5.0.23
EN pin current	I_{EN}	–	0.01	–	µA	[5] $V_{EN} = 0$ V; $T_j = 25$°C	P_5.0.24
EN pin current	I_{EN}	–	1	–	µA	[5] $V_{EN} = 20$ V; $T_j = 25$°C	P_5.0.25
Output voltage noise							
Output voltage noise	e_{no}	–	55	–	µV_{RMS}	[6] C_Q =10 µF; C_{BYP} =10 nF; $I_Q = 500$ mA; BW =10 Hz to 100 kHz	P_5.0.26
Output voltage noise	e_{no}	–	44	–	µV_{RMS}	[6] $C_Q = 10$ µF + 250 mΩ resistor in series; $C_{BYP} = 10$ nF; $I_Q = 500$ mA; BW = 10 Hz to 100 kHz	P_5.0.27
Output voltage noise	e_{no}	–	42	–	µV_{RMS}	[6] $C_Q = 22$ µF $C_{BYP} = 10$ nF; $I_Q = 500$ mA; BW =10 Hz to 100 kHz	P_5.0.28
Output voltage noise	e_{no}	–	42	–	µV_{RMS}	[6] $C_Q = 22$ µF +250 mΩ resistor in series; $C_{BYP} = 10$ nF; $I_Q = 500$ mA; BW =10 Hz to 100 kHz	P_5.0.29
Power supply ripple rejection [6]							

(table continues...)

Table 5 (continued) Electrical characteristics

-40°C < T_j < 125°C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power supply ripple rejection	$PSRR$	–	65	–	dB	[6] $V_I - V_Q = 1.5$ V (avg); $V_{ripple} = 0.5$ V_{pp}; $f_r = 120$ Hz; $I_Q = 500$ mA	P_5.0.30
Output current limitation							
Output current limit	$I_{Q,limit}$	520	–	–	mA	$V_I = 7$ V; $V_Q = 0$ V	P_5.0.31
Output current limit	$I_{Q,limit}$	520	–	–	mA	$V_I = V_{Q,nom} + 1$ V $\Delta V_Q = -0.1$ V	P_5.0.32
Input reverse leakage current							
Input reverse leakage	$I_{leak,rev}$	–	–	1	mA	$V_I = -20$ V; $V_Q = 0$ V	P_5.0.33
Reverse output current							
Reverse output current	$I_{Reverse}$	–	10	20	µA	[7] $V_Q = V_{Q,nom}$; $V_I < V_{Q,nom}$; $T_j = 25$°C	P_5.0.34

1) This parameter specifies the minimum input voltage for which the device requires to power up and provide the maximum nominal output current of 500 mA. Under this minimum input voltage condition the TLS205B0EJ V50 starts to be in tracking mode and the output voltage will typically be in the range of around 1 V while providing the 500 mA.

2) The operating conditions are limited by the maximum junction temperature. The regulated output voltage specification applies only in conditions where the maximum junction temperature is not exceeded. It does therefore not apply to all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current must be limited for thermal reasons. The same holds true when operating at maximum output current where the input voltage range must be limited for thermal reasons.

3) The dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to $V_I - V_{DR}$.

4) GND pin current is tested with $V_I = V_{Q,nom}$ and a current source load. This means that this parameter is tested while being in the dropout region. The GND pin current in most cases decreases slightly at higher input voltages. For details, see the corresponding typical performance graphs.

5) The EN pin current flows into the EN pin.

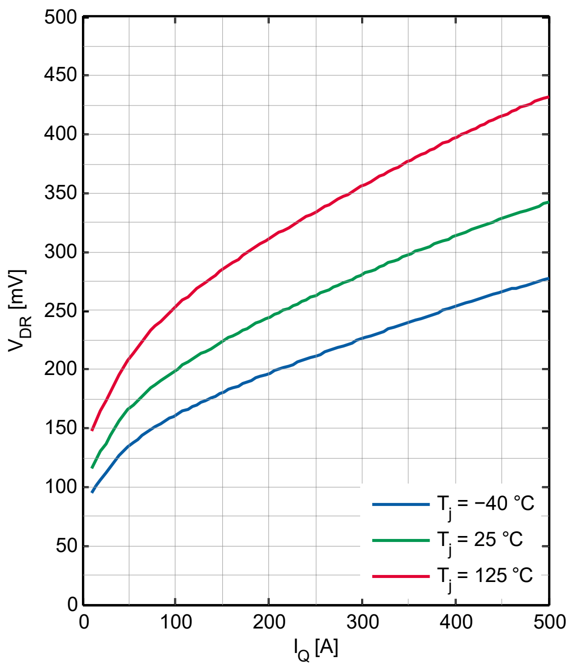
6) Not subject to production test, specified by design.

7) The reverse output current is tested with the I pin grounded and the Q pin forced to the rated output voltage. This current flows into the Q pin and out of the GND pin.

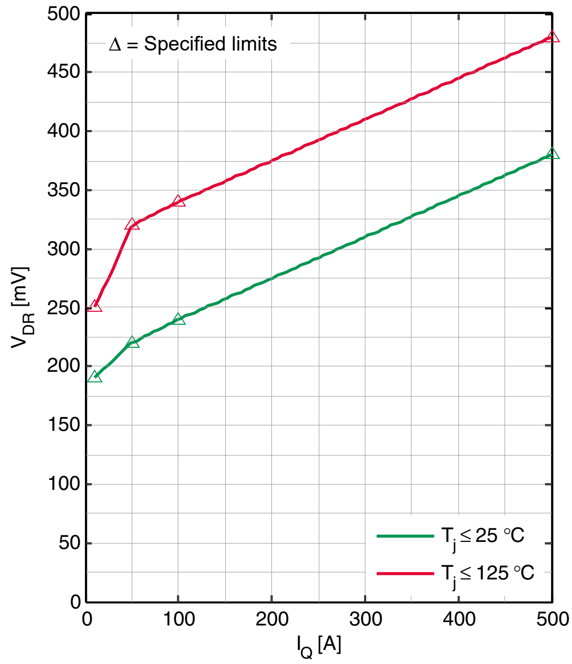
***Note**: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.*

4.1 Typical performance characteristics

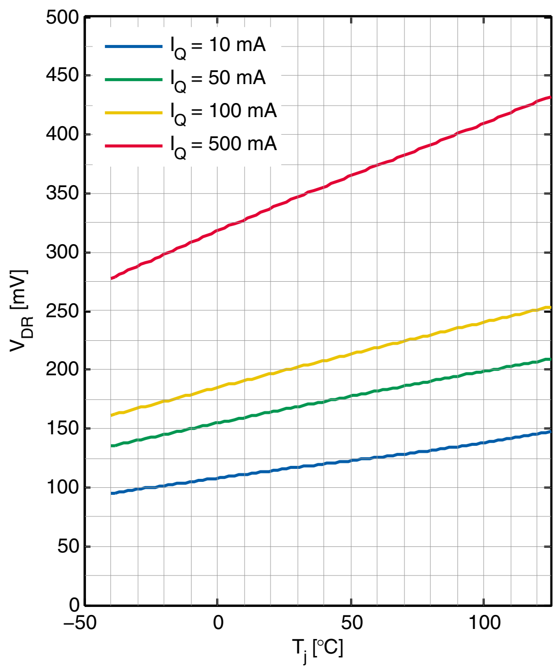
Dropout voltage V_{DR} versus output current I_Q



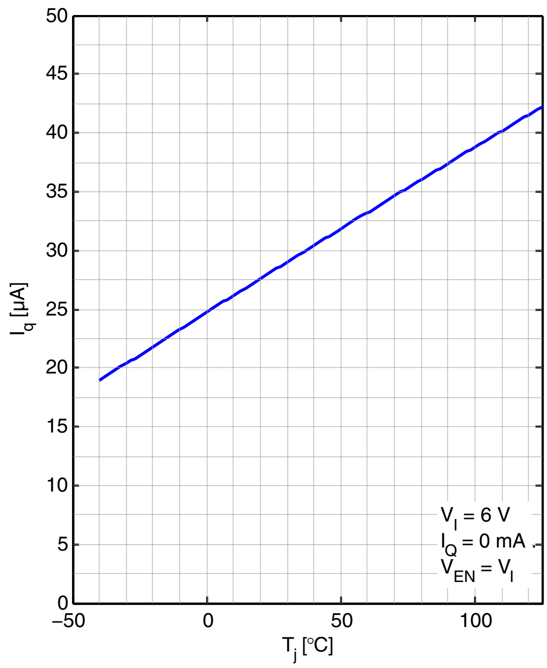
Specified dropout voltage V_{DR} versus output current I_Q



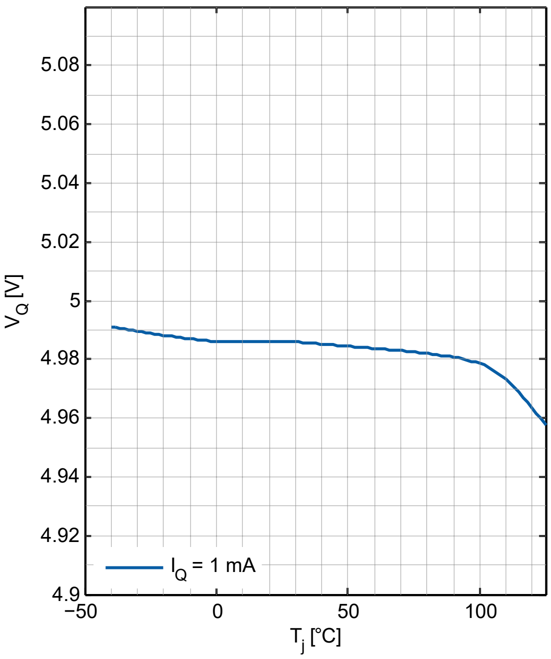
Dropout voltage V_{DR} versus junction temperature T_j



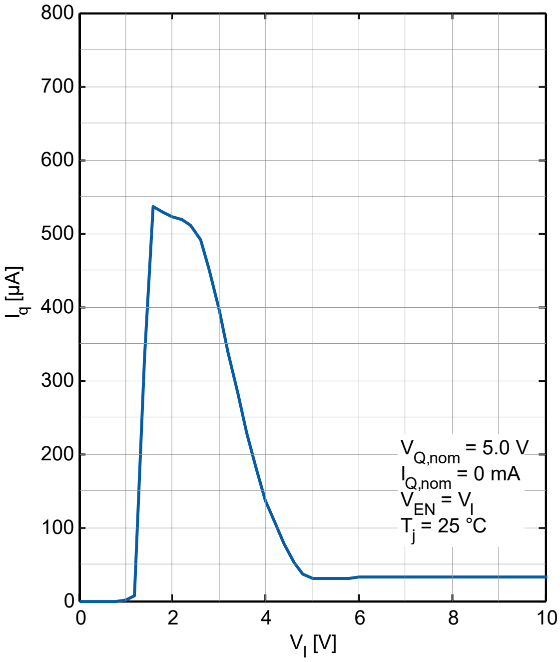
Quiescent current I_q versus junction temperature T_j



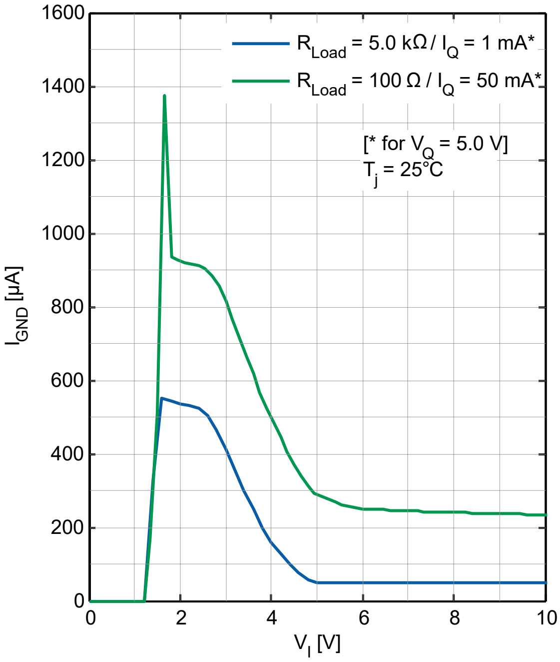
Output voltage V_Q versus junction temperature T_j



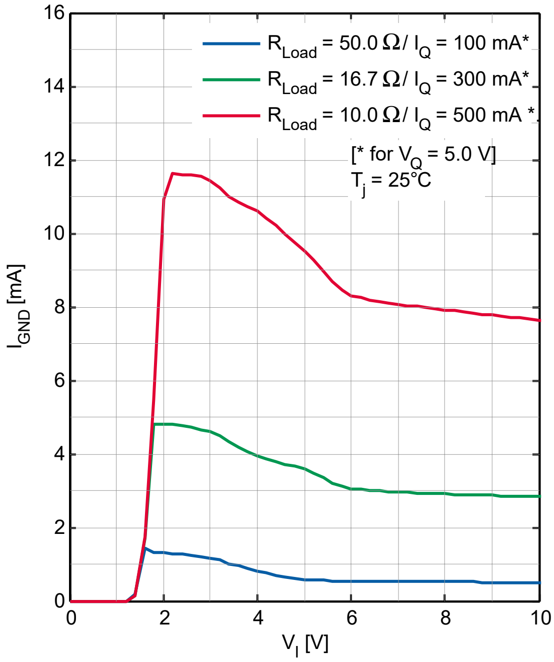
Quiescent current I_q versus input voltage V_I



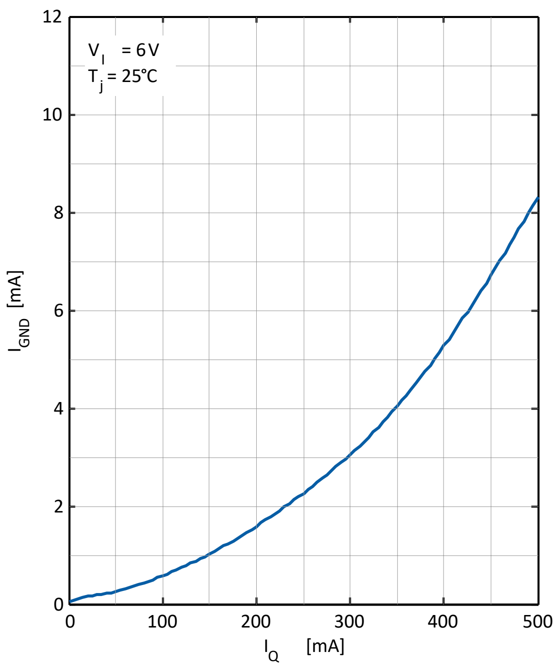
GND pin current I_{GND} versus input voltage V_I



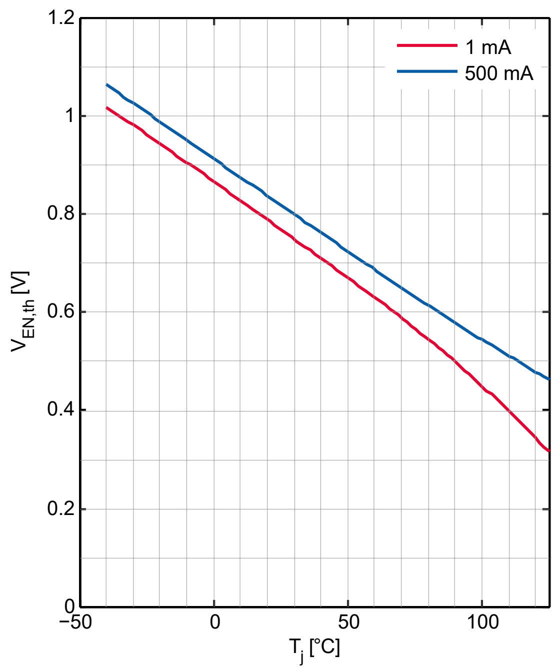
GND pin current I_{GND} versus input voltage V_I



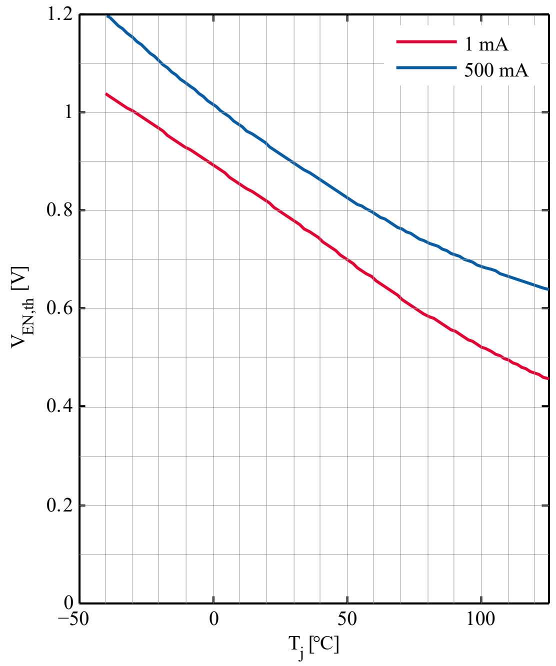
GND pin current I_{GND} versus output current I_Q



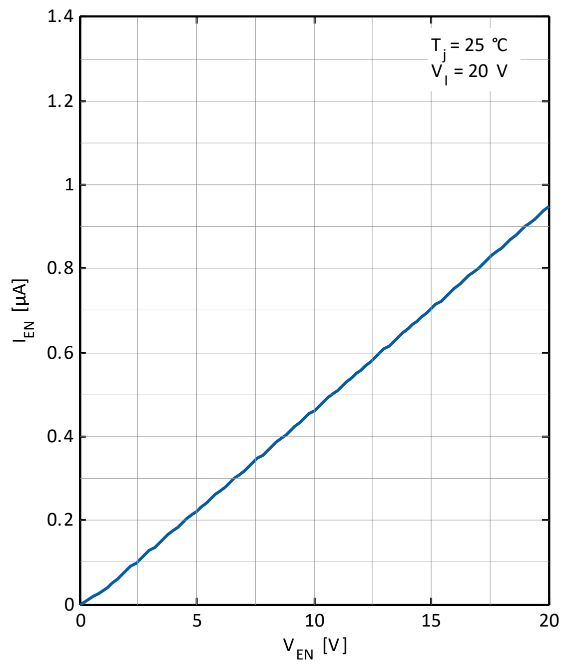
EN pin threshold $V_{tl,EN}$ (on to off) versus junction temperature T_j



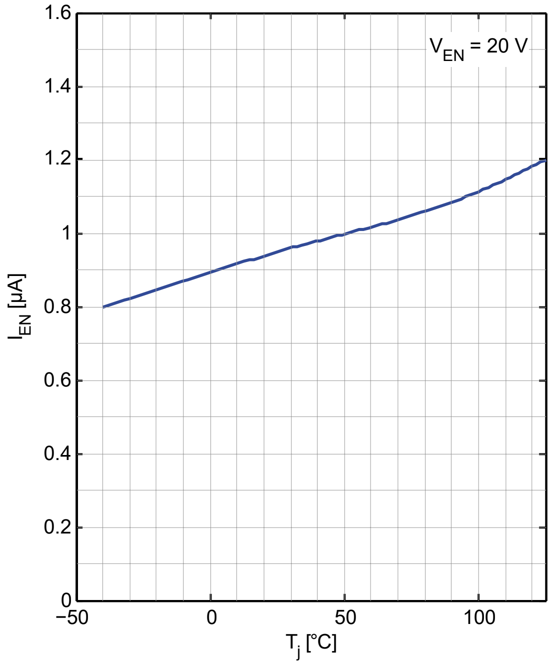
EN pin threshold $V_{th,EN}$ (off to on) versus junction temperature T_j



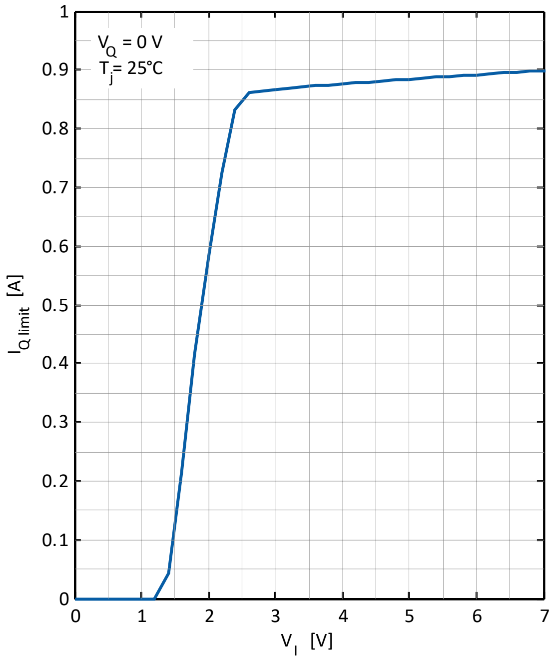
EN pin input current I_{EN} versus EN pin voltage V_{EN}



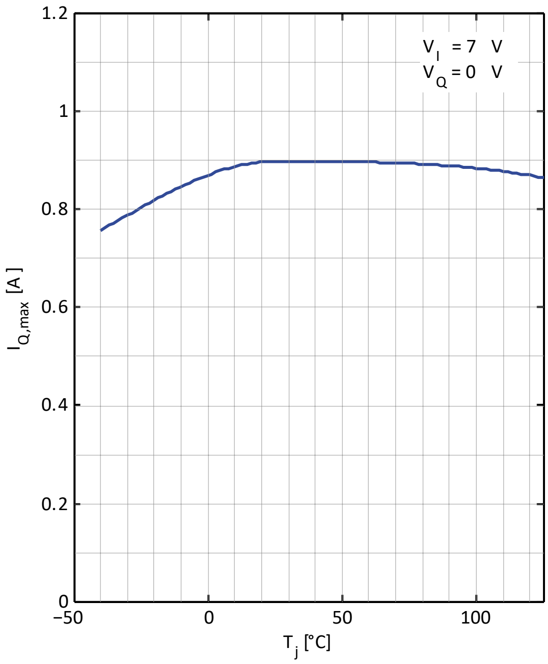
EN pin current I_{EN} versus junction temperature T_j



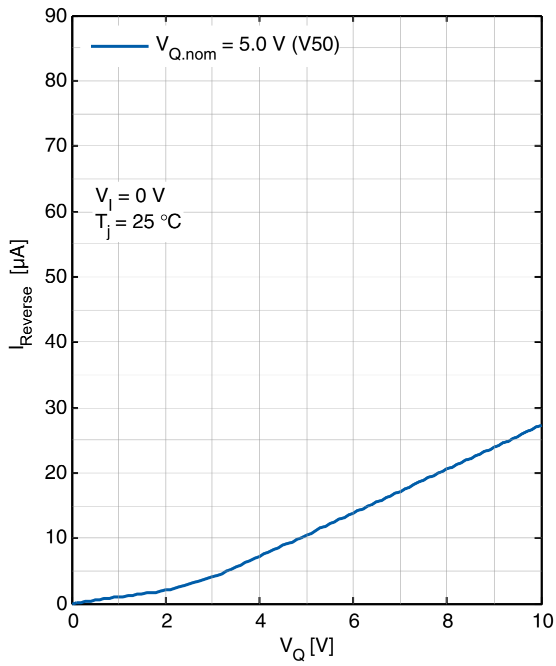
Current limit $I_{Q,limit}$ versus input voltage V_I



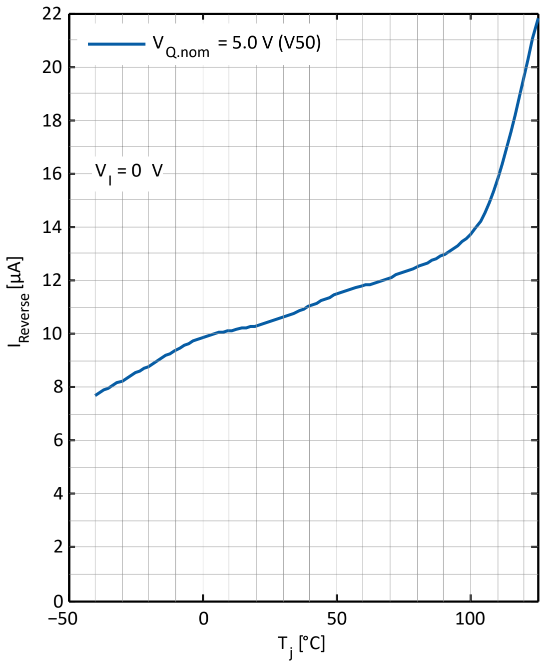
Current limit $I_{Q,limit}$ versus junction temperature T_j



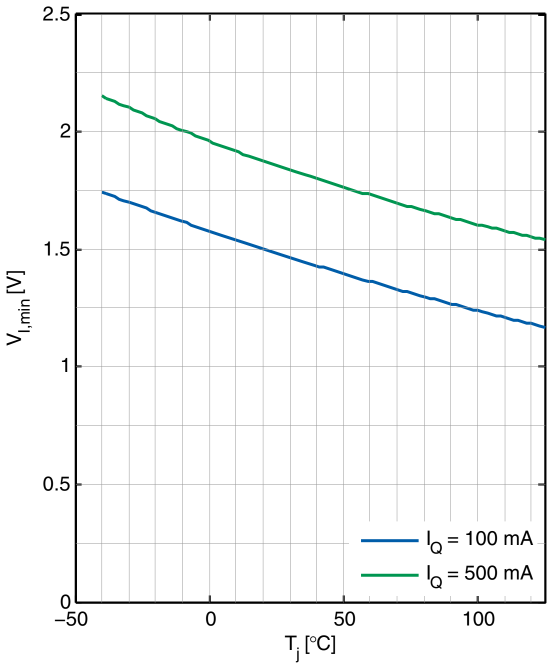
Reverse output current $I_{Reverse}$ versus output voltage V_Q



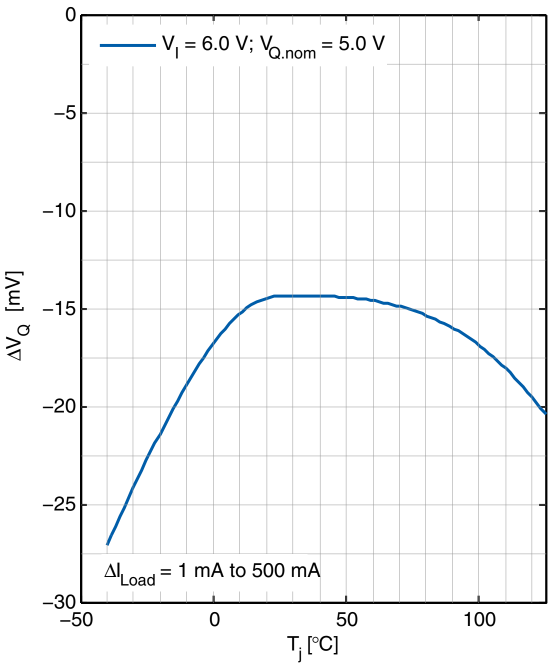
Reverse output current $I_{Reverse}$ versus junction temperature T_j



Minimum input voltage[1] $V_{I,min}$ versus junction temperature T_j

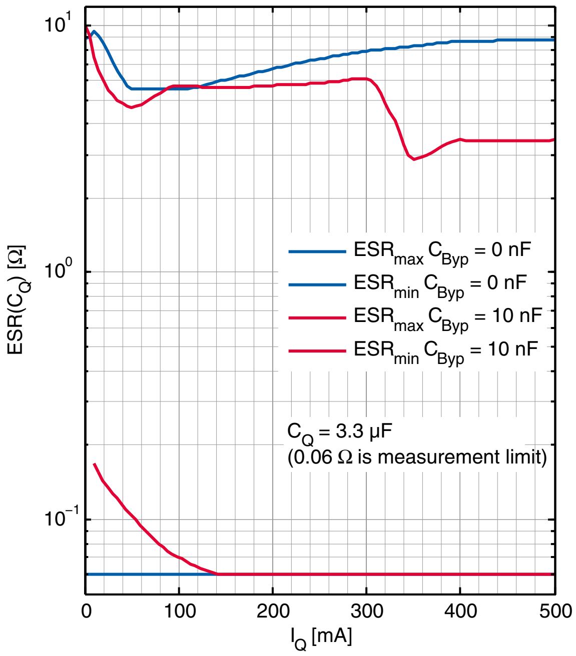


Load regulation ΔV_Q versus junction temperature T_j

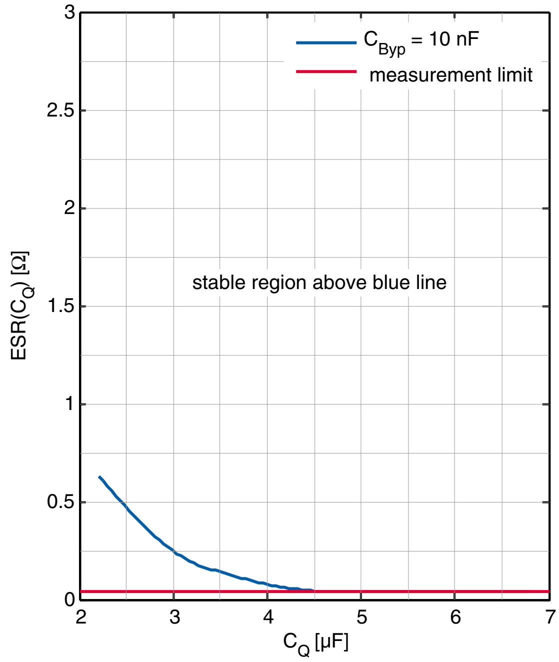


1) $V_{I,min}$ is referred here as the minimum input voltage for which the requested current is provided and V_Q reaches 1 V.

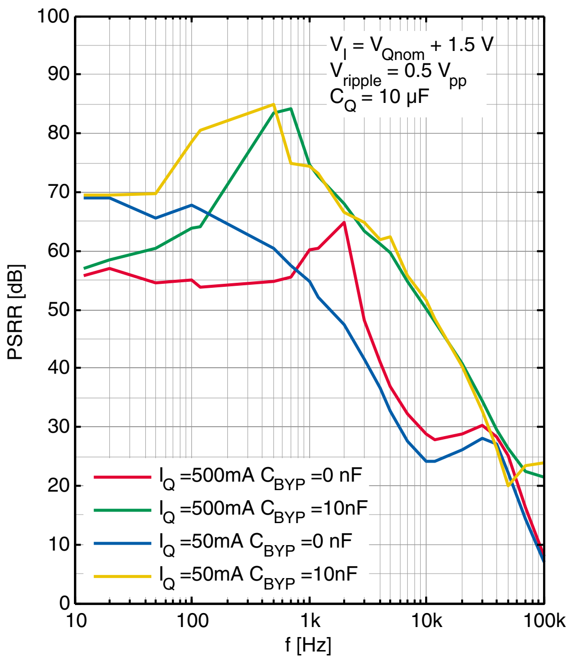
ESR stability versus output current I_Q (for C_Q = 3.3 µF)



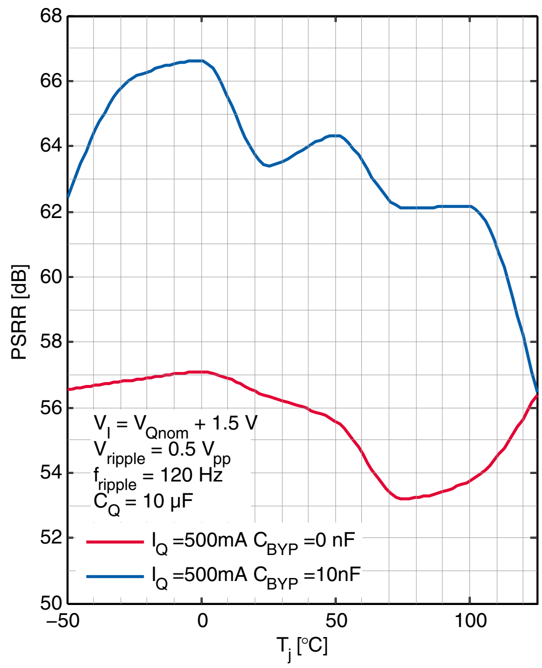
ESR(C_Q) with C_{BYP} = 10 nF versus output capacitance C_Q



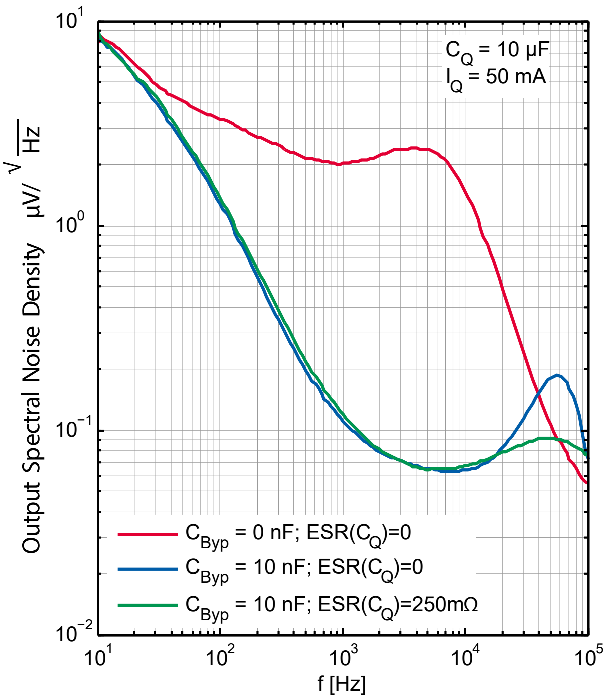
Power supply ripple rejection PSRR versus frequency f



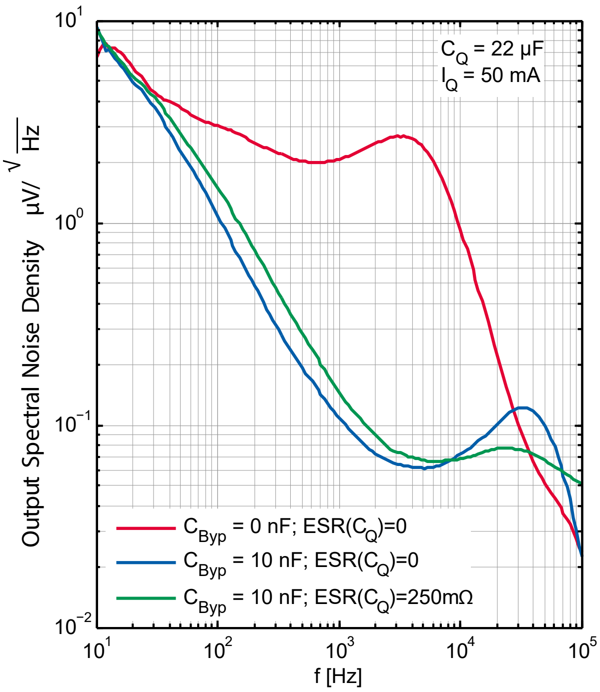
Power supply ripple rejection PSRR versus junction temperature T_j



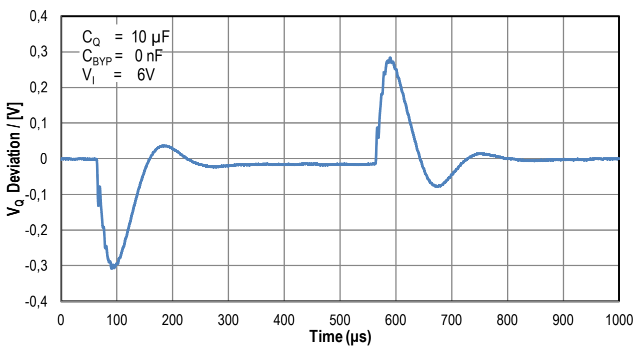
Output noise spectral density versus frequency f (C_Q = 10 µF, I_Q = 50 mA)

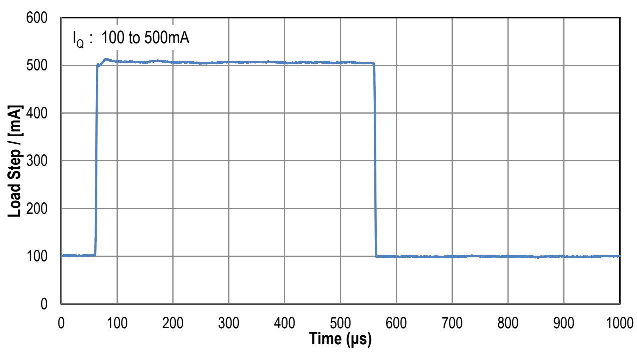


Output noise spectral density versus frequency f (C_Q = 22 µF, I_Q = 50 mA)

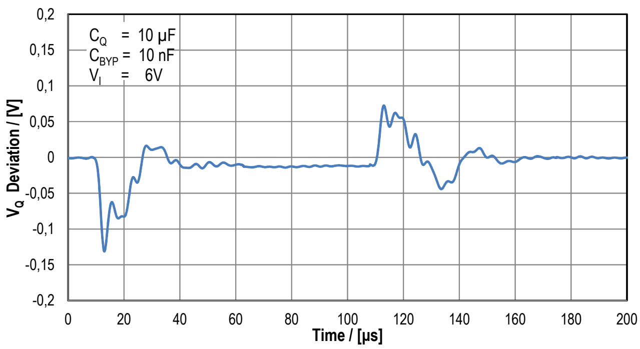


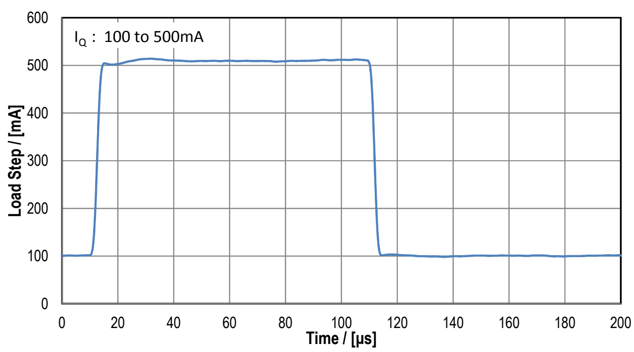
Transient response C_{BYP} = 0 nF





Transient response C_{BYP} = 10 nF





5 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

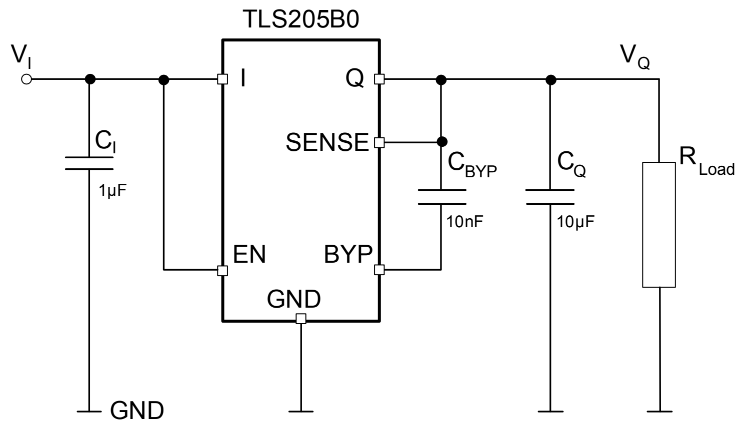


Figure 3 Typical application circuit

***Note**: This is a very simplified example of an application circuit. The functionality must be verified in the real application.*[1] [2]

The TLS205B0EJ V50 is a 500 mA low-dropout regulator with very low quiescent current and Enable-functionality. The device is capable of supplying 500 mA at a dropout voltage of 350 mV. Output voltages down to 42 μV_{RMS} can be achieved over a bandwidth from 10 Hz to 100 kHz with the addition of a 10 nF reference bypass capacitor. Using a reference bypass capacitor additionally improves the transient response of the regulator, lowering the settling time for transient load conditions. The device has a low operating quiescent current of typically 30 µA that drops to less than 1 µA in shutdown (EN pulled low). The device also incorporates several protection features which makes it ideal for battery-powered systems. It is protected against both reverse input and reverse output voltages.

5.1 Kelvin sense connection

The SENSE pin is the input to the error amplifier. Optimal regulation is obtained at the point where the SENSE pin is connected to the output pin Q of the regulator. In critical applications, however, small voltage drops may be caused by the resistance R_p of the PC traces and may lower the resulting voltage at the load. This effect may be eliminated by connecting the SENSE pin to the output as close as possible to the load (see Figure 4). Note that the voltage drop across the external PC trace will add to the dropout voltage of the regulator.

1 Note that when a non-negligible inductance is present at the input pin I, for example, due to long cables, traces, parasitics, etc, a bigger input capacitor C_I may be required to filter its influence. As a rule of thumb: If the I pin is more than 15 centimeter away from the main input filter capacitor, an input capacitor value of C_I = 10 µF is recommended.

2 For specific needs, a small optional resistor may be placed in series to very low ESR output capacitors C_Q for enhanced noise performance. (For details see Bypass capacitance and low noise performance.)

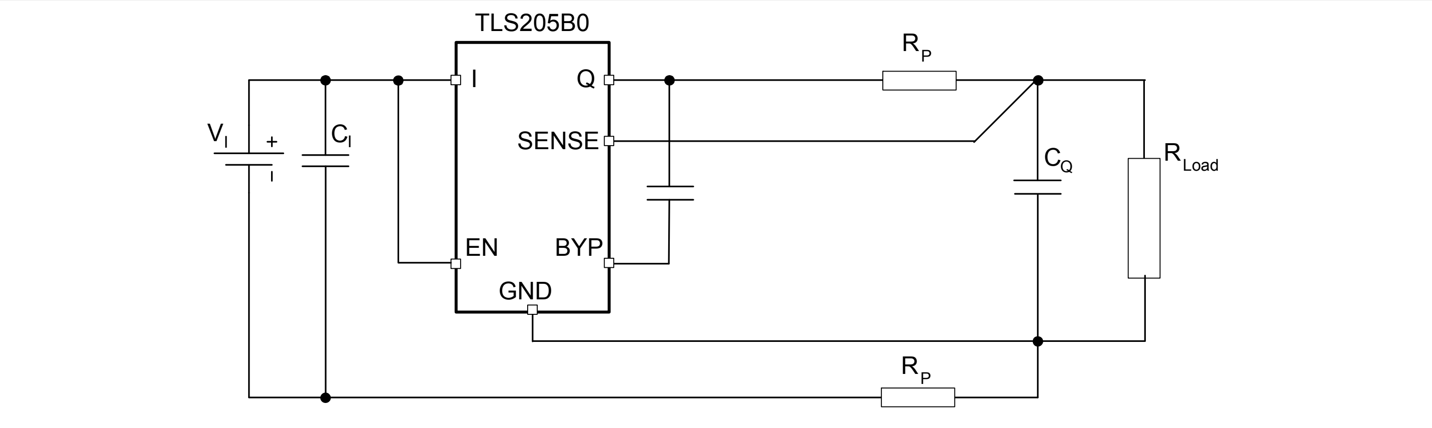


Figure 4 **Kelvin sense connection**

5.2 Bypass capacitance and low noise performance

The TLS205B0EJ V50 regulator can be used in combination with a bypass capacitor connecting the output pin Q to the BYP pin in order to minimize output voltage noise[3]. This capacitor bypasses the reference of the regulator, providing a low-frequency noise pole. The noise pole provided by such a bypass capacitor will lower the output voltage noise in the considered bandwidth. For a given output voltage, actual numbers of the output voltage noise of the

TLS205B0EJ V50 will - next to the bypass capacitor itself - be dependent on the capacitance of the applied output capacitor C_Q and its ESR.

In the case of using a bypass capacitor of 10 nF in combination with a (low-ESR) ceramic C_Q of 10 µF results in an output voltage noise number of typically 55 μV_{RMS}. This output noise level can be reduced to typically 44 μV_{RMS} under the same conditions by adding a small resistor in the range of ~250 mΩ in series to the 10 µF ceramic output capacitor, thus acting as additional ESR. A reduction of the output voltage noise can also be achieved by increasing the capacitance of the output capacitor. For C_Q = 22 µF (ceramic low-ESR), the output voltage noise will typically be around 42 μV_{RMS}.

For output capacitor values of 22 µF or bigger, adding resistance in series to C_Q does not further lower output noise numbers significantly anymore.

For further details see Output voltage noise in electrical characteristics. Note that next to reducing the output voltage noise level, the usage of a bypass capacitor has the additional benefit of improving transient response, further explained in Chapter 5.3. However, one needs to take into consideration that the regulator start-up time is proportional to the size of the bypass capacitor and slows down to values around 15 ms when using a 10 nF bypass capacitor in combination with a 10 µF output capacitor C_Q.

5.3 Output capacitance and transient response

The TLS205B0EJ V50 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor is an essential parameter with regard to stability, most notably with small capacitors. A minimum output capacitor of 3.3 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. As is typical for LDOs, the output transient response of the TLS205B0EJ V50 is a function of the output capacitance. Larger output capacitances decrease peak deviations and thus improve transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TLS205B0EJ V50, increase the effective output capacitor value. Note that, when using bypass capacitors for low-noise operation, either larger values of output capacitors may be needed or a minimum ESR requirement of C_Q may have to be considered, shown by the graph, ESR(C_Q) with C_{BYP} = 10 nF versus output capacitance C_Q as an example.

In conjunction with a 10 nF bypass capacitor, an output capacitor C_Q of at least 6.8 µF is recommended. The benefit of a bypass capacitor C_{BYP} to the transient response performance is impressive and illustrated as an example in Figure 5. The transient response of the TLS205B0EJ V50 to the same load step from 100 mA to 500 mA is shown with and without a 10 nF bypass capacitor C_{BYP} . For the given configuration of C_Q = 10 µF with no bypass capacitor, the load

3 A good -quality low-leakage capacitor is recommended.

step settles in the range of less than 200 µs, while for C_Q = 10 µF in conjunction with a 10 nF bypass capacitor the same load step settles in the range of 20 µs. Due to the shorter reaction time of the regulator obtained by adding the bypass capacitor, not only does the settling time improve but also output voltage deviations caused by load steps are sharply reduced.

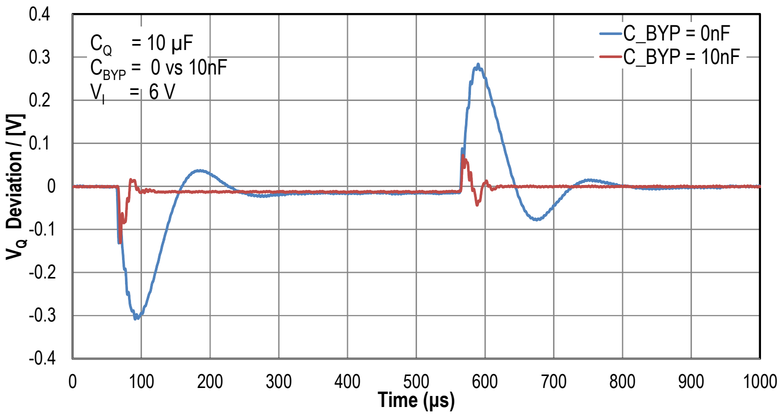


Figure 5 **Influence of C_{BYP}: Example of transient response to the same load step with and without C_{BYP} of 10 nF (I_Q: 100 mA to 500 mA)**

5.4 Protection features

The OPTIREG™ linear TLS205B0EJ regulator family incorporates several protection features which makes it ideal for use in battery-powered circuits. In addition to normal protection features associated with monolithic regulators like current-limiting and thermal-limiting, these devices are protected against reverse input voltage, reverse output voltage, and reverse voltages from output to input.

Current-limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature must not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flowing into the device is limited to less than 1 mA (typically less than 100 µA) and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries being plugged backwards.

The output of the TLS205B0EJ V50 can be pulled below ground without damaging the device. If the input is left open-circuit or grounded, the output can be pulled below ground by 20 V. Under such conditions, the output of the device by itself behaves like an open circuit with practically no current flowing out of the pin. [4)]

In more application-relevant cases, however, where the output is connected to the SENSE pin a small current of typically less than 100 µA will be present from this origin.

If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case grounding the EN pin will turn the device off and stop the output from sourcing the short-circuit current.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open-circuit. Current flow back into the output follows the curve as shown in Figure 6 below.

4 Typically < 1 µA for the mentioned conditions, V_Q being pulled below ground with other pins either grounded or open.

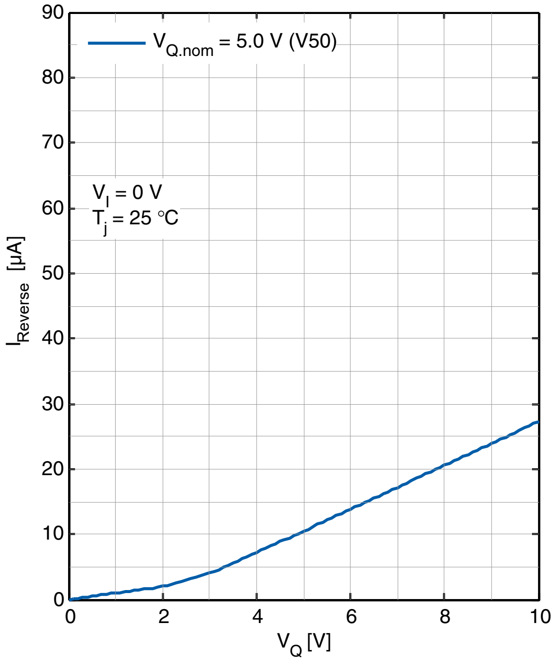


Figure 6 **Reverse output current**

6 Package information

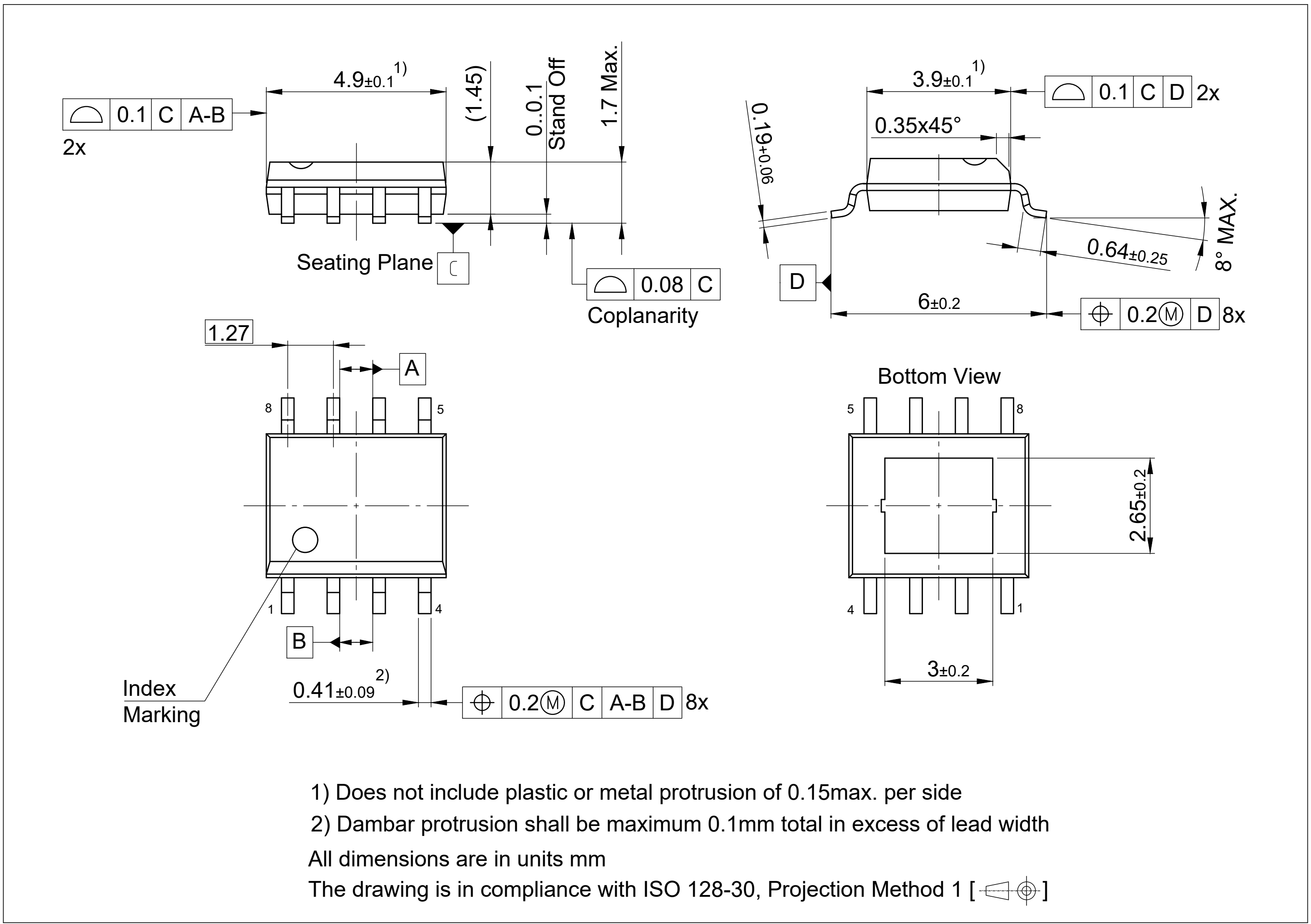


Figure 7 **PG-DSO-8 exposed pad**

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

Revision history

Document version	Date of release	Description of changes
1.20	2025-02-13	PG-TSON-10 package variant removed. Editorial changes. Updated template and layout
1.10	2015-01-12	PG-TSON-10 package variant added: product overview, pin configuration, thermal resistance, etc. -wording and description added or updated accordingly. Editorial changes
1.00	2014-06-30	Datasheet - Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-02-13

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-mww1731058384267
Z8F53142152