DATA SHEET

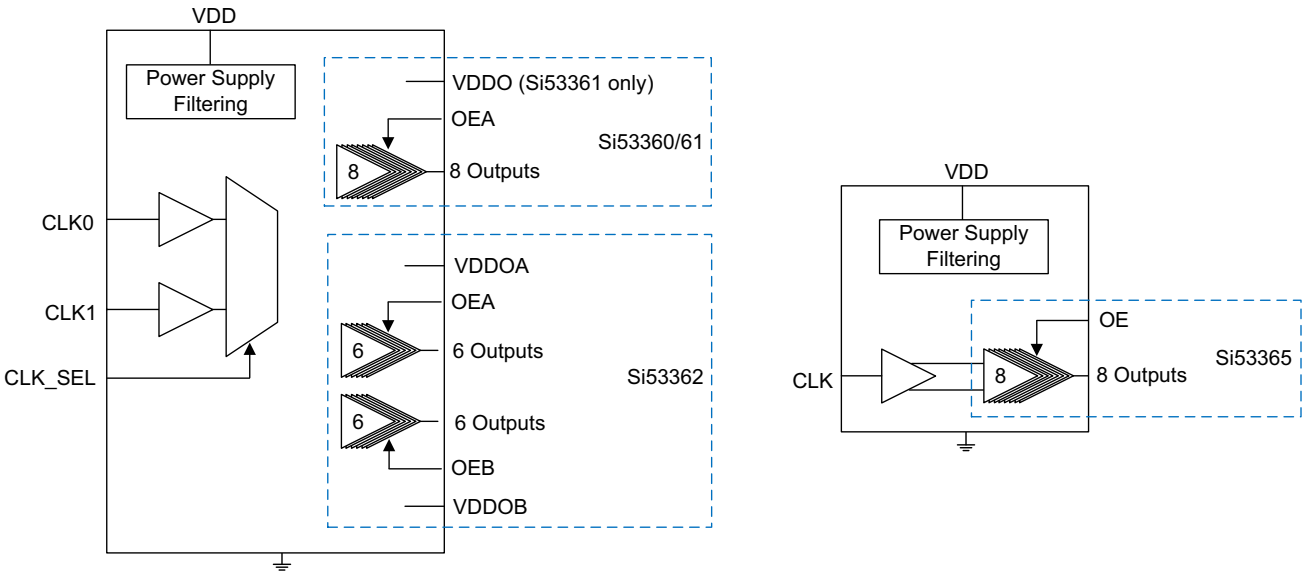
Si5336x Low-Jitter, LVCMOS Fanout Clock Buffers with up to 12 Outputs and Frequency Range from DC to 200 MHz

The Si53360/61/62/65 family of LVCMOS fanout buffers is ideal for clock/data distribution and redundant clocking applications. This device family utilizes Skyworks advanced CMOS technology for fanout clocks from dc to 200 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. Built-in LDOs deliver high PSRR performance, eliminating the need for external components and simplifying low-jitter clock distribution in noisy environments.

The CMOS buffers are available in multiple configurations with eight outputs (Si53360/61/65) or dual banks of six outputs each (Si53362). These buffers can be paired with Skyworks oscillators, clock generators, jitter attenuators, and network synchronizers to deliver end-to-end clock tree performance.

Key Features

- Low additive jitter: 120 fs_{RMS}.
- Built-in LDOs for high PSRR performance.
- Up to 12 LVCMOS outputs from LVCMOS inputs.
- Frequency range: dc to 200 MHz.
- Multiple configuration options:
  - Dual-bank option.
  - 2:1 Input MUX option.
- Temperature range: –40 to +85 °C.
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.



1. Pin Descriptions

1.1. Si53360 Pin Descriptions

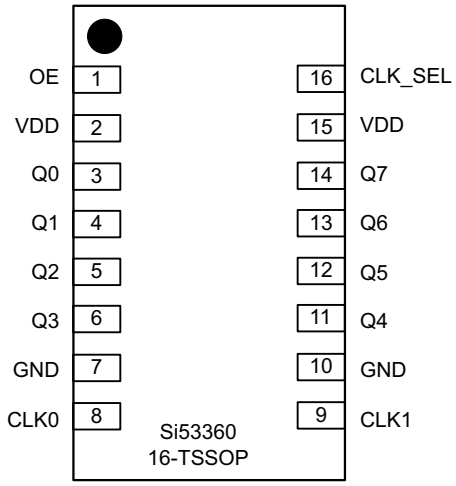


Figure 1. Si53360 16-TSSOP Pinout

Table 1. Si53360 16-TSSOP Pin Descriptions

Pin	Name	Type[1]	Description
1	OE	I	Output enable. When OE = high, the clock outputs are enabled. When OE = low, the clock outputs are tri-stated. OE features an internal pull-up resistor and may be left unconnected.
2	VDD	P	Core and output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
3	Q0	O	Output Clock 0.
4	Q1	O	Output Clock 1.
5	Q2	O	Output Clock 2.
6	Q3	O	Output Clock 3.
7	GND	GND	Ground.
8	CLK0	I	Input Clock 0.
9	CLK1	I	Input Clock 1.
10	GND	GND	Ground.
11	Q4	O	Output Clock 4.
12	Q5	O	Output Clock 5.
13	Q6	O	Output Clock 6.
14	Q7	O	Output Clock 7.
15	VDD	P	Core and output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
16	CLK_SEL	I	MUX input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor.

1. I = Input; O = Output; P = Power; GND = Ground.

1.2. Si53361 Pin Descriptions

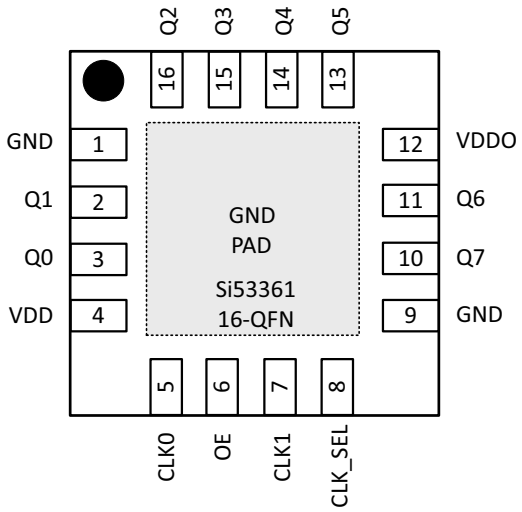


Figure 2. Si53361 16-QFN Pinout

Table 2. Si53361 16-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	GND	GND	Ground.
2	Q1	O	Output Clock 1.
3	Q0	O	Output Clock 0.
4	VDD	P	Core voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDD pin as possible.
5	CLK0	I	Input Clock 0.
6	OE	I	Output enable. When OE = high, the clock outputs are enabled. When OE = low, the clock outputs are tri-stated. OE features an internal pull-up resistor and may be left unconnected.
7	CLK1	I	Input Clock 1.
8	CLK_SEL	I	MUX input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor.
9	GND	GND	Ground.
10	Q7	O	Output Clock 7.
11	Q6	O	Output Clock 6.
12	VDDO	P	Output voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDDO pin as possible.
13	Q5	O	Output Clock 5.
14	Q4	O	Output Clock 4.
15	Q3	O	Output Clock 3.

Table 2. Si53361 16-QFN Pin Descriptions (Continued)

Pin	Name	Type[1]	Description
16	Q2	O	Output Clock 2.
GND pad	Exposed ground pad	GND	Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

1. I = Input; O = Output; P = Power; GND = Ground.

1.3. Si53362 Pin Descriptions

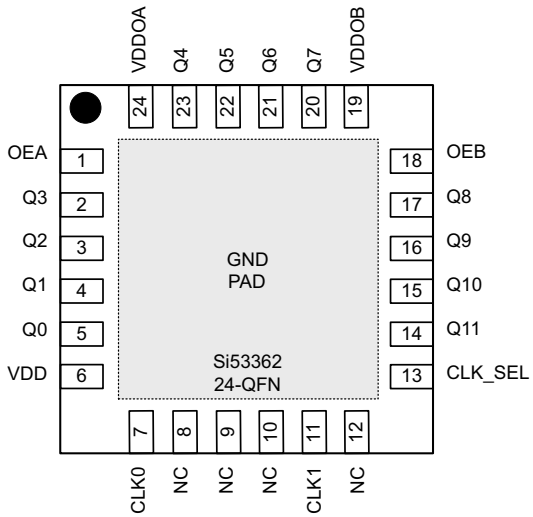


Figure 3. Si53362 24-QFN Pinout

Table 3. Si53362 24-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	OEA	I	Output enable for Bank A (Q0–Q5). When OEA = HIGH, outputs Q0–Q5 are enabled. This pin contains an internal pull-up resistor, and leaving the pin disconnected enables the outputs. When OEA = LOW, Q0–Q5 are tri-stated.
2	Q3	O	Output Clock 3.
3	Q2	O	Output Clock 2.
4	Q1	O	Output Clock 1.
5	Q0	O	Output Clock 0.
6	VDD	P	Core voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDD pin as possible.
7	CLK0	I	Input Clock 0.
8	NC	—	No connect. Leave this pin unconnected.
9	NC	—	No connect. Leave this pin unconnected.
10	NC	—	No connect. Leave this pin unconnected.
11	CLK1	I	Input Clock 1.
12	NC	—	No connect. Leave this pin unconnected.
13	CLK_SEL	I	MUX input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor.
14	Q11	O	Output Clock 11.

Table 3. Si53362 24-QFN Pin Descriptions (Continued)

Pin	Name	Type[1]	Description
15	Q10	O	Output Clock 10.
16	Q9	O	Output Clock 9.
17	Q8	O	Output Clock 8.
18	OEB	I	Output enable for bank B (Q6–Q11). When OEB = HIGH, outputs Q6–Q11 are enabled. This pin contains an internal pull-up resistor, and leaving the pin disconnected enables the outputs. When OEB = LOW, Q6–Q11 are tri-stated.
19	VDDOB	P	Output voltage supply—Bank B (Outputs: Q6 to Q11). Bypass with 1.0 µF capacitor, and place as close to the VDDOB pin as possible.
20	Q7	O	Output Clock 7.
21	Q6	O	Output Clock 6.
22	Q5	O	Output Clock 5.
23	Q4	O	Output Clock 4.
24	VDDOA	P	Output voltage supply—Bank A (Outputs: Q0 to Q5). Bypass with 1.0 µF capacitor, and place as close to the VDDOA pin as possible.
GND pad	Exposed ground pad	GND	Ground Pad—Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

1. I = Input; O = Output; P = Power; GND = Ground.

1.4. Si53365 Pin Descriptions

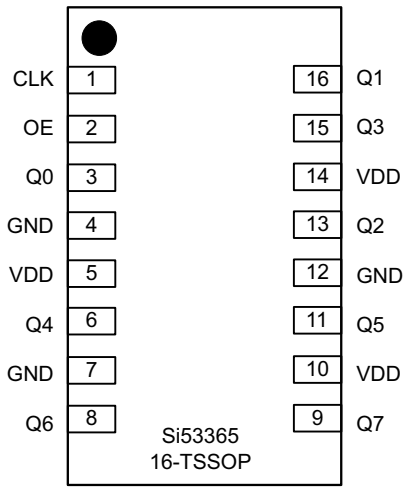


Figure 4. Si53365 16-TSSOP Pinout

Table 4. Si53365 16-TSSOP Pin Descriptions

Pin	Name	Type[1]	Description
1	CLK	I	Input clock.
2	OE	I	Output enable. When OE = high, the clock outputs are enabled. When OE = low, the clock outputs are low. OE features an internal pull-up resistor and may be left unconnected.
3	Q0	O	Output Clock 0.
4	GND	GND	Ground.
5	VDD	P	Core and output voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDD pin as possible.
6	Q4	O	Output Clock 4.
7	GND	GND	Ground.
8	Q6	O	Output Clock 6.
9	Q7	O	Output Clock 7.
10	VDD	P	Core and output voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDD pin as possible.
11	Q5	O	Output Clock 5.
12	GND	GND	Ground.
13	Q2	O	Output Clock 2.
14	VDD	P	Core and output voltage supply. Bypass with 1.0 µF capacitor, and place as close to the VDD pin as possible.
15	Q3	O	Output Clock 3.
16	Q1	O	Output Clock 1.

1. I = Input; O = Output; P = Power; GND = Ground.

2. Functional Description

The Si53360/61/62/65 are a family of low-jitter, low-skew, fixed-format (LVMCOS) buffers. These devices are available in multiple configurations customized for end applications (refer to “8. Ordering Guide” on page 29 for more details on configurations).

2.1. LVCMOS Input Termination

Table 5 summarizes the various ac- and dc-coupling options supported by the LVCMOS device, and the figure shows the recommended input clock termination.

Table 5. LVCMOS Input Clock Options

	LVCMOS	
V_{DD} Voltage	AC-Coupled	DC-Coupled
1.8 V	No	Yes
2.5/3.3 V	Yes	Yes

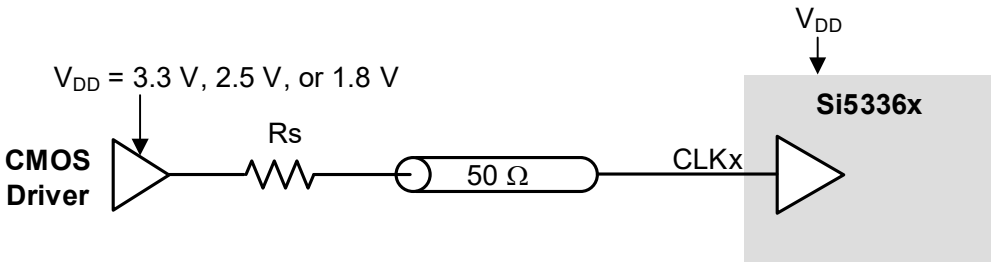


Figure 5. Recommended Input Clock Termination

Note: Value for Rs should be chosen so that the total source impedance matches the characteristic impedance of the PCB trace.

2.2. Input MUX

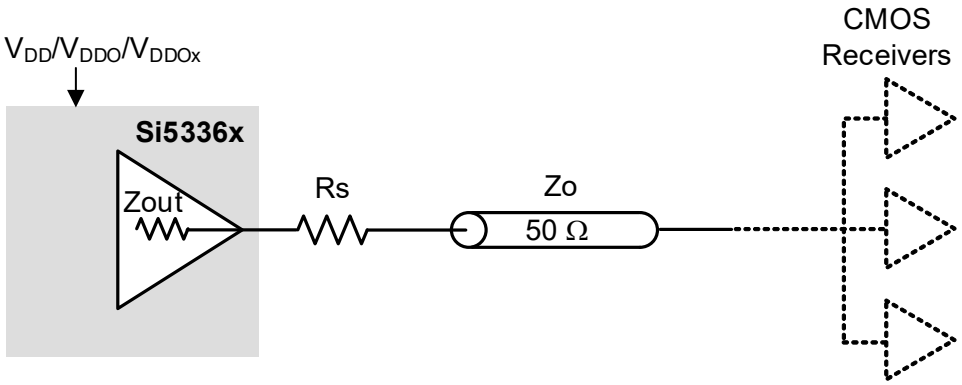
The Si53360/61/62 provide two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. Table 6 summarizes the input and output clock based on the input MUX settings.

Table 6. Input MUX Logic

CLK_SEL	CLK0	CLK1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

2.3. Output Clock Termination Options

The recommended output clock termination options are shown in Figure 6. Unused outputs should be left unconnected.



Note:
Rs = 33 Ω for 3.3 V and 2.5 V operation.
Rs = 0 Ω for 1.8 V operation.

Figure 6. LVCMOS Output Termination

2.4. AC Timing Waveforms

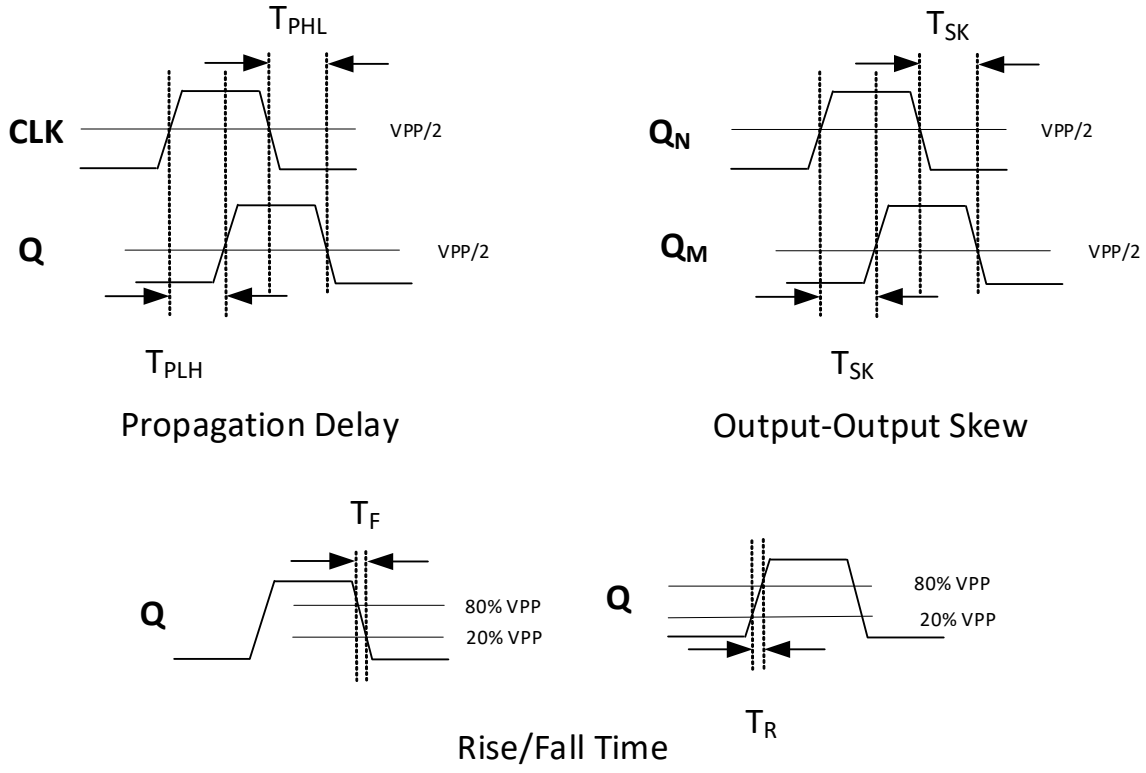


Figure 7. AC Timing Waveforms

2.5. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject power supply noise and simplify low-jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. See AN491: Power Supply Rejection for Low-Jitter Clocks for more information.

2.6. Typical Phase Noise Performance: Single-Ended Input Clock

Each of the phase noise plots superimposes Source Jitter and Total Jitter on the same diagram.

- **Source Jitter**—Reference clock phase noise (measured Single-ended to PNA).
- **Total Jitter**—Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. See "3. Electrical Specifications" on page 13 for more information.

Note: To calculate the additive RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS) method.

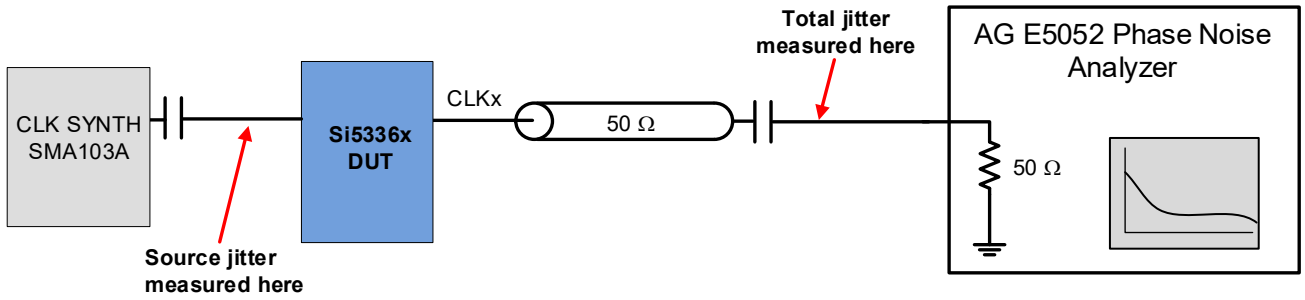


Figure 8. Single-Ended Measurement Method

Figure 9 shows two phase noise plots superimposed on the same diagram. Table 7 lists the slew rate and jitter data.

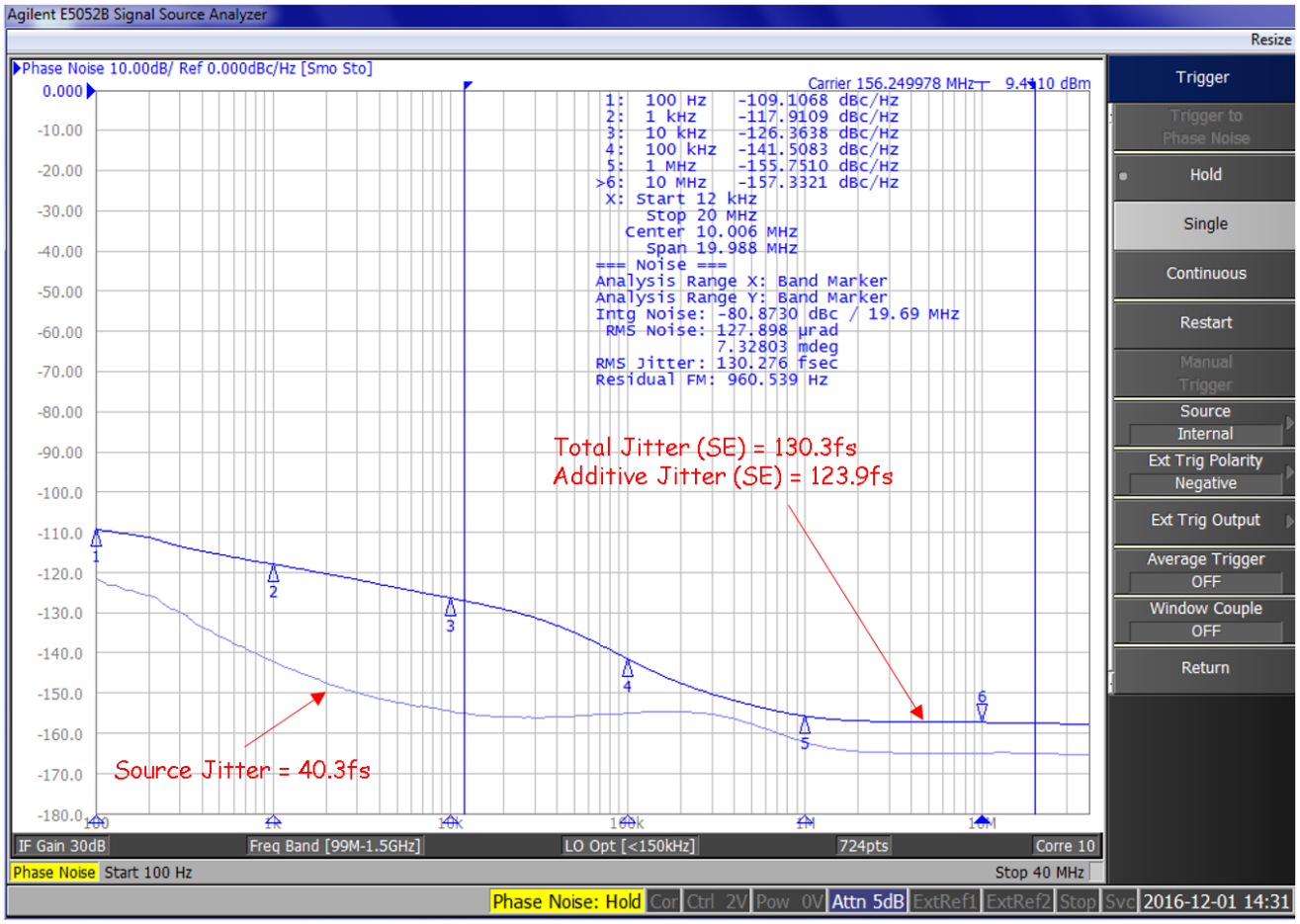


Figure 9. Total Jitter Single-Ended Input (156.25 MHz)

Table 7. Total Jitter Single-Ended Input (156.25 MHz)

Frequency (MHz)	Single-Ended Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)
156.25	1.0	40.3	130.28	123.89

2.7. Input MUX Noise Isolation

The input clock MUX is designed to minimize crosstalk between the CLK0 and CLK1 inputs. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. Figure 10 shows measurements of input MUX noise isolation.

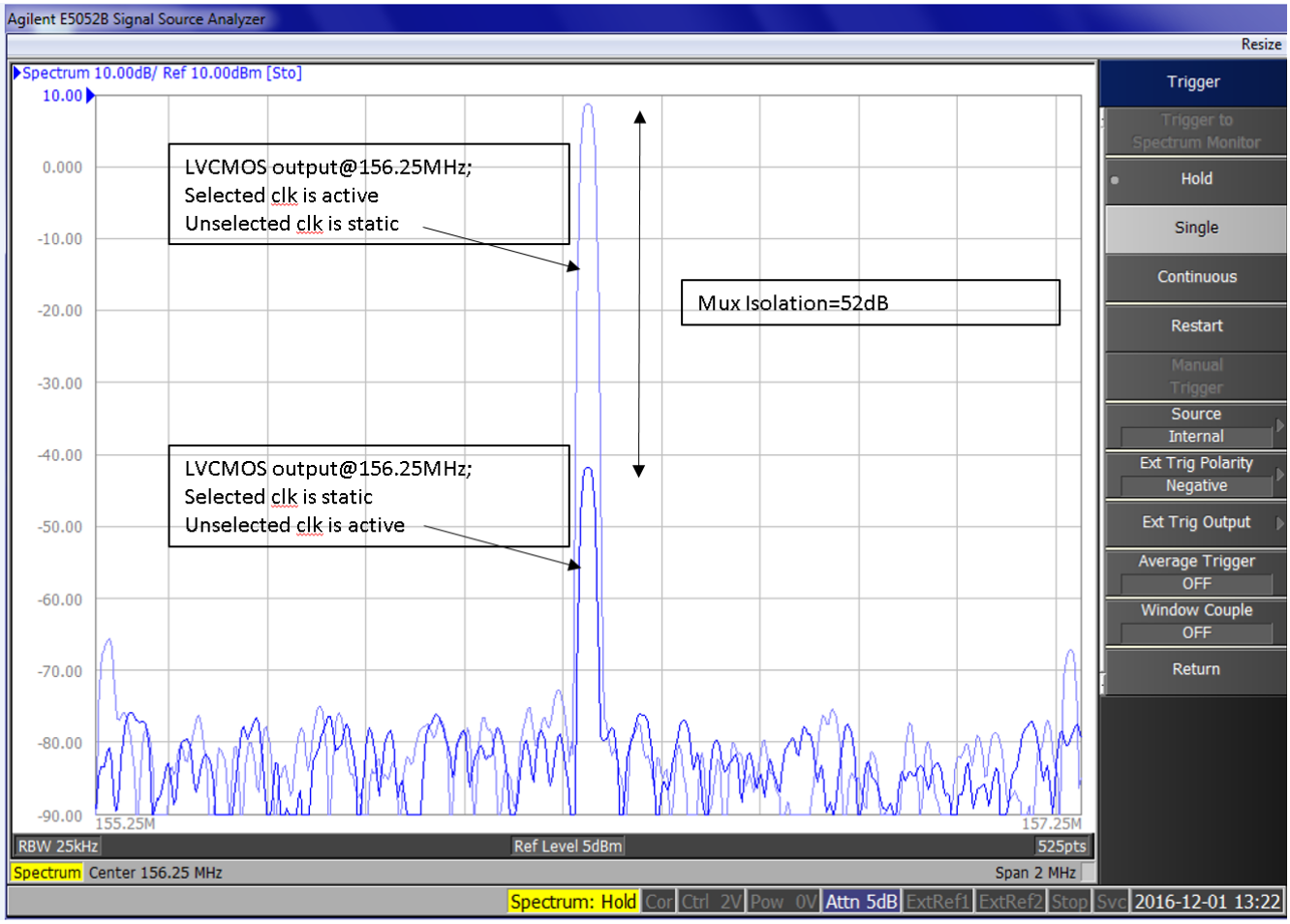


Figure 10. Input MUX Noise Isolation (Single-Ended Input Clock, 16-QFN Package)

3. Electrical Specifications

Table 8. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_S		–55	—	150	°C
Supply voltage	V_{DD}, V_{DDO}, V_{DDOx}		–0.5	—	3.8	V
Input voltage	V_{IN}		–0.5	—	V_{DD} + 0.3	V
Output voltage	V_{OUT}	Si53360, Si53365 only	—	—	V_{DD} + 0.3	V
		Si53361 only	—	—	V_{DDO} + 0.3	V
		Si53362 only	—	—	V_{DDOx} + 0.3	V
ESD sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	—	—	2000	V
	CDM		—	—	500	V
Peak soldering reflow temperature	T_{PEAK}	Pb-free; solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum junction temperature	T_J		—	—	125	°C

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 9. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient operating temperature	T_A		–40	—	85	°C
Supply voltage range	V_{DD}, V_{DDOx}	LVCMOS	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 10. Input Clock Specifications

V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS input high voltage	V_{IH}		V_{DD} x 0.7	—	—	V
LVCMOS input low voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input capacitance	C_{IN}	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

Table 11. DC Common Characteristics (CLK_SEL, OEx)

V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C
V_{DDO}/V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C (Si53361/2 only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current	I_{DD}[1]	V_{DD} = 3.3 V, Si53360/65	—	150	—	mA
		V_{DD} = 3.3 V, Si53361/62	—	35	—	mA
Output supply current (per clock output, Si53361/62 only)	I_{DDO}[1]	V_{DDOx} = 1.8 V	—	7	—	mA
		V_{DDOx} = 2.5 V	—	10	—	mA
		V_{DDOx} = 3.3 V	—	13	—	mA
Input-high voltage	V_{IH}		V_{DD} x 0.8	—	—	V
Input-low voltage	V_{IL}		—	—	V_{DD} x 0.2	V
Internal pull-up resistor	R_{UP}	OE_X, CLK_SEL	—	25	—	kΩ

1. Frequency = 200 MHz, C_{load} = 0 pF

Table 12. Output Characteristics (LVCMOS)

V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C
V_{DDO}/V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C (Si53361/2 only)

Parameter	Symbol	Test Condition[1]	Min	Typ	Max	Unit
Output voltage high	V_{OH}	I_{OH} = –12 mA, V_{DD} = 3.3 V I_{OH} = –9 mA, V_{DD} = 2.5 V I_{OH} = –6 mA, V_{DD} = 1.8 V	V_{DD} x 0.8	—	—	V
Output voltage low	V_{OL}	I_{OL} = 12 mA, V_{DD} 3.3 V I_{OL} = 9 mA, V_{DD} = 2.5 V I_{OL} = 6 mA, V_{DD} = 1.8 V	—	—	V_{DD} x 0.2	V

1. For this table, V_{DD} represents the output supply voltage: V_{DD} (Si5360/65), V_{DDO} (Si53361), or V_{DDOx} (Si53362).

Table 13. AC Characteristics

V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C
V_{DDO}/V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C (Si53361/2 only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVCMOS	dc	—	200	MHz
Duty cycle (50% input duty cycle)	DC	200 MHz, 2 pF load T_R/T_F < 10% of period	40	50	60	%
Minimum input clock slew rate	SR	Required to meet prop delay and additive jitter specifications (20 to 80%)	0.75	—	—	V/ns
Output rise/fall time	T_R/T_F	200 MHz, 20/80%, 2 pF load	—	—	850	ps
Minimum input pulse width	T_W		2	—	—	ns
Propagation delay	T_{PLH}, T_{PHL}	Low-to-high, high-to-low single-ended, C_L = 2 pF	1.5	3.0	4.5	ns

Table 13. AC Characteristics (Continued)

V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C
V_{DDO}/V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C (Si53361/2 only)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output enable time	T_{EN}	F = 1 MHz	—	10	—	ns
		F = 100 MHz	—	10	—	ns
Output disable time	T_{DIS}	F = 1 MHz	—	20	—	ns
		F = 100 MHz	—	20	—	ns
Part-to-part skew	T_{SKPP}	C_L = 2 pF	0	—	300	ps
Output-to-output skew	T_{SK}	C_L = 2 pF	—	40	125	ps

Table 14. Additive Jitter

$V_{DD}/V_{DDO}/V_{DDOx}$	Input[1]				Output	Additive Jitter (fs_{RMS}, 12 kHz to 20 MHz)	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Slew Rate (Single-Ended 20 to 80%) (V/ns)	Clock Format	Typ	Max
3.3	200	Single-ended	1.7	1.0	LVCMOS	130	180
3.3	156.25	Single-ended	2.18	1.0	LVCMOS	125	220
2.5	200	Single-ended	1.7	1.0	LVCMOS	115	250
2.5	156.25	Single-ended	2.18	1.0	LVCMOS	125	240

1. For best additive jitter results, use the fastest slew rate possible. See AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance for more information.

Table 15. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
16-TSSOP thermal resistance (junction-to-ambient)	θ_{JA}	Still air	124.4	°C/W
16-QFN thermal resistance (junction-to-ambient)	θ_{JA}	Still air	57.6	°C/W
16-QFN thermal resistance (junction-to-case)	θ_{JC}	Still air	41.5	°C/W
24-QFN thermal resistance (junction-to-ambient)	θ_{JA}	Still air	37	°C/W
24-QFN thermal resistance (junction-to-case)	θ_{JC}	Still air	25	°C/W

4. Detailed Block Diagrams

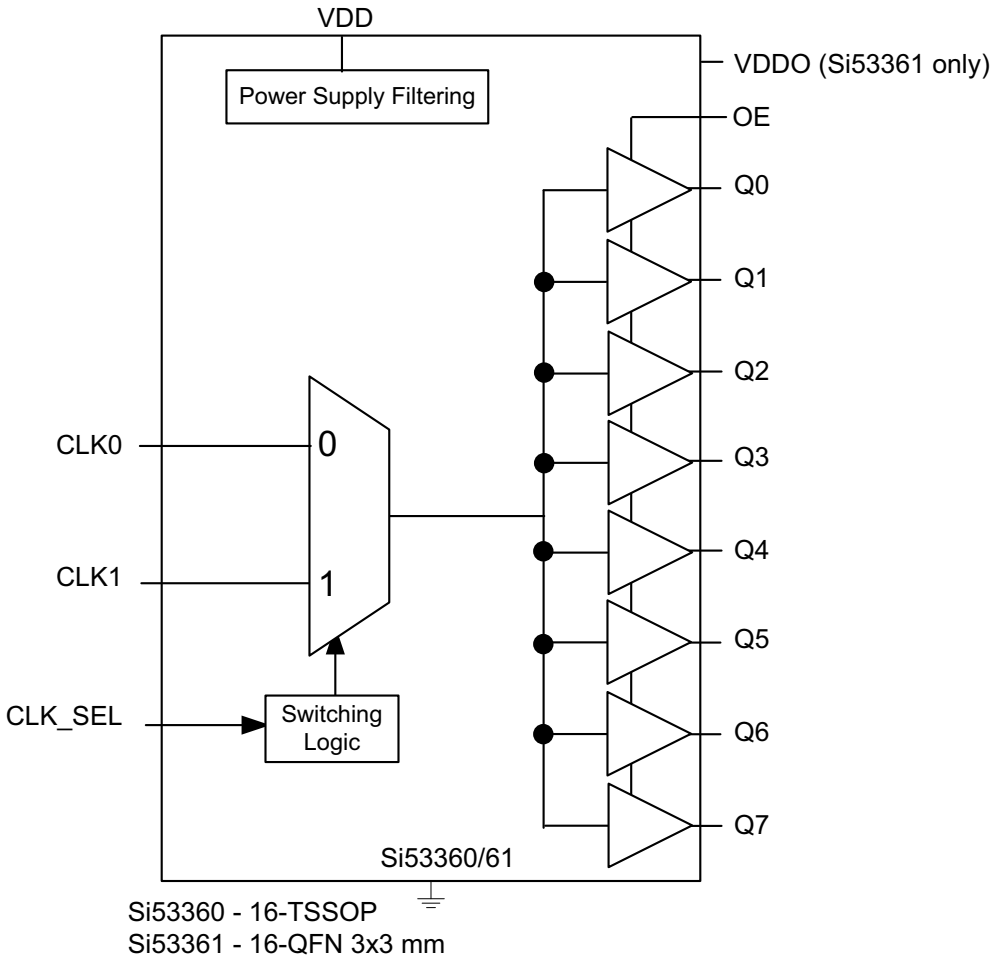


Figure 11. Si53360 and Si53361 Block Diagram

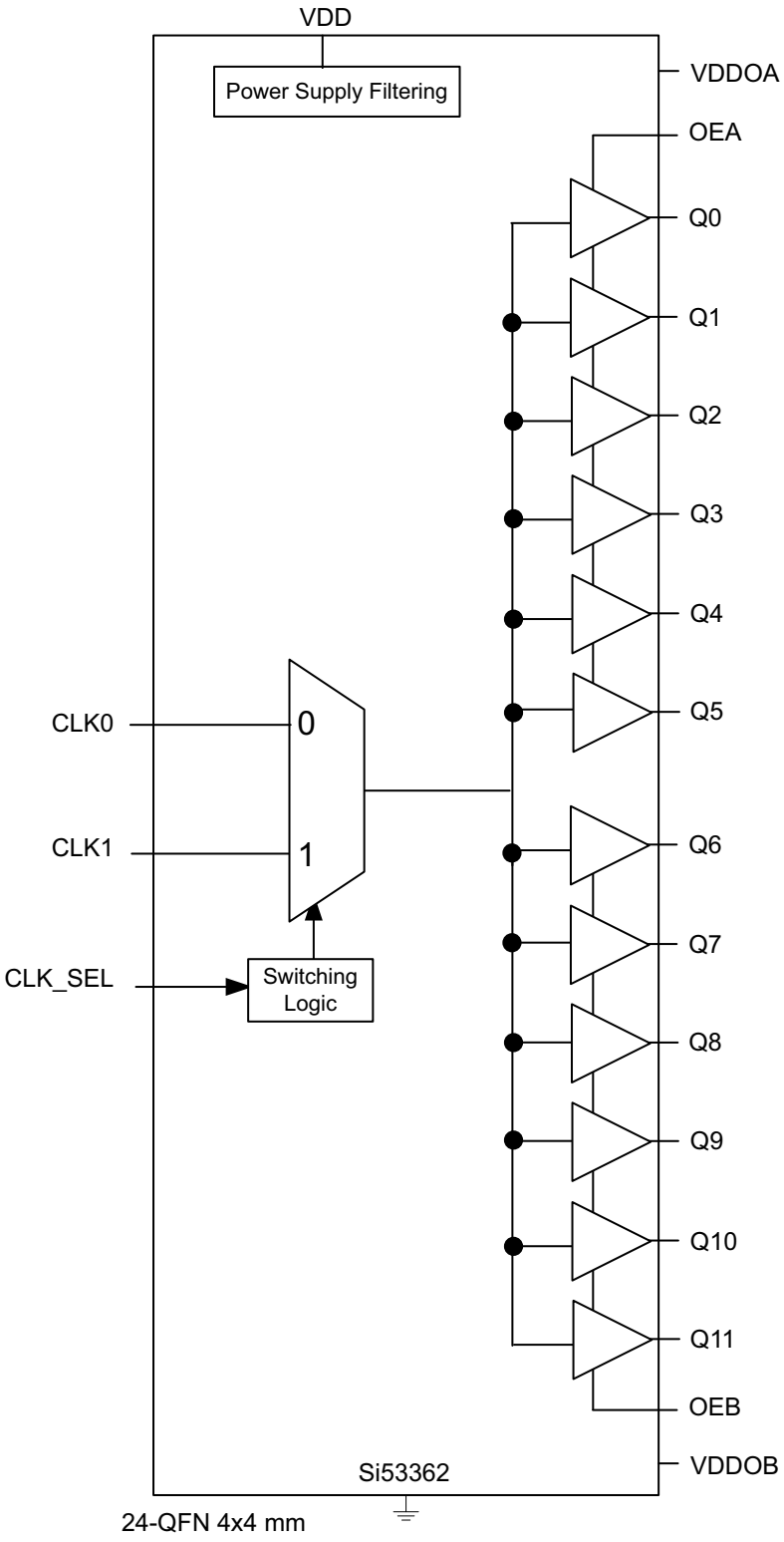


Figure 12. Si53362 Block Diagram

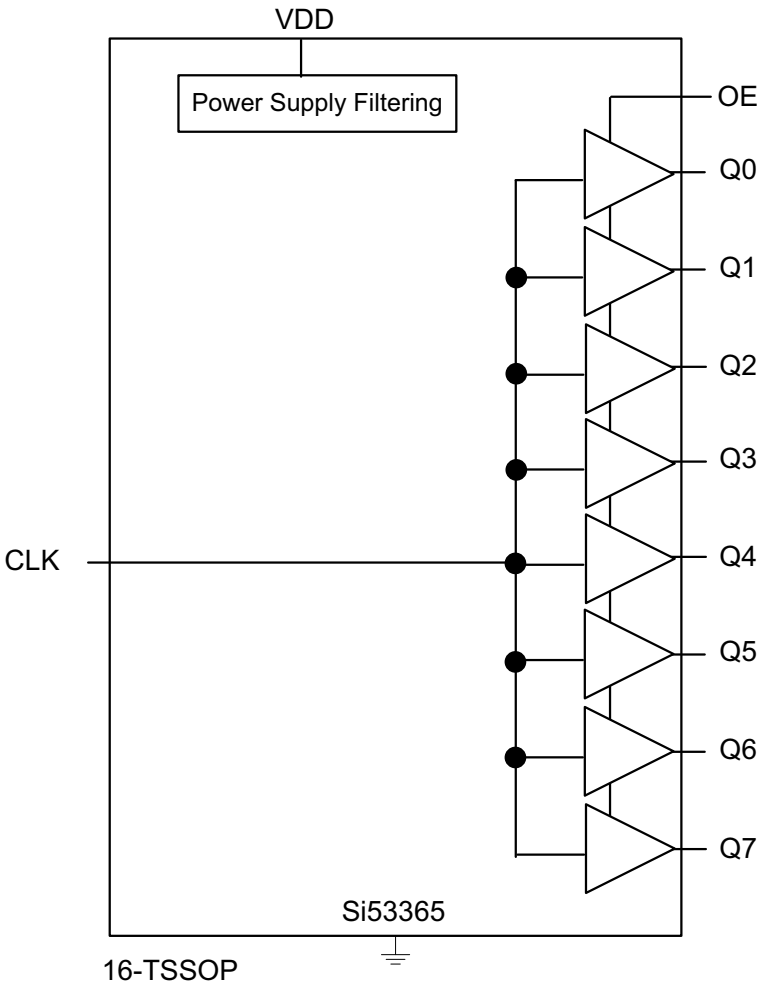


Figure 13. Si53365 Block Diagram

5. Package Outlines

5.1. 16-Pin TSSOP Package

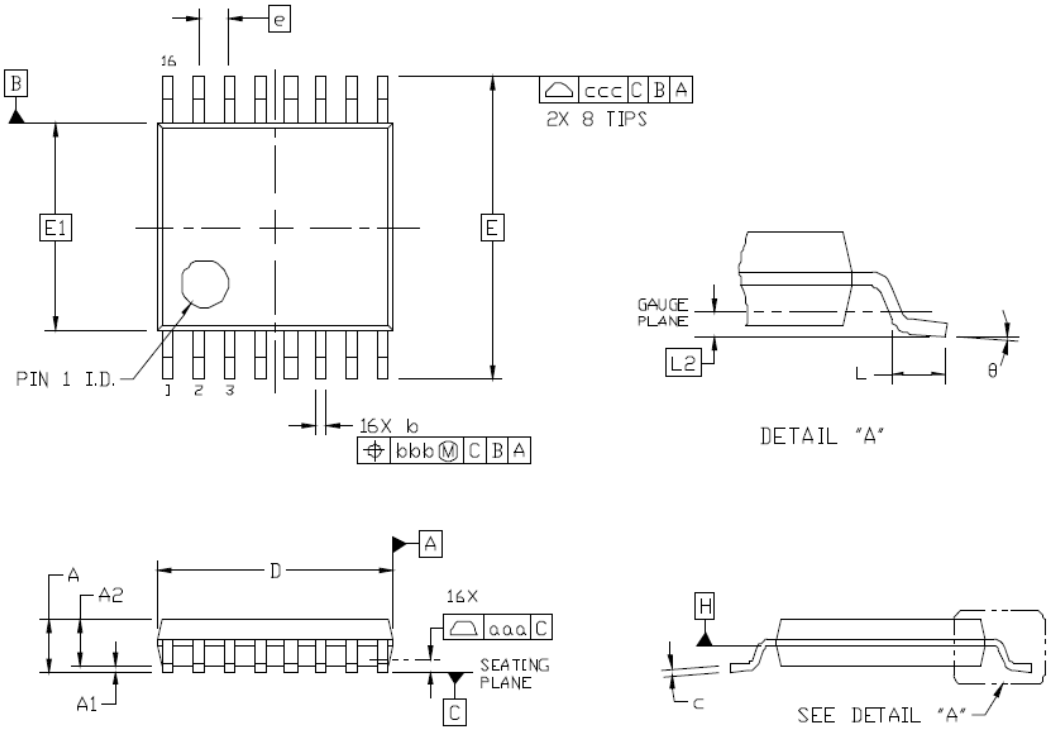


Figure 14. 16-Pin TSSOP Package

Table 16. 16-Pin TSSOP Package Dimensions[1,2,3,4]

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L2		0.25 BSC	
θ	0°	—	8°

Table 16. 16-Pin TSSOP Package Dimensions[1,2,3,4] (Continued)

Dimension	Min	Nom	Max
aaa		0.10	
bbb		0.10	
ccc		0.20	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5.2. 16-Pin QFN Package

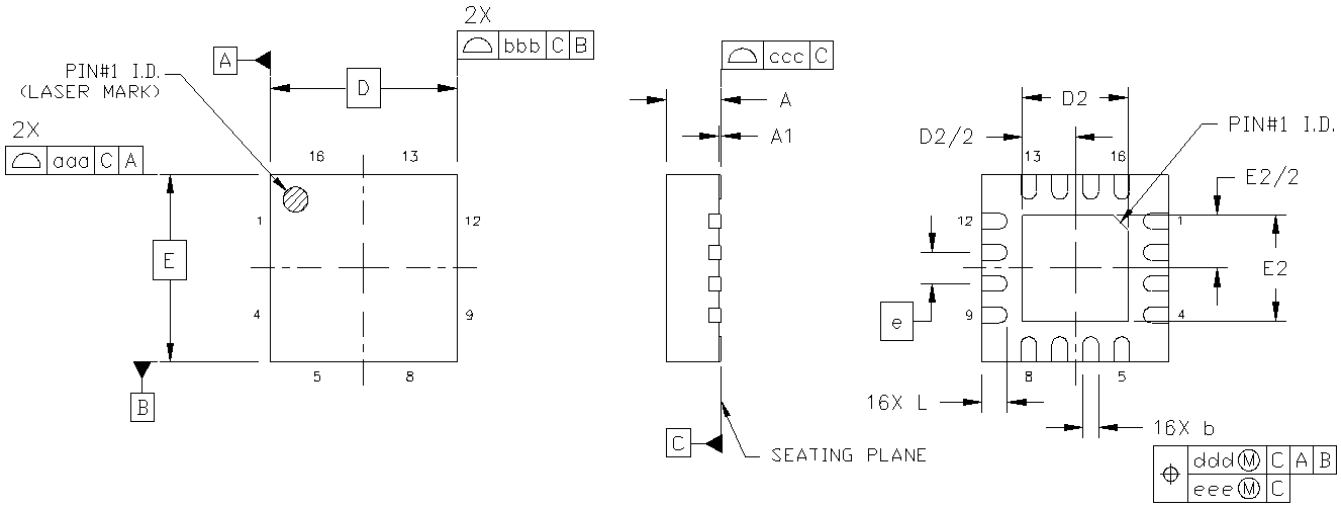


Figure 15. 16-Pin QFN Package

Table 17. 16-QFN Package Dimensions[1,2]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.65	1.70	1.75
e		0.50 BSC.	
E		3.00 BSC.	
E2	1.65	1.70	1.75
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

5.3. 24-Pin QFN Package

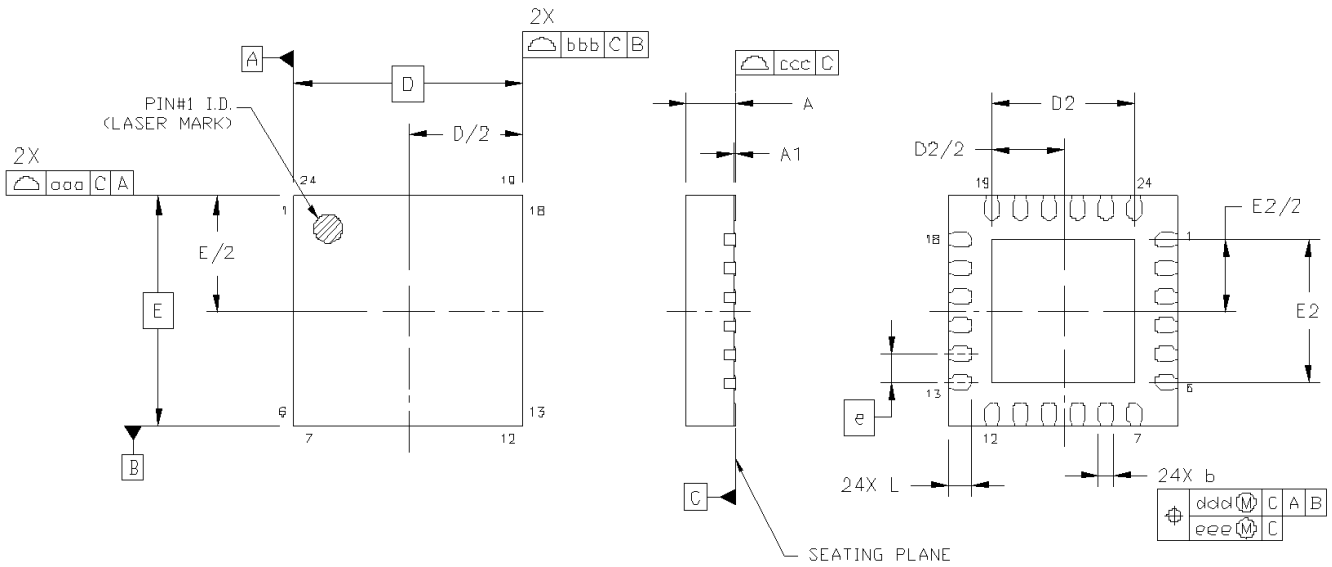


Figure 16. 24-Pin QFN Package

Table 18. 24-QFN Package Dimensions[1,2,3,4]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

6. PCB Land Patterns

6.1. 16-Pin TSSOP Land Pattern

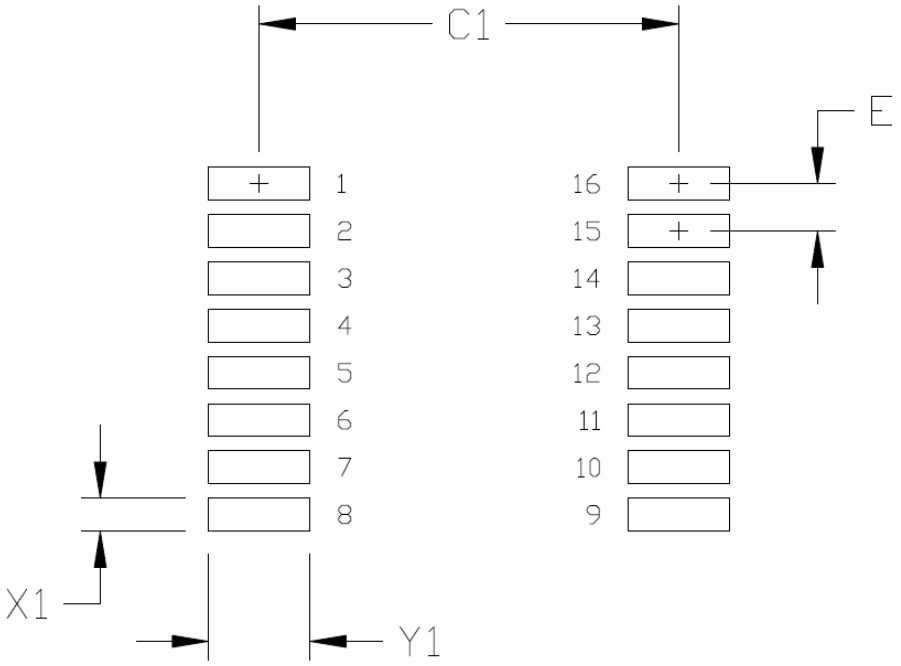


Figure 17. 16-Pin TSSOP Land Pattern

Table 19. 16-Pin TSSOP Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad column spacing	5.80
E	Pad row pitch	0.65
X1	Pad width	0.45
Y1	Pad length	1.40

1. This land pattern design is based on IPC-7351 specifications for Density Level B (median land protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.2. 16-Pin QFN Land Pattern

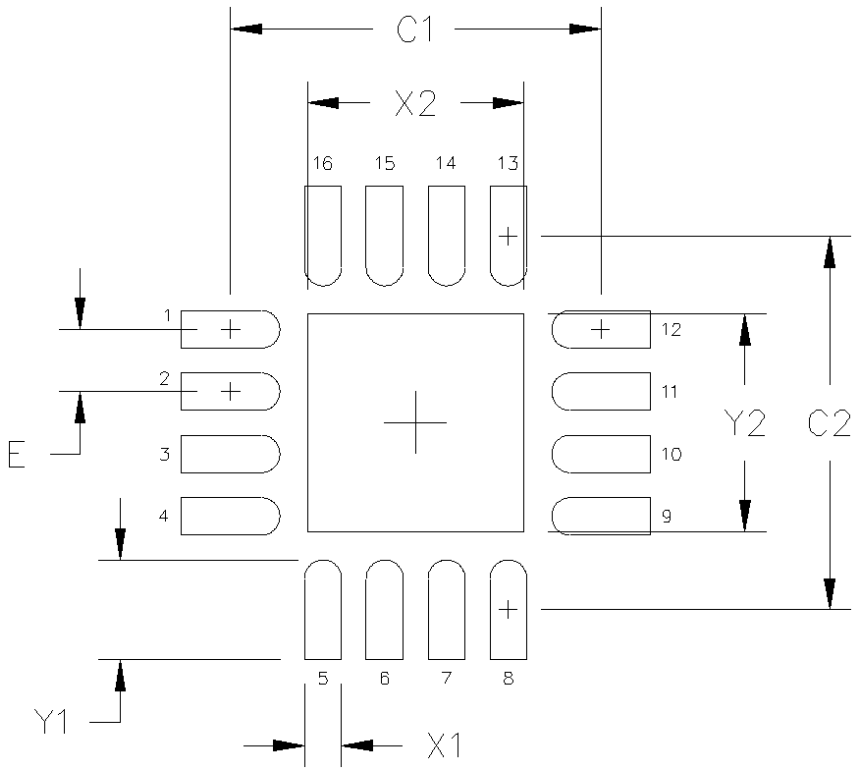


Figure 18. 16-Pin QFN Land Pattern

Table 20. 16-Pin QFN Land Pattern Dimensions

Dimension	mm	Notes
C1	3.00	**Notes:** **General** 1. All dimensions shown are in millimeters (mm). 2. This land pattern design is based on the IPC-7351 guidelines. 3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder-paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 2x2 array of 0.65 mm square openings on a 0.9 mm pitch should be used for the center ground pad. **Card Assembly** 1. A no-clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
C2	3.00	
E	0.50	
X1	0.30	
Y1	0.80	
X2	1.75	
Y2	1.75	

6.3. 24-Pin QFN Land Pattern

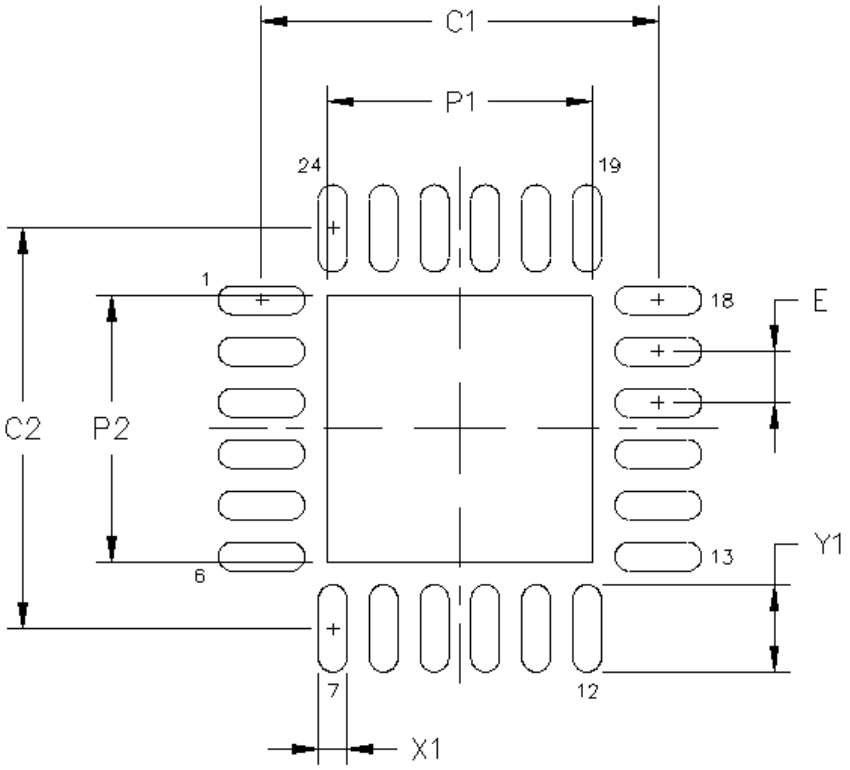


Figure 19. 24-Pin QFN Land Pattern

Table 21. 24-Pin QFN Land Pattern Dimensions

Dimension	mm	Notes
P1	2.55	**Notes:** **General** 1. All dimensions shown are in millimeters (mm). 2. This land pattern design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be Non Solder Mask Defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder-paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
P2	2.55	
X1	0.25	
Y1	0.80	
C1	3.90	
C2	3.90	
E	0.50	

7. Top Markings

7.1. Si53360/65 Top Markings

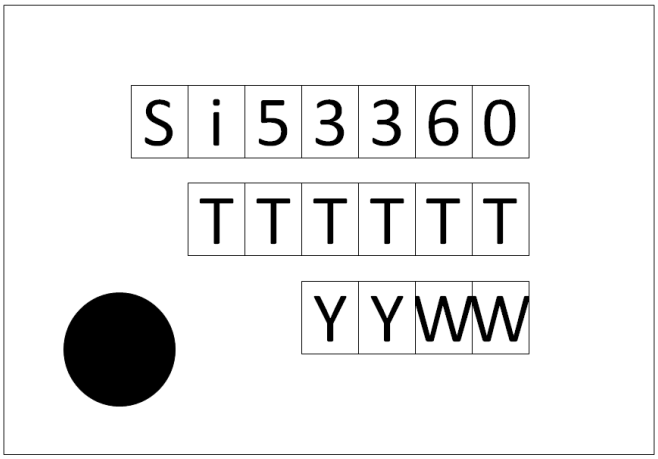


Figure 20. Si53360 Top Marking

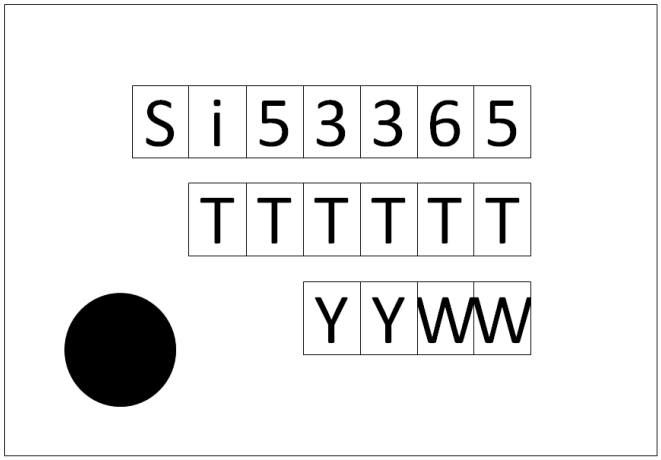


Figure 21. Si53365 Top Marking

Si53360/65 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 point (0.71 mm), right-justified	
Line 1 Marking:	Device part number	
Line 2 Marking:	TTTTTT = Mfg code	Manufacturing code from the assembly purchase order form.
Line 3 Marking	YY = year, WW = work week	Corresponds to the year and work week of the mold date.

7.2. Si53361 Top Marking

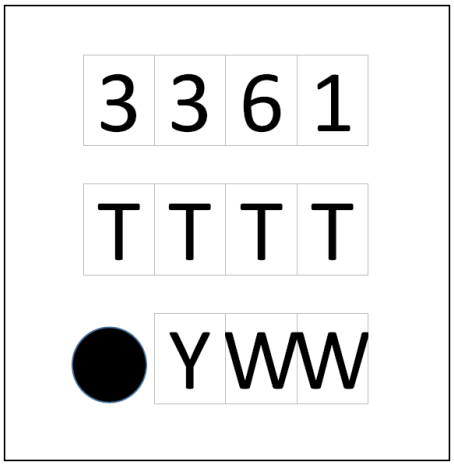


Figure 22. Si53361 Top Marking

Table 22. Si53361 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (0.71 mm), center-aligned	
Line 1 Marking:	Device part number	3361 for Si53361
Line 2 Marking:	TTTT = Mfg code	Manufacturing code from the assembly purchase order form.
Line 3 Marking	Y = year WW = work week	Corresponds to the year and work week of the mold date.

7.3. Si53362 Top Marking

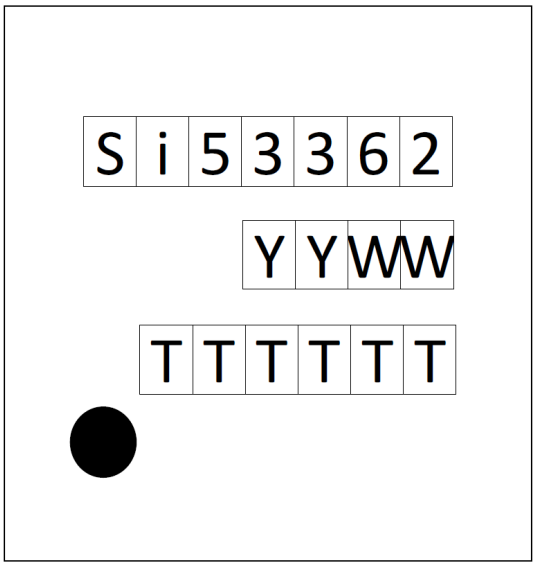


Figure 23. Si53362 Top Marking

Table 23. Si53362 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 point (0.71 mm), right-justified	
Line 1 Marking:	Device part number	53362 for Si53362
Line 2 Marking	YY = year WW = work week	Corresponds to the year and work week of the mold date.
Line 3 Marking:	TTTTTT = Mfg code	Manufacturing code from the assembly purchase order form.

8. Ordering Guide

Table 24. Si5336x Ordering Guide

Part Number	Input	LVCMOS Output	Output Enable	Frequency Range	Package
Si53360-B-GT	2:1 selectable MUX LVCMOS	1 bank/8 outputs	Single	dc to 200 MHz	16-TSSOP
Si53361-B-GM	2:1 selectable MUX LVCMOS	1 bank/8 outputs (settable VDDO)	Single	dc to 200 MHz	16-QFN 3x3 mm
Si53362-B-GM	2:1 selectable MUX LVCMOS	2 banks/6 outputs	1 per bank	dc to 200 MHz	24-QFN 4x4 mm
SI53365-B-GT	1 bank/1 Input LVCMOS	1 bank/8 outputs	Single	dc to 200 MHz	16-TSSOP

9. Revision History

Revision	Date	Description
A	May, 2025	• Added V_{DDO} and V_{DDOx} to Table 8, “Absolute Maximum Ratings,” on page 13. • Added V_{DDOx} to Table 9, “Recommended Operating Conditions,” on page 13. • Updated table description in Table 11, “DC Common Characteristics (CLK_SEL, OEx),” on page 14. • Updated table description in Table 12, “Output Characteristics (LVCMOS),” on page 14. • Updated table description in Table 13, “AC Characteristics,” on page 14.
1.3	December, 2018	• Changed CLK_SEL from pull-down resistor to pull-up resistor. • Updated output state to low when OE pin is asserted low on Si53365.
1.2	December, 2016	• Introduced new Si53361 and Si53362 devices. • Merged Si53360/65 data sheets with the new devices to create a single LVCMOS buffer data sheet. • Added core supply current specification at multiple supply voltages. • Added “Internal pull-down resistor” typical specification.