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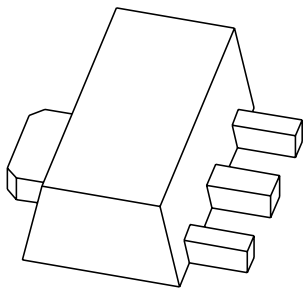
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Kind regards,

Team Nexperia

DATA SHEET



PBSS5330X

30 V, 3 A

PNP low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2003 Nov 28

2004 Nov 03

30 V, 3 A PNP low V_{CEsat} (BISS) transistor

PBSS5330X

FEATURES

- SOT89 (SC-62) package
- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- Higher efficiency leading to less heat generation
- Reduced printed-circuit board requirements.

APPLICATIONS

- Power management
 - DC/DC converters
 - Supply line switching
 - Battery charger
 - LCD backlighting.
- Peripheral drivers
 - Driver in low supply voltage applications (e.g. lamps and LEDs)
 - Inductive load driver (e.g. relays, buzzers and motors).

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT89 plastic package.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS5330X	*1S

Note

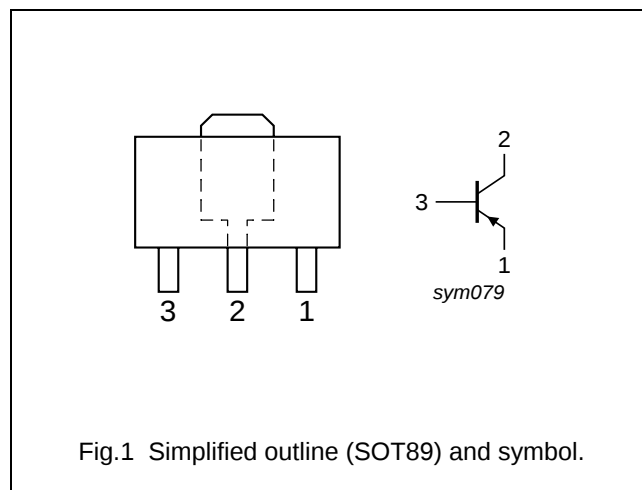
- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	−30	V
I_C	collector current (DC)	−3	A
I_{CM}	peak collector current	−5	A
R_{CEsat}	equivalent on-resistance	107	mΩ

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5330X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

30 V, 3 A

PNP low V_{CEsat} (BISS) transistor

PBSS5330X

LIMITING VALUES

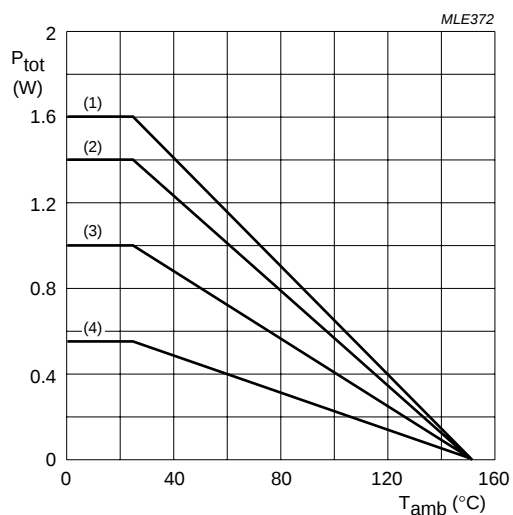
In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CEO}	collector-emitter voltage	open base	–	–30	V
V_{EBO}	emitter-base voltage	open collector	–	–6	V
I_C	collector current (DC)	note 4	–	–3	A
I_{CM}	peak collector current	limited by $T_{j(max)}$	–	–5	A
I_B	base current (DC)		–	–0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$			
		note 1	–	550	mW
		note 2	–	1	W
		note 3	–	1.4	W
		note 4	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; standard footprint.
2. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 1 cm².
3. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 6 cm².
4. Device mounted on a ceramic printed-circuit board 7 cm², single-sided copper, tin-plated.

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- (1) Ceramic PCB; 7 cm² mounting pad for collector.
- (2) FR4 PCB; 6 cm² copper mounting pad for collector.
- (3) FR4 PCB; 1 cm² copper mounting pad for collector.
- (4) Standard footprint.

Fig.2 Power derating curves.

30 V, 3 A

PNP low V_{CEsat} (BISS) transistor

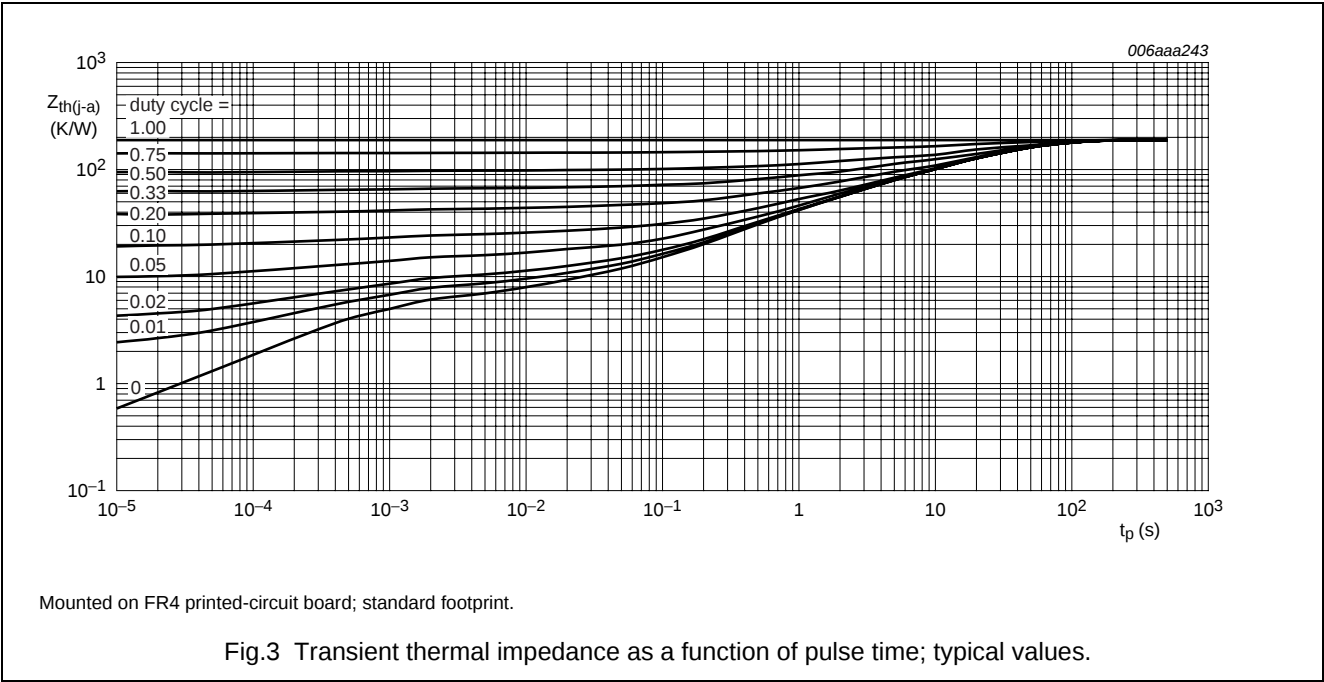
PBSS5330X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		note 1	225	K/W
		note 2	125	K/W
		note 3	90	K/W
		note 4	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

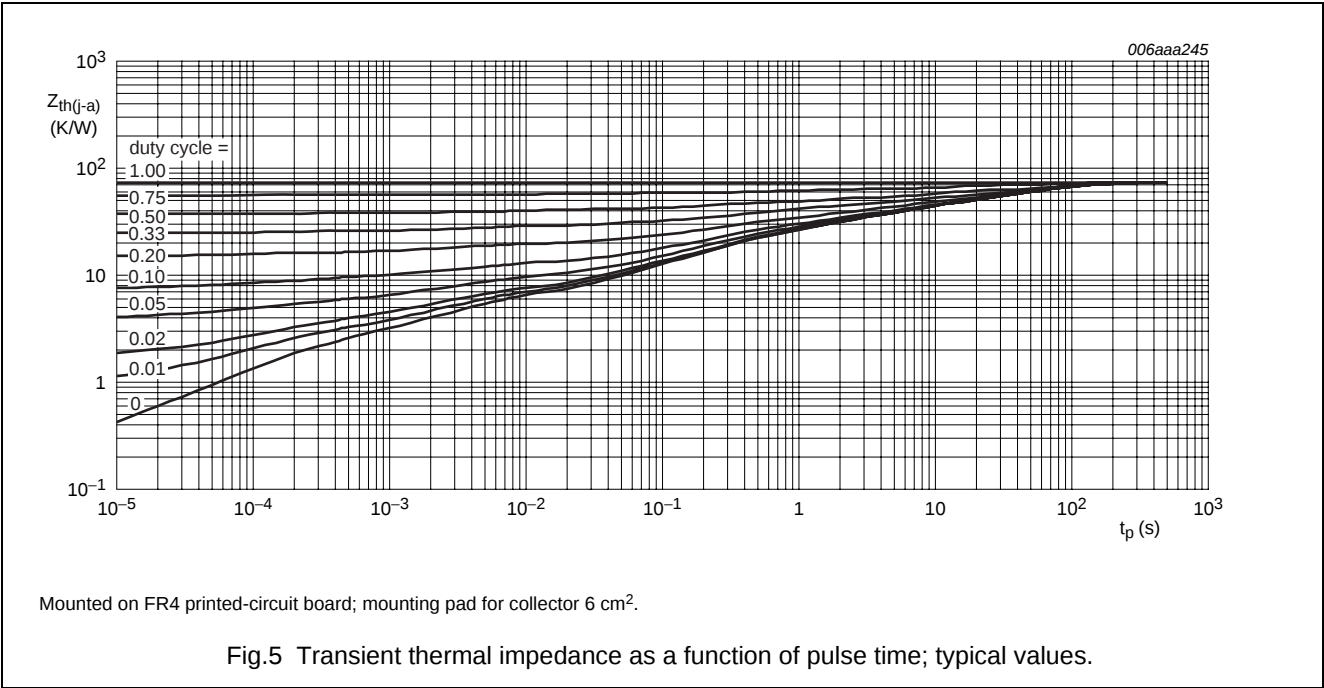
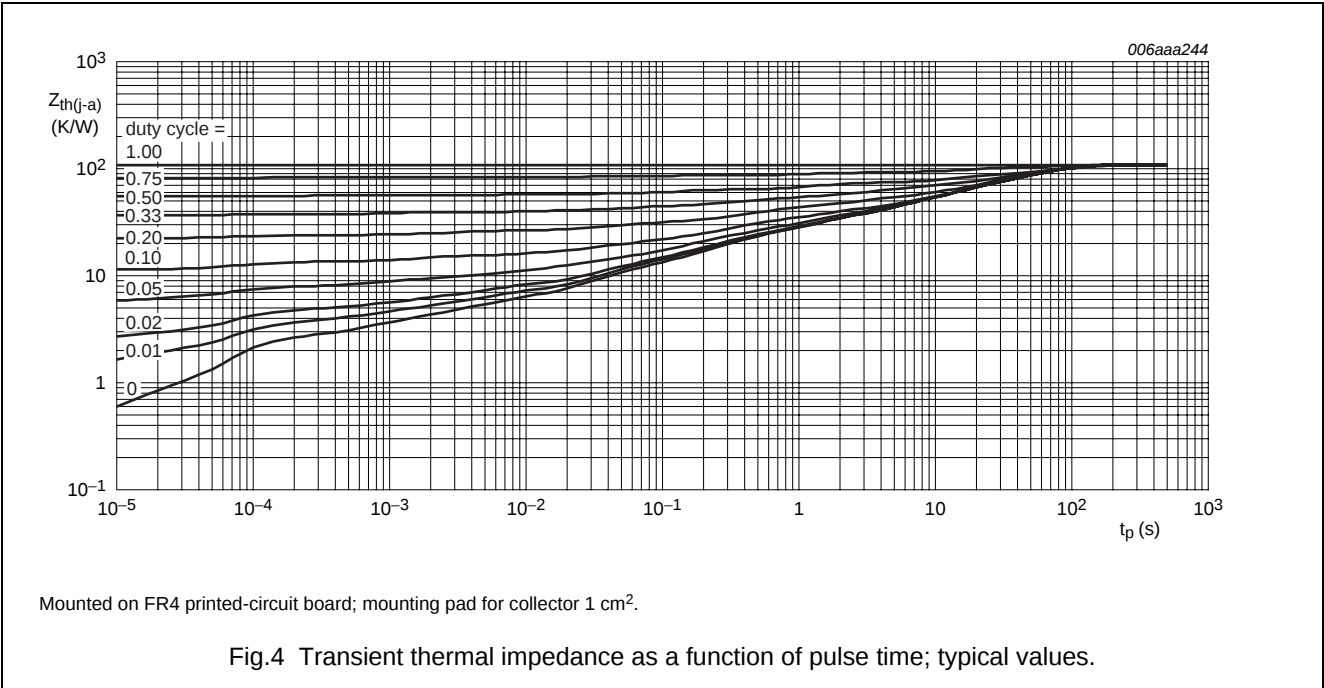
Notes

1. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; standard footprint.
2. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 1 cm².
3. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 6 cm².
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CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	–	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0\text{ A}; T_J = 150\text{ °C}$	–	–	–50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; V_{BE} = 0\text{ V}$	–	–	–100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}$				
		$I_C = -0.1\text{ A}$	200	–	–	
		$I_C = -0.5\text{ A}$	200	–	–	
		$I_C = -1\text{ A}; \text{note 1}$	175	–	450	
		$I_C = -2\text{ A}; \text{note 1}$	140	–	–	
		$I_C = -3\text{ A}; \text{note 1}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	–	–	–70	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–	–130	mV
		$I_C = -2\text{ A}; I_B = -100\text{ mA}$	–	–	–240	mV
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	–	–320	mV
R_{CEsat}	equivalent on-resistance	$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	80	107	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -100\text{ mA}$	–	–	–1.1	V
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	–	–	–1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	–1.0	–	–	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V};$ $f = 100\text{ MHz}$	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	–	–	45	pF

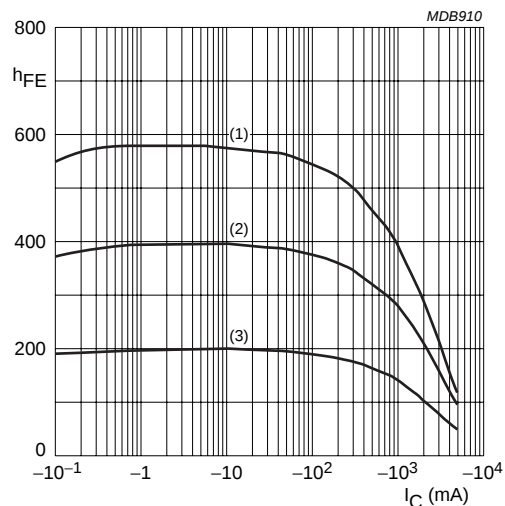
Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

30 V, 3 A

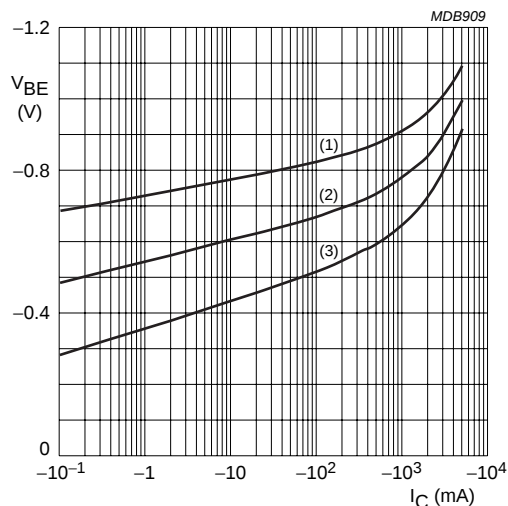
PNP low V_{CEsat} (BISS) transistor

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 $V_{CE} = -2$ V.

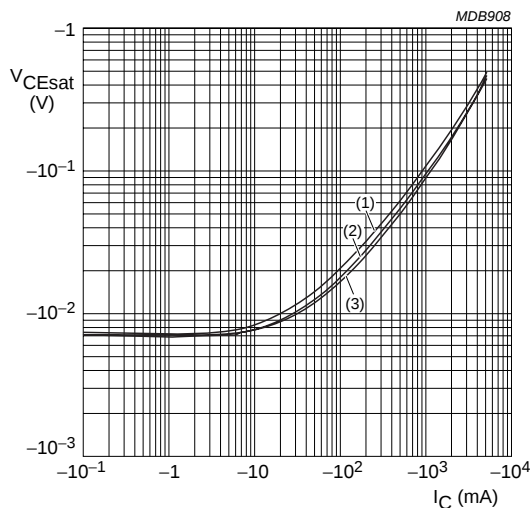
- (1) $T_{amb} = 100$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = -55$ °C.

Fig.6 DC current gain as a function of collector current; typical values.

 $V_{CE} = -2$ V.

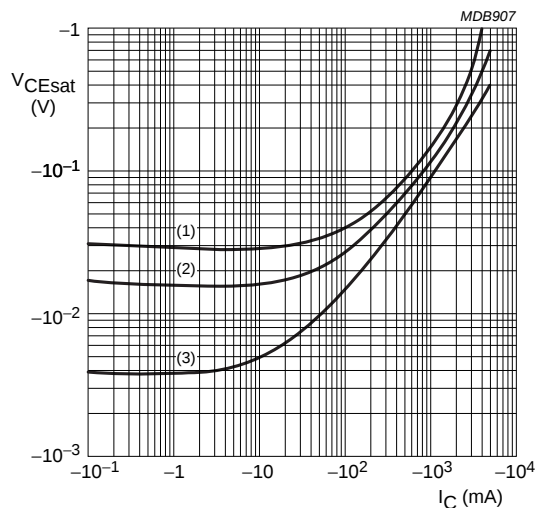
- (1) $T_{amb} = -55$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = 100$ °C.

Fig.7 Base-emitter voltage as a function of collector current; typical values.

 $I_C/I_B = 20$.

- (1) $T_{amb} = 100$ °C.
- (2) $T_{amb} = 25$ °C.
- (3) $T_{amb} = -55$ °C.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.

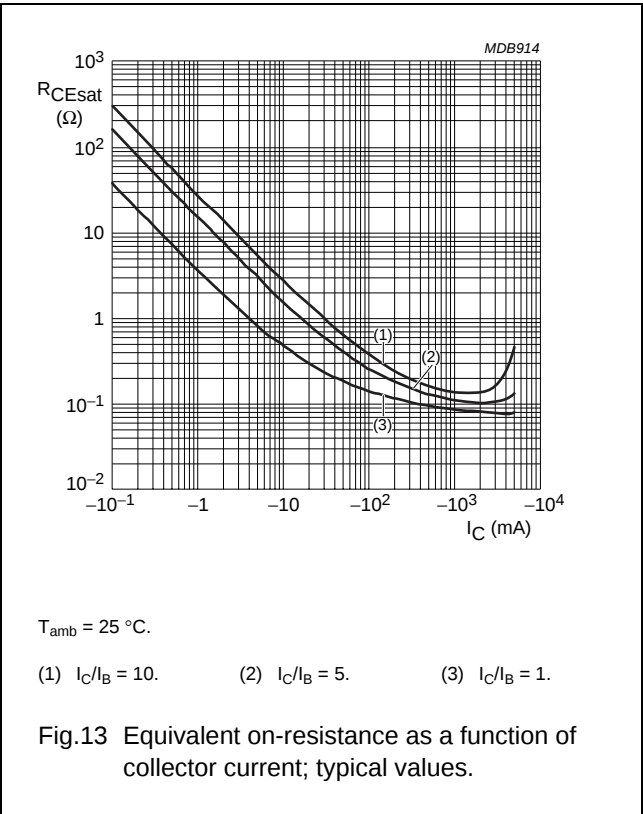
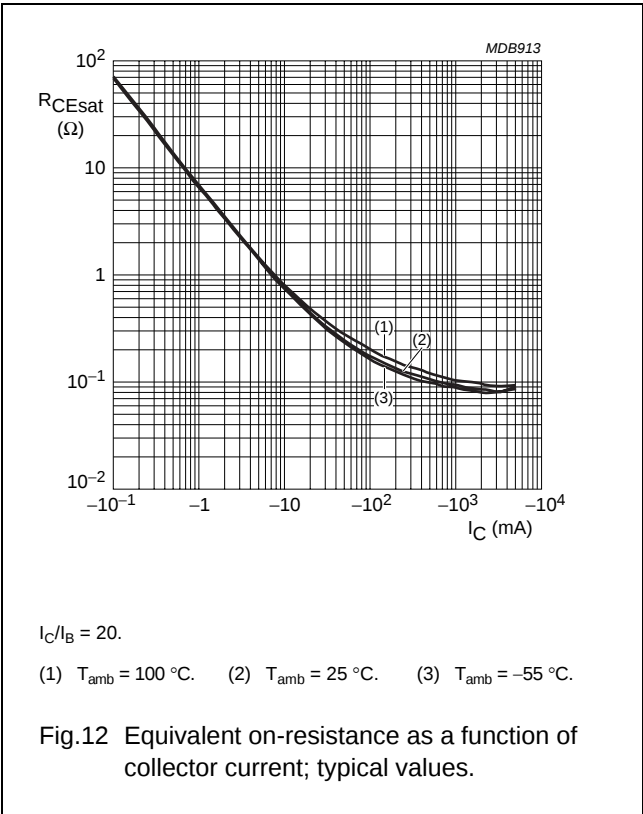
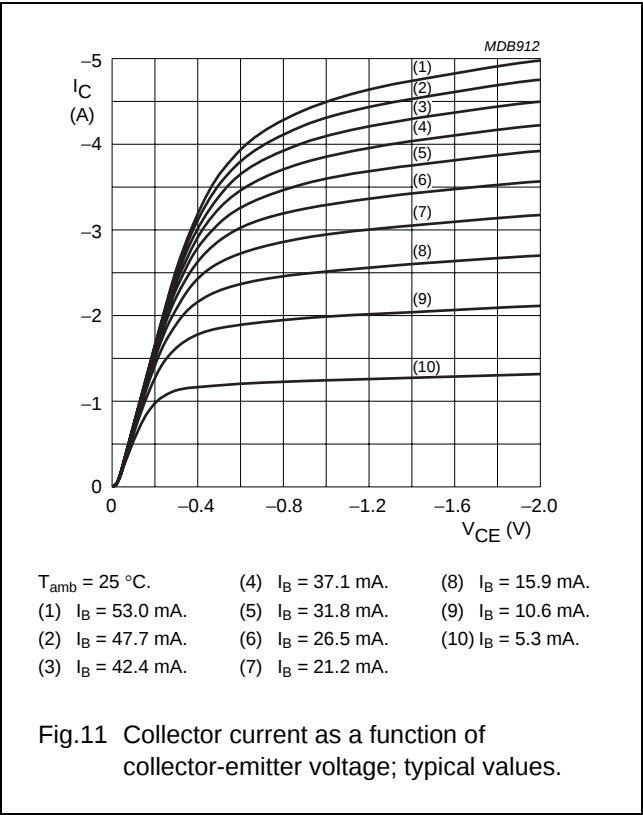
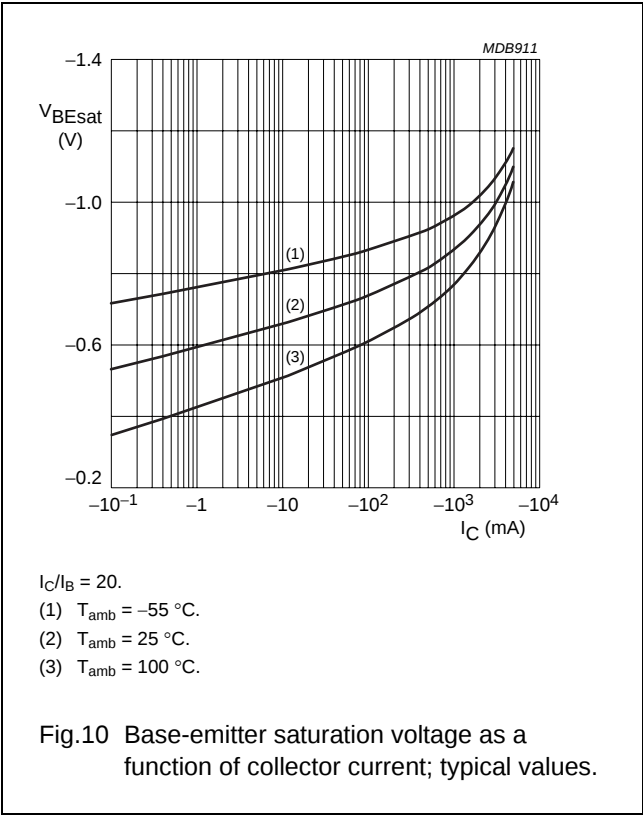
 $T_{amb} = 25$ °C.

- (1) $I_C/I_B = 100$.
- (2) $I_C/I_B = 50$.
- (3) $I_C/I_B = 10$.

Fig.9 Collector-emitter saturation voltage as a function of collector current; typical values.

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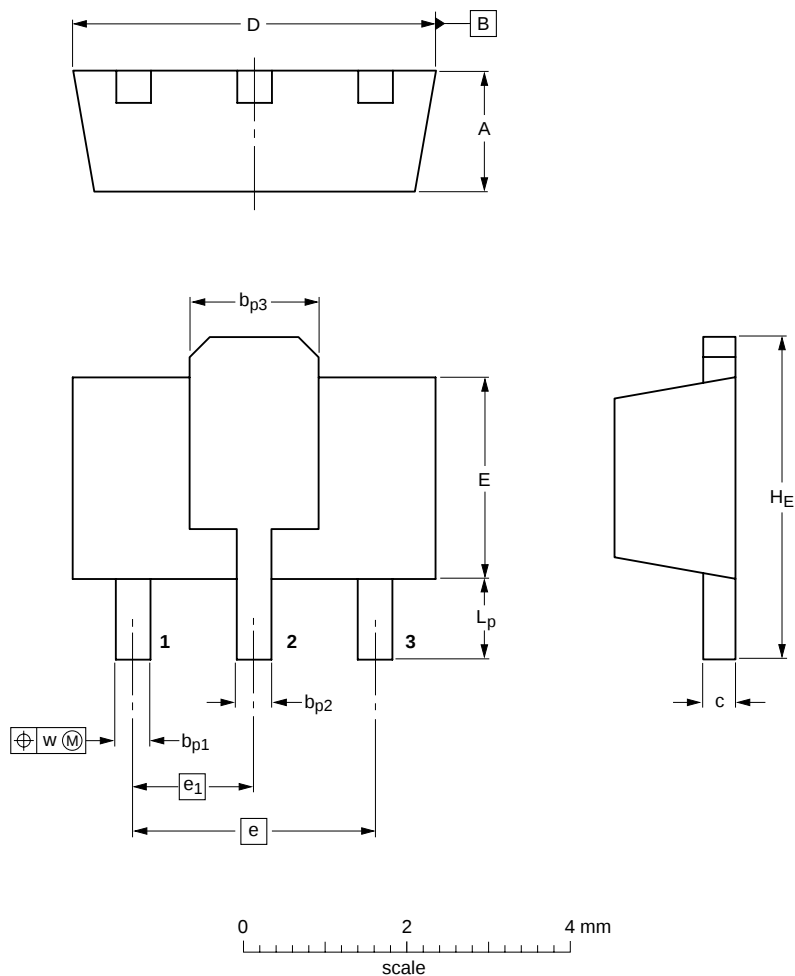
30 V, 3 A
PNP low V_{CEsat} (BISS) transistor

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PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			04-08-03 06-03-16

30 V, 3 A

PNP low V_{CEsat} (BISS) transistor

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

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Contact information

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