Description

The RT3A and RT3AQ are temperature compensated real-time clock modules with integrated crystal, eliminating the need for an external 32.768 kHz crystal. The device supports clock/calendar, programmable alarms, fixed cycle timer, and a programmable square-wave output. Address and data are transferred serially through an I²C bus.

With integrated DTCXO, the device supports up to +/-3.5ppm clock accuracy for -40°C to +85°C temperature range and +/-10ppm for -40°C to +125°C temperature range.

The device also has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm and timer operation. RT3A is industrial grade and RT3AQ is automotive grade. Both devices are available in a small 3225 ceramic package.

Application(s)

- Home Appliances
- Surveillances
- Automotive Infotainment, T-Box, Dash Board

Features

- Real-Time Clock Module (RTC) for Time (Seconds, Minutes and Hours) and Calendar (Day, Date, Month and Year with Leap-Year Compensation Valid Up to 2100)
- Temperature Compensated with Integrated Crystal
  - +/-3.5ppm -40°C to 85°C (Equivalent to 9sec/Month Deviation), RT3A3241N3/Q3
  - +/-5ppm -40°C to +85°C (Equivalent to 13sec/Month Deviation), RT3A3240N3
  - +/-10ppm -40°C to +125°C (Equivalent to 26sec/Month Deviation), RT3A3240Q1
- Max 50uA current consumption with temp compensation
- 1st year aging -2ppm, 15 year aging -8ppm
- Typical 22uA current consumption when output and I2C is disabled
- I²C Serial Interface Supports I²C-Bus's High Speed Mode (400 kHz)
- Programmable square wave frequency output, defaults to 32 kHz on Power-up
- Alarm and Fixed Cycle Timer Interrupt
- Max Timer Duration Up to 22.75 Days
- Automatic Power-Fail Detect and Switch Circuitry
- The RT3A: -40°C to +85°C
- The RT3AQ: -40°C to +125°C, AECQ
- Packaging (Pb-free & Green available):
  - 10-pad Ceramic SMD package, 3.2x2.5mm
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The RT3AQ is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
  https://www.diodes.com/quality/product-definitions/

Table 1. Diverse functions of RTC circuits

Item	Function			RT3A/RT3AQ
1	Time	Display	24-hour	√
2	Interrupt	Alarm interrupt		√
		Fixed Cycle Timer interrupt		√
		Minute or Second interrupt		√
3	Programmable square wave output (Hz)			1, 1024, 32.768K
4	Communication	2-wire I²C bus		√
5	Power failure detect			√
6	Temperature Compensation			√

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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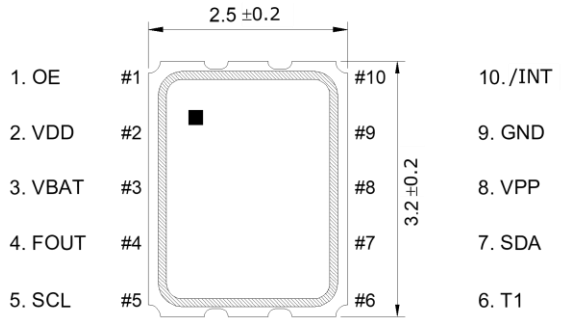
Pin Configuration



Pin Description

Pin Number	Pin Name	Type	Description
1	OE	I	**Square-Wave Frequency Output Enable** 1 = enable, 0 = disable
5	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on V_{DD}.
7	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{DD}.
3	V_{BAT}	P	**Secondary Power Supply.** Supply voltage must be held between 1.6V and 5.5V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Diodes should not be placed in series between the backup source and the V_{BAT} input, or improper operation will result. If a backup supply is not required, V_{BAT} must be connected to VDD.
4	Fout	O	CMOS output. When OE = High, Fout outputs 32.768 kHz signal. When OE = Low, Fout = Hi-Z
10	/INT	O	**Interrupt Output.** It is an open-drain output and requires an external pull up resistor. The pull up voltage may be up to 5.5V regardless of the voltage on V_{DD}. If not used, this pin may be left unconnected.
2	V_{DD}	P	**Power.** When voltage is applied within normal limits, the device is fully accessible and data can be written and read.
9	GND	P	**Ground.**
6	T1	I	Test mode enable: 1 = enable, 0 = disable (do not connect externally)
8	VPP	I/O	For manufacturer OTP mode: VPP = 2.7V to 3V; For other mode = floating; (do not connect externally)

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Maximum Ratings

Storage Temperature	-55°C to +150°C
Junction Temperature	max 150°C
Supply Voltage to Ground Potential (V_{CC} to GND)	-0.3V to +6.0V
DC Input (All Other Inputs except V_{CC} & GND)	-0.3V to V_{CC} +0.3V
DC Output Voltage (SDA, SQW /INT pins)	-0.3V to +6.0V
Power Dissipation	320mW (depend on package)
Lead Temperature (soldering, 10s)	+260 °C
Soldering Temperature (reflow)	+260 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.5	3.3	3.6	V
V_{BAT}	1BBackup Supply Voltage	1.6	3.0	3.6	V
Vtemp	Temperature Compensation Voltage	2.0	3.0	3.6	V
T_A	3BRT3A Operating Temperature	-40	25	85	°C
	4BRT3AQ1 Operating Temperature	-40	25	125	°C

DC Electrical Characteristics

Unless otherwise specified, V_{CC} = MIN to MAX, V_{BACKUP}=MIN to MAX, T_A = -40 °C to +85 °C

Symbol	Item	Pin	Condition	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage	SCL, SDA, FOE	V_{IN} = V_{DD} or GND	-1		1	µA
I_{LO}	I/O Leakage	SDA, FOUT/INT	V_{out} = V_{DD} or GND	-1		1	µA
Icomp1	Temperature Compensation Current Consumption		V_{DD} = 3V, V_{DD} = Vbat FOE = GND Fout = off, I2C = off, Temp comp interval 0.5s Voltage detection time 2ms		22	50	µA
Icomp2	Temperature Compensation Current Consumption		V_{DD} = 3V, V_{DD} = Vbat FOE = V_{DD}, Fout = 32.768kHz, I2C = off, CL = 0pF, Temp comp interval 0.5s Voltage detection time 2ms		25	50	uA
V_{IH}	High Level Input Voltage			0.7* VDD		VDD +0.3	V
V_{IL}	Low Level Input voltage			-0.3		0.3* VDD	V

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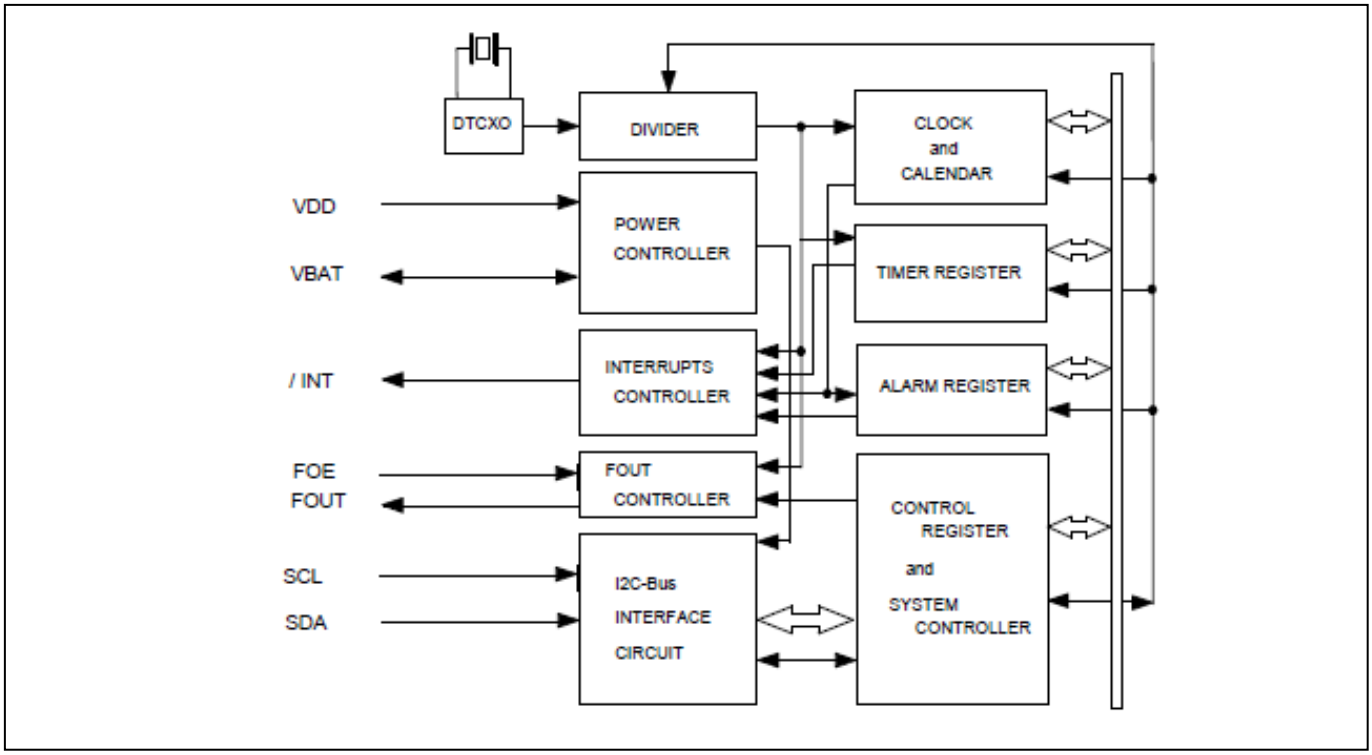
Functional Block Diagram



Functional Description

1. Overview of Functions

1.1 Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

After power-on reset (POR), the time and date are set to 00:00:00 01/01/00 (hh:mm:ss DD/MM/YY) and the Day of the Week register is set to 01.

RT3A integrates an internal crystal and DTXO. Typical accuracy is approximately ±5ppm (equivalent to 13sec/month deviation) for temperature range -40°C to 85°C and ±10ppm (equivalent to 26sec/month deviation) for -40°C to 125°C

1.2 Alarm Function

The device supports alarm that outputs interrupt signals from INT to CPU when the date, day of the week, hour, minute match the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

1.3 Fixed Cycle Timer Function

The device also supports fixed cycle timer interrupt, either by specified second, or specified minute, or a specified period between 244.14us and 32767 minute (22.75days).

1.4 Programmable Square Wave Output

A square wave output enable bit controls square wave output at pin 4. Frequencies are selectable: 1, 1024, 32.768 kHz.

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1.5 Interface with CPU

The RT3A operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed.
Data is read and written via the I2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I2C bus's high-speed mode.

1.6 Temperature Compensation

The device integrates a DTXO which compensates oscillator frequency according to the temperature reading. Temperature compensation interval can be adjusted based on four interval choices.

1.7 Battery Backup

The RT3A supports backup battery switchover function that enhances its operation reliability.

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2. Registers

2.1 Register Table

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read	Write
00	SEC	o	40	20	10	8	4	2	1	P	P
01	MIN	o	40	20	10	8	4	2	1	P	P
02	HOUR	o	o	20	10	8	4	2	1	P	P
03	WEEK	o	6	5	4	3	2	1	0	P	P
04	DAY	o	o	20	10	8	4	2	1	P	P
05	MONTH	o	o	o	10	8	4	2	1	P	P
06	YEAR	80	40	20	10	8	4	2	1	P	P
07	RAM	•	•	•	•	•	•	•	•	P	P
08	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
09	HOUR Alarm	AE	•	20	10	8	4	2	1	P	P
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		•	20	10	8	4	2	1		
0B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
0C	Timer Counter 1	•	•	•	•	2048	1024	512	256	P	P
0D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
0E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET	P	P
0F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	o	o	RESET	P	P
10	SEC	o	40	20	10	8	4	2	1	P	P
11	MIN	o	40	20	10	8	4	2	1	P	P
12	HOUR	o	o	20	10	8	4	2	1	P	P
13	WEEK	o	6	5	4	3	2	1	0	P	P
14	DAY	o	o	20	10	8	4	2	1	P	P
15	MONTH	o	o	o	10	8	4	2	1	P	P
16	YEAR	80	40	20	10	8	4	2	1	P	P
17	TEMP	128	64	32	16	8	4	2	1	P	I
18	Backup Function	o	o	o	o	VDET OFF	SWOFF	BKSMP1	BKSMP0	P	P
19	Not use	o	o	o	o	o	o	o	o	P	I
1A	Not use	o	o	o	o	o	o	o	o	P	I
1B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
1C	Timer Counter 1	•	16384	8192	4096	2048	1024	512	256	P	P
1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
1E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET	P	P
1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	o	o	RESET	P	P

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2.2 Clock Counter (SEC-HOUR)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00, 10	SEC	o	40	20	10	8	4	2	1
01, 11	MIN	o	40	20	10	8	4	2	1
02, 12	HOUR	o	o	20	10	8	4	2	1

Note: 'o' indicates write-protected bits. A zero is always read from these bits

The clock counter counts seconds, minutes, and hours
The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.
*Note with caution that writing no-existent time data may interfere with normal operation of the clock counter.

1. Second Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00, 10	SEC	o	40	20	10	8	4	2	1

This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

2. Minute Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01, 11	MIN	o	40	20	10	8	4	2	1

This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

3. Hour Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02, 12	HOUR	o	o	20	10	8	4	2	1

This hour counter counts from "00" to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

2.3 Calendar Counter (WEEK-YEAR)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03, 13	WEEK	o	6	5	4	3	2	1	0

Note: "o" indicates write-protected bits. A zero is always read from these bits.

Day of the WEEK Counter

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

WEEK	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Day	Data [h]
Write/Read	0	0	0	0	0	0	0	1	Sunday	01h
	0	0	0	0	0	0	1	0	Monday	02h
	0	0	0	0	0	1	0	0	Tuesday	04h
	0	0	0	0	1	0	0	0	Wednesday	08h
	0	0	0	1	0	0	0	0	Thursday	10h
	0	0	1	0	0	0	0	0	Friday	20h
	0	1	0	0	0	0	0	0	Saturday	40h
Write Prohibit	Do not set "1" to more than one day at the same time. Also note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								-	-

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04, 14	DAY	o	o	20	10	8	4	2	1
05, 15	MONTH	o	o	O	10	8	4	2	1
06, 16	YEAR	80	40	20	10	8	4	2	1

Note: 'o' indicates write-protected bits. A zero is always read from these bits

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- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

*Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1. Day Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04, 14	DAY	o	o	20	10	8	4	2	1

- The updating of dates by the date counter varies according to the month setting.
- A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92 or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01,"etc.

DAY	MONTH	Date Update Pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

2. Month Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05, 15	MONTH	o	o	O	10	8	4	2	1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

3. Year Counter

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06, 16	YEAR	80	40	20	10	8	4	2	1

- The year counts from 00, 01, 02 and up to 99, then start again at 00.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as leap year.

2.4 Alarm Registers

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the AIE, AF and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

2.5 Fixed-cycle Timer Control Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B, 1B	Timer Counter 0	128	64	32	16	8	4	2	1
0C, 1C	Timer Counter 1	•	16384	8192	4096	2048	1024	512	256

- These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also used to set the fixed-cycle timer interrupt function.
- When the value in the above fixed-cycle timer control register changes from 001h to 000h, the /INT pin goes to low level and "1" is set to the TF bit to report that a fixed-cycle timer interrupt event has occurred.

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2.6 Extension Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D, 1D	Extension Register (Default)	TEST (o)	WADA (-)	USEL (-)	TE (-)	FSEL 1 (o)	FSEL 0 (o)	TSEL 1 (-)	TSEL 0 (-)

Notes:
1. "o" indicates write-protected bits. A zero is always read from these bits.
2. "-" indicates a default value is undefined.

- This register is used to specify the target for the alarm function or time update interrupt function and to select of set operations such as fixed-cycle timer operations.

1. TEST Bit

This is the manufacturer's test bit. Its value should always be"0."
Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode *Default
	1	Setting prohibited (manufacturer's test bit)

2. WADA (Week Alarm/Day Alarm) Bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies DAY as the comparison for the alarm interrupt function.
Writing a "0" to this bit specifies WEEK as the comparison for the alarm interrupt function.

3. USEL (Update Interrupt Select) Bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.

USEL	Data	Update Interrupts	Auto Reset Time tRTN
Write/Read	0	Second update *Default	500ms
	1	Minute update	7.813ms

4. TE (Timer Enable) Bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset vlaue).
Writing a "0" to this bit specifies stopping of the fixed-cycle timer interrupt function.

5. FSEL0, 1 (FOUT frequency Select 0, 1) Bits

The combination of these two bits is used to set the FOUT frequency.

FSEL0, 1	FSEL 1 (Bit 3)	FSEL 0 (Bit 2)	FOUT Frequency
Write/Read	0	0	32768Hz Output *Default
	0	1	1024Hz Output
	1	0	1Hz Output
	1	1	32768Hz Output

6. TSEL0, 1 (Timer Select 0, 1) Bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four setting can be made).

FSEL0, 1	TSEL 1 (Bit 1)	TSEL 0 (Bit 0)	Source Clock
Write/Read	0	0	4096Hz / Once per 244.14μs
	0	1	64Hz / Once per 15.625ms
	1	0	"Second" update / Once per second
	1	1	"Minute" update / Once per minute

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2.7 Flag Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E, 1E	Flag Register (Default)	o (o)	o (o)	UF (1)	TF (1)	AF (1)	o (o)	VLF (1)	VDET (1)

Notes:
"o" indicates write-protected bits. A zero is always read from these bits.

- This register is used to detect the occurrence of various interrupt events and reliability problems in internal data.

1. UF (Update Flag) Bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when a time update interrupt event has occurred. Once this flag bit's value is "1," its value is retained until a "0" is written to it.

2. TF (Timer Flag) Bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1," its value is retained until a "0" is written to it.

3. AF (Alarm Flag) Bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when an alarm interrupt event has occurred. Once this flag bit's value is "1," its value is retained until a "0" is written to it.

4. VLF (Voltage Low Flag) Bit

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1," its value is retained until a "0" is written to it. When after powering up from 0V, this bit's value is "1".

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Data loss is not detected.
	1	Data loss is detected. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

5. VDET (Voltage Detection Flag) Bit

This flag bit indicates the status of temperature compensation. Its value changes from "0" to "1" when stop the temperature compensation, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it When after powering up from 0V this bit's value is "1".

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	The write access of "1" to this bit is invalid.
Read	0	Temperature compensation is normal.
	1	Temperature compensation is stop detected.

2.8 Control Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F, 1F	Control Register (Default)	CSEL 1 (o)	CSEL 0 (0)	UIE (-)	TIE (-)	AIE (-)	o (o)	o (o)	RESET (-)

Notes:
1. "o" indicates write-protected bits. A zero is always read from these bits.
2. "-" indicates a default value is undefined.

- This register is used to control interrupt event output from the /INT pin and stop/start status of clock and calendar operations.

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1. CSEL0, 1 (Compensation interval Select 0, 1) Bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL0, 1	CSEL 1 (Bit 7)	CSEL 0 (Bit 6)	Compensation Interval
Write/Read	0	0	0.5s *Default
	0	1	2.0s
	1	0	10s
	1	1	30s

2. UIE (Update Interrupt Enable) Bits

When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1." This /INT status is automatically cleared (/INT status changes from low to Hi-Z) 7.8ms after the interrupt occurs.

3. TIE (Timer Interrupt Enable) Bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies of an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1." Up to 7.8ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z)

4. AIE (Alarm Interrupt Enable) Bit

When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is "1." This setting is retained until the AF bit value is cleated to zero. (No automatic cancellation)

Caution:

- The /INT pin is a shared interrupt output pin for three types of interrupts. It outputs the OR'ed result of these interrupt outputs. When an interrupt has occurred (when the /INT pin is at low level), the UF, TF, read AF flags to determine which flag has a value of "1" (this indicates which type of interrupt event has occurred).

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- To keep the /INT pin from changing to low level, write "0" to the UIE, TIE and AIT bits. To check whether an event has occurred without outputting any interrupts via the /INT pin, use software to monitor the value of the UF, TF, and AF interrupt flags.

5. RESET Bit

When this bit is set to "1," values (less than seconds) of the counter in the Clock & Calendar circuitry is reset, and the clock also stops.

RESET bit can be released after receiving an I2C STOP condition or by writing "0" to this bit

2.9 Temperature Data Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	TEMP	128	64	32	16	8	4	2	1

1. Temperature Data Register

This register can begin to read digital temperature data.

The temperature data are updated in an operation timing of the temperature compensation circuit.

2.10 Backup Power Supply Function Register

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	Backup Function	o	o	o	o	VDET OFF	SWOFF	BKSMP 1	BKSMP 0

- This register is a setting register the voltage detection of VDD and built-in MOS switch of anti-countercurrent control.

1. VDETOFF (Voltage Detector OFF) Bit

This bit controls the voltage detection circuit of the main power supply VDD.

2. SWOFF (Switch OFF) Bit

This bit controls the internal P-MOS switch for preventing back flow.

3. BKSMP1, BKSMP0 (Backup Mode Sampling Time) Bit

This bit controls the operation time when to be intermittently driven the VDD voltage detection.

The duration of VDD voltage detection is controlled by BKSMP1 and BKSMP0. It can be set to 2ms, 16ms, 126ms or 256ms. VDD voltage detection is finished at the end of the detection period.

VDD Detector	VDETOFF	SWOFF	BKSMP1	BKSMP0	VDET3 Sampling Operation Period	Pch-Switch ON/OFF	Remarks
ON	0	X	0	0	2ms	2ms OFF	VDETOFF: 0, BKSMP1: 0, BKSMP1: 0 default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256msOFF	
OFF	1	0	X	X	OFF	ON	VDD and VBAT short circuit via Pch-switch
		1	X	X	OFF	OFF	VDD connected via diode to VBAT

X = Don't Care.

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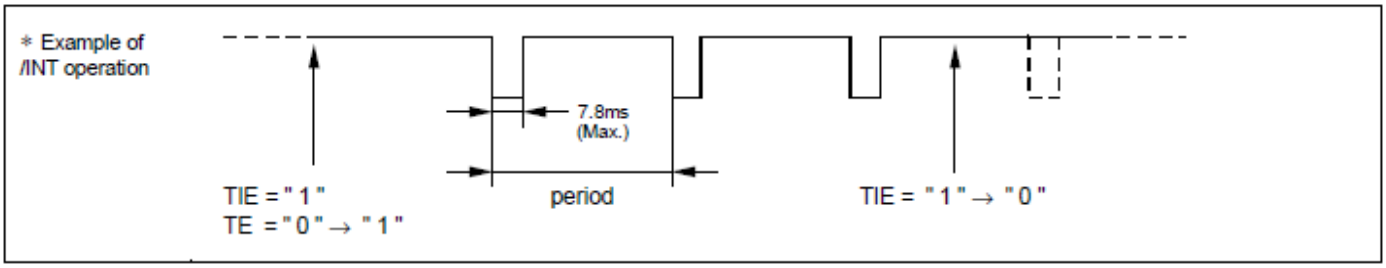
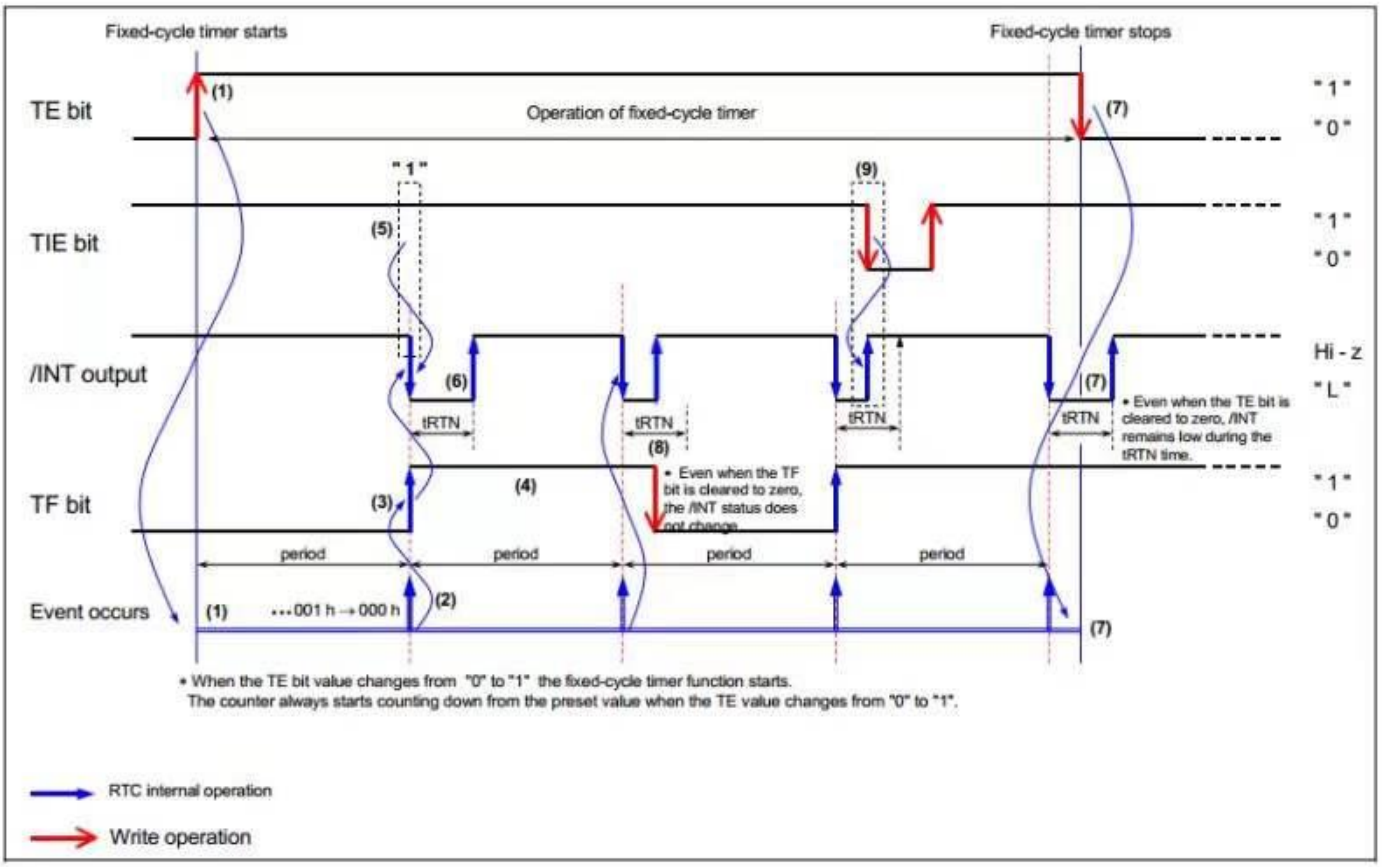
2.11 Fixed-Cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14μs and 32767 minutes.

When an interrupt event is generated, the /INT pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1." Up to 7.8ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).





(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 0001h to 0000h, an interrupt event occurs.
*After the interrupt event that occurs when the count value changes from 0001h to 0000h, the counter automatically reloads the preset value and again starts to count down, (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleated to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low.

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*If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
*/INT is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /INT pin is set to Hi-Z status.
*When /INT = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

(8) /INT changes from Low to High immediately after TF bit changes from "1" to "0"

(9) When /INT= low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit changes from "1" to "0".

2.12 Related Registers for Time Interrupt Functions

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B, 1B	Timer Counter 0	128	64	32	16	8	4	2	1
0C, 1C	Timer Counter 1	•	•	•	•	2048	1024	512	256
0D, 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E, 1E	Flag Register	o	o	UF	TF	AF	EVF	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	EIE	o	RESET

Notes:
1. "o" indicates write-protected bits. A zero is always read from these bits.
2. Bits marked with "•" are RAM bits that can contain any value and are read/write accessible.

- Before entering settings for operations, we recommend writing a "0" to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.
- When RESET bit value is "1" the time update interrupt function operates only partially. (Operation continues if the source clock setting is 4096Hz. Otherwise, operation is stopped.)
- When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – B to C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1. TSEL0, 1 (Timer Select 0, 1) Bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL0, 1	TSEL 1 (Bit 1)	TSEL 0 (Bit 0)	Source Clock	Auto Reset Time tRTN	Effects of RESET Bits
Write/Read	0	0	4096Hz / Once per 244.14μs	122μs	-
	0	1	64Hz / Once per 15.625ms	7.8125ms	*Does not operate when the RESET bit value is "1."
	1	0	"Second" update / Once per second	7.8125ms	
	1	1	"Minute" update / Once per minute	7.8125ms	

Notes:
1. The /INT pin's auto reset time (tRNT) varies as shown above according to the source clock setting.
2. When the source clock has been set to "second update" or "minute update," the timing of both countdown and interrupts is coordinated with the clock update timing.

2. Fixed-cycle Timer Control Register (Reg – B to C)

This register is used to set the default (preset) value for the counter. Any count value from 1 (0001h) to 32767 (7FFF) can be set. The counter counts down based on the source clock's period, and when the count value changes from 0001h to 0000h, the TF bit value becomes "1."

The countdown that starts when the TE bit value changes from "0" to "1" always begins from the present value. Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

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Address C Timer Counter 1								Address B Timer Counter 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
•	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

3. TE (Timer Enable) Bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.

TE	Data	Description
Write/Read	0	Stop fixed-cycle timer interrupt function.
	1	Starts fixed-cycle timer interrupt function. *The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4. TF (Timer Flag) Bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1," its value is retained until a "0" is written to it.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection. *Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z)
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero)

5. TIE (Timer Interrupt Enable) Bit

When a fixed-cycle timer interrupt event occurs (When the TF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

TIE	Data	Description
Write/Read	0	1. When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2. When a fixed-cycle timer interrupt event occurs, an interrupt signal is canceled (/INT status changes from low to Hi-Z). *Even when the TIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1." UP to 7.8ms after the interrupt occurs, the /INT status is automatically cleated (/INT status changes from low to Hi-Z).

2.13 Fixed-Cycle Timer Interrupt Interval (Example)

Timer Counter Setting	Source Clock			
	4096Hz TSEL1, 0 = 0, 0	64Hz TSEL1, 0 = 0, 1	"Second" Update TSEL1, 0 = 1, 0	"Minute" Update TSEL1, 0 = 1, 1
0	-	-	-	-
1	244.14µs	15.625ms	1s	1min
2	488.28µs	31.25ms	2s	2min
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
41	10.010ms	640.63ms	41s	41min
205	50.049ms	3.203s	205s	205min
410	100.10ms	6.406s	410s	410min
2048	500.00ms	32.000s	2048s	2048min
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
32767	7.999735s	511.9844s	32767s	22.75486days

- Time Error in Fixed-cycle Timer

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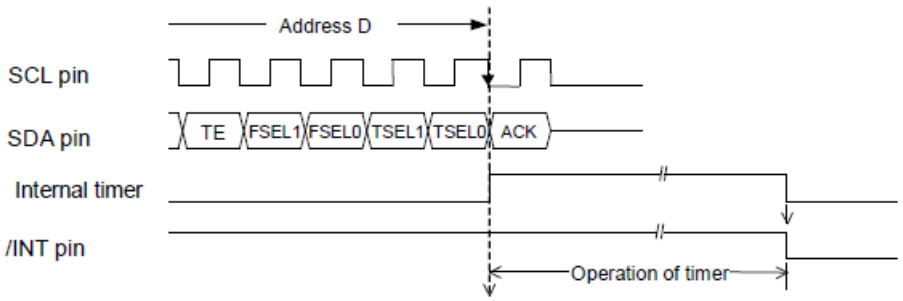
A time error in the fixed-cycle timer will produce a positive or negative time period error in the selected source clock. The fixed-cycle timer's time is within the following range relative to the time setting.

Fixed-cycle timer's time setting (*) – source clock period) to (timer's time setting)
*The timer's time setting = source clock period X timer counter's division value.

*The time actually set to the timer is adjusted by adding the time describes above to the communication time for the serial data transfer clock used for the setting.

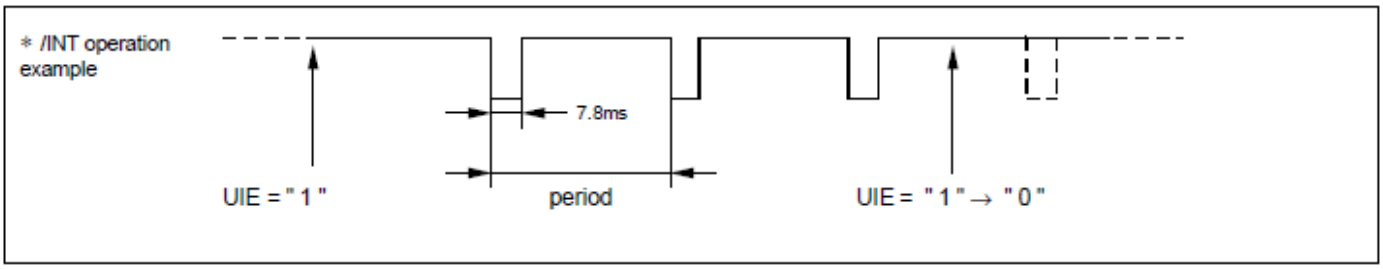
2.14 Fixed-Cycle Timer Start Timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



2.15 Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1." This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) 7.8ms (fixed value) after the interrupt occurs.



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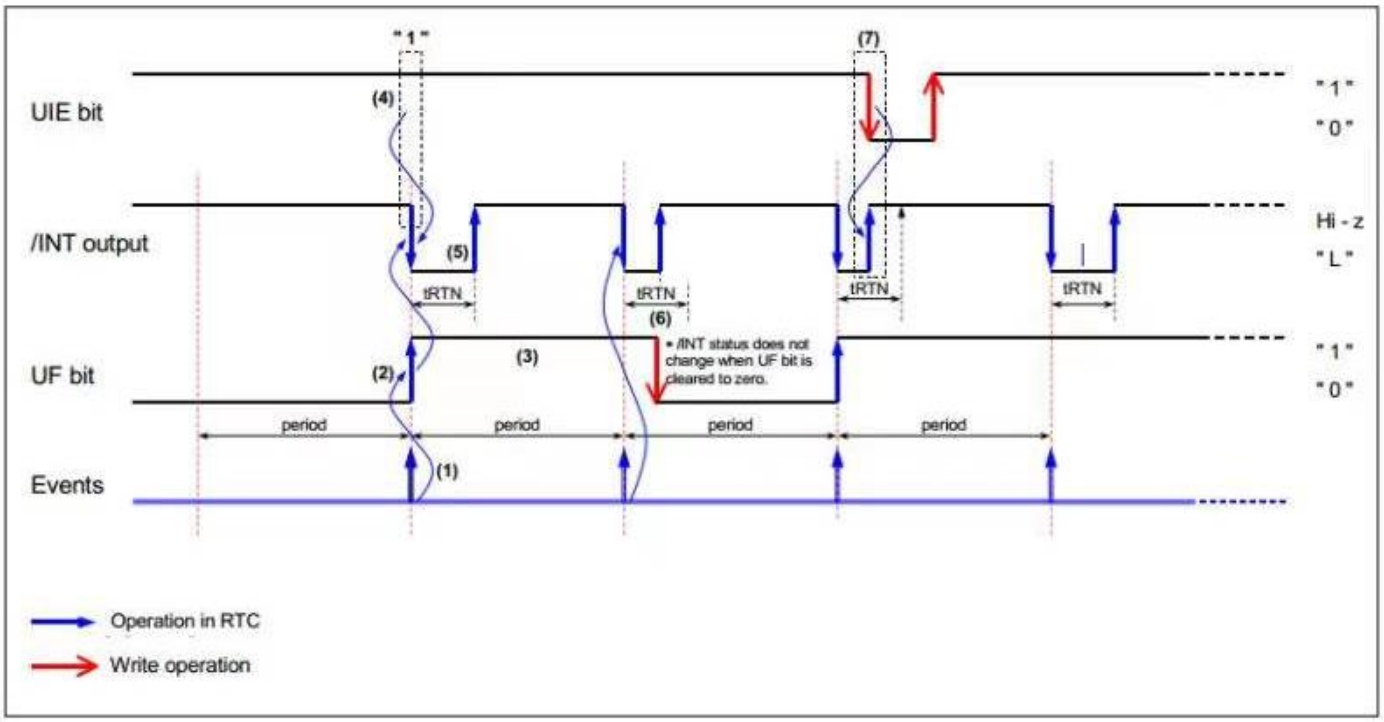

(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
(2) When a time update interrupt event occurs, the UF bit value becomes "1."
(3) When the UF bit value is "1" its value is retained until it is cleared to zero.
(4) When a time update interrupt occurs, /INT pin output is low if UIE = "1."
*If UIE = "0" when a timer update interrupt occurs, the /INT pin status remains Hi-Z.
(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.1825ms for time update interrupts) after which it is automatically cleared to Hi-Z.
*/INT pin output goes low again when the next interrupt event occurs.
(6) When UF bit value changes from "1" to "0", /INT changes from low to high.
(7) When /INT=low, /INT pin status changes from low to Hi-Z as soon as UIE bit changes from "1" to "0"

2.16 Related Registers for Time Update Interrupt Function

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D, 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E, 1E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	o	o	RESET

Notes:
1. "o" indicates write-protected bits. A zero is always read from these bits.

- Before entering settings for operations, we recommend writing a "0" to the UIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.
- When the RESET bit value is "1" time update interrupt events do not occur.
- Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1. USEL (Update Interrupt Select) Bit

This bit used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

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USEL	Data	Description
Write/Read	0	Selects “second update” (once per second) as the timing for generation of interrupt events.
	1	Selects “minute update” (once per minute) as the timing for generation of interrupt events.

2. UF (Update Flag) Bit

Once it has been set to “0,” this flag bit value changes from “0” to “1” when a time update interrupt event occurs. When this flag bit = “1” its value is retained until a “0” is written to it.

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection. *Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z)
	1	This bit is invalid after a “1” has been written to it.
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

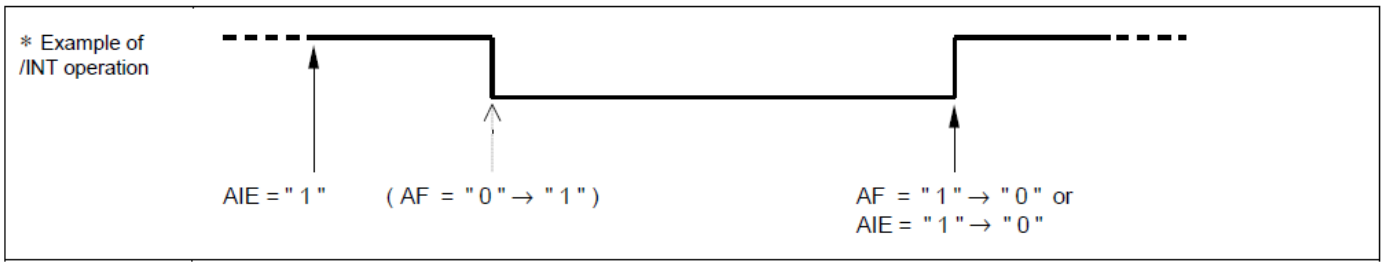
3. UIE (Update Interrupt Enable) Bit

When a time update interrupt event occurs (UF bit value changes from “0” to “1”), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z).

UE	Data	Description
Write/Read	0	1. Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z). 2. Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z). *Even when the UIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = “L”).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is “1.” Up to 7.8ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

2.17 Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to “1” and the /INT pin goes to low level to indicate that an event has occurred.



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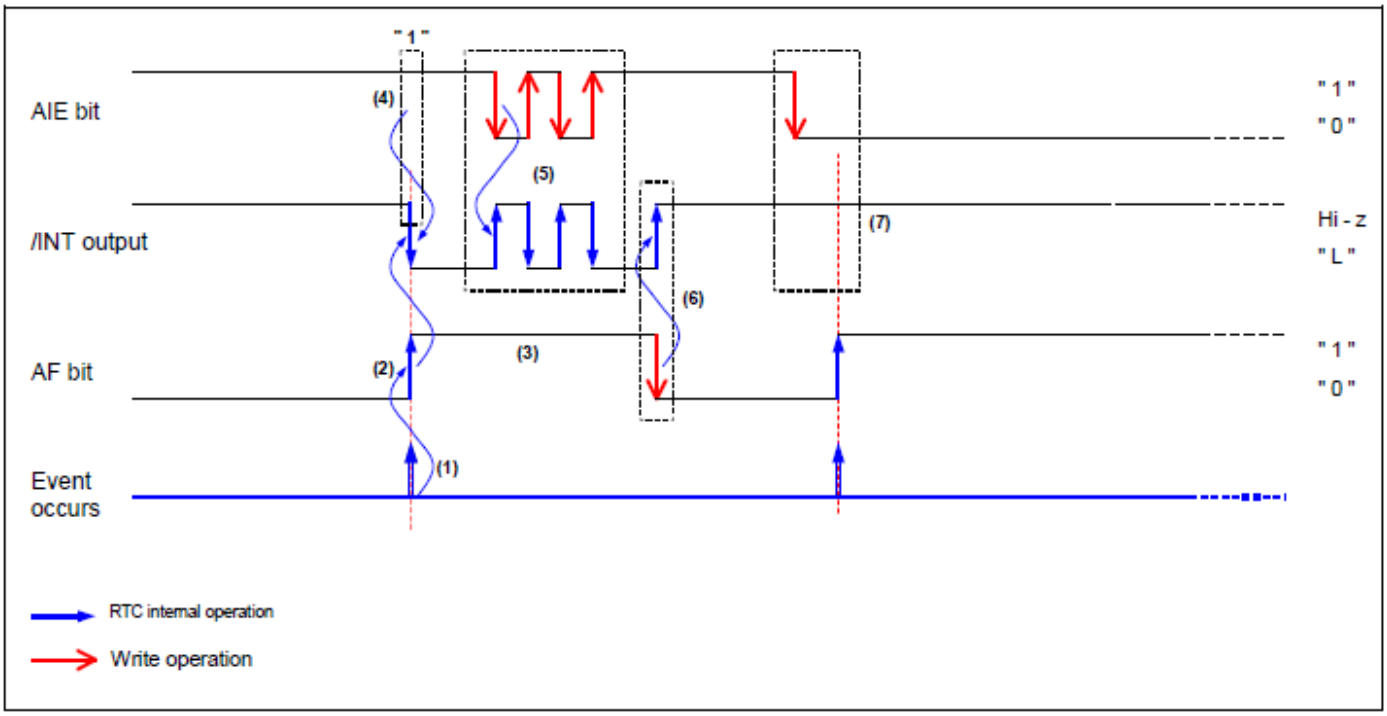

(1) The hour, minute, date or day is set in advance along with the WADA bit, and when the setting matches the current time an alarm interrupt event occurs.
*Note: Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
(2) When a time update interrupt event occurs, the AF bit values becomes "1."
(3) When the AF bit = "1," its value is retained until it is cleared to zero.
(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low.
*When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared bit the AF bit or AIE bit
(5) If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.
(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.
(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

2.18 Related Registers

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01, 12	MIN	o	40	20	10	8	4	2	1
02, 13	HOUR	o	o	20	10	8	4	2	1
03, 14	WEEK	o	6	5	4	3	2	1	0
04, 15	DAY	o	o	20	10	8	4	2	1
08, 18	MIN Alarm	AE	40	20	10	8	4	2	1
09, 19	HOUR Alarm	AE	•	20	10	8	4	2	1
0A, 1A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D, 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E, 1E	Flag Register	o	o	UF	TF	AF	o	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	o	o	RESET

Notes:
1. "o" indicates write-protected bits. A zero is always read from these bits.
2. Bits marked with "•" are RAM bits that can contain any value and are read/write accessible.

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- Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
- When the RESET bit value is "1" alarm interrupt events do not occurs.
- When the alarm interrupt function is not being used, the Alarm registers (Reg – 8 to A) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
- When the AIE bit value is "1" and the Alarm registers (Reg – 8 to A) is being used as a RAM register, /INT may be changed to low level unintentionally.

1. WADA (Week Alarm/Day Alarm) Bit

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write/Read	0	Sets WEEK as target of alarm function (DAY setting is ignored).
	1	Sets DAY as target of alarm function (WEEK setting is ignored).

2. Alarm Registers

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.
In the WEEK alarm/Day alarm register (Reg -A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).
When the setting made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1." At that time, if the AIE bit value has already been set to "1," the /INT pin goes low.

*The register that "1" was set to "AE" bit, doesn't compare alarm.
Example - Write 80h (AE = "1") to the WEEK Alarm/DAY Alarm register (Reg - A): Only the hour and minute setting are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets. As a result, alarm occurs if only an hour and minute accords with alarm data.
*If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

3. AF (Alarm Flag) Bit

When this flag bit value is already set to "0," occurrence of an alarm interrupt event changes it to "1." When this flag bit value is "1," its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection. *Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleated to zero)

4. AIE (Alarm Interrupt Enable) Bit

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

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AIE	Data	Description
Write/Read	0	1. When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2. When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). *Even when the AIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). *When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is "1." This value is retained (not automatically cleared) until the AF bit is cleared to zero.

2.19 Example of Alarm Setting

Example of alarm setting when "WEEK" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg - A								Reg - 9	Reg - 8
	Bit 7 AE	Bit 6 S	Bit 5 F	Bit 4 T	Bit 3 W	Bit 2 T	Bit 1 M	Bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00AM *Minute value is ignored	0	0	1	1	1	1	1	0	07h	80h ~ FFh
Every Saturday and Sunday, for 30 minutes each hour *Hour value is ignored	0	1	0	0	0	0	0	1	80h ~ FFh	30h
Every day, at 6:59PM	0	1	1	1	1	1	1	1	18h	59h
	1	X	X	X	X	X	X	X		

X: Don't Care.

Example of alarm setting when "DAY" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A								Reg - 9	Reg - 8
	Bit 7 AE	Bit 6 •	Bit 5 20	Bit 4 10	Bit 3 08	Bit 2 04	Bit 1 02	Bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00AM *Minute value is ignored	0	0	0	0	0	0	0	1	07h	80h ~ FFh
15th of each month, for 30 minutes each hour *Hour value is ignored	0	0	0	1	0	1	0	1	80h ~ FFh	30h
Every day, at 6:59PM	1	X	X	X	X	X	X	X	18h	59h

X: Don't Care.

2.20 Temperature Compensation Function

Frequency compensation value for the oscillation circuit which matched with a value of a built-in temperature sensor by a shipment inspection process of our company is set by built-in memory. Oscillation frequency for a temperature change is compensated.
This function cannot stop with the high operation voltage than temperature compensation operation voltage (VTEM).

Related registers for temperature compensation function

Address [h]	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	o	o	RESET

- CSEL1, CSEL0 Bit (Compensation Interval Select 1, 0)

This bit sets an interval of a temperature compensation operation.
Consumption electric currents decrease by setting an operation interval of a temperature compensation circuit for long time.
CSEL1, 0 is set at the time of initial power supply injection by ("0", "1").

CSEL 1	CSEL 0	Compensation Interval
0	0	0.5s
0	1	2.0s
1	0	10s
1	1	30s

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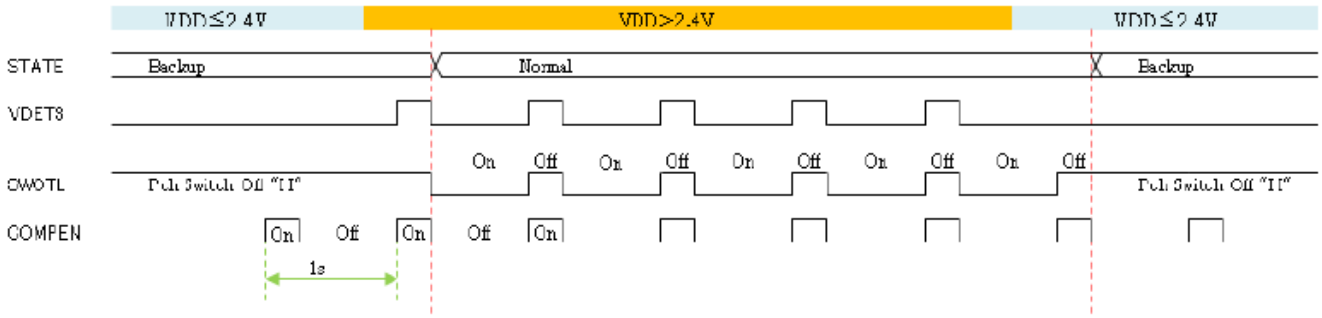
Even if the power supply voltage falls than VTEM and a VDET bit is set to "1," a temperature compensation operation is performed afterwards when rose up the power supply voltage than VETM.

2.21 Battery Backup Function

It consists of the power-source detector "VDET" which detects the power down of the main power source "VDD," and built-in MOS switches located between the main power-source pin "VDD" and the backup power supply pin "VBAT."
In turning off a MOS switch according to the supply-voltage detection result of VDET, when a drive power source changes to VDD OFF → VBAT (it shifts to a backup operation from a normal operation), it becomes possible to prevent a reverse-current (VBAT → VDD) of an electric current.

Power Switching Control



- BACKUP State

PMOS switch is turned off at all times. Voltage detection VDET3 is responsible for monitoring every 1sec.
This state will be selected at cold start. Make the voltage detection for the first time in 1sec after since it was powered on VDD pin.
Until voltage detection for the first time, VBAT is charged in the forward current of the PMOS switch.
In this state, the (VDET3 = L → H), main power supply (VDD) shifts to the NORMAL state of the drive state when it detects a rise VDET level. Return of the main power supply is detected, the internal voltage supply of the RTC will transition to NORMAL state.

- NORMAL State

PMOS switch is turned off in every 1sec, power drop is detected in the off timing of the switch.
OFF time of the switch can be selected in the register.
Drop of the main power supply is detected, an internal power supply voltage of the RTC will be backed up state transitions.

Functions available during battery backup state.
When operating in the backup, please VDD = VSS = 0V.

Function	Available/Not Available	Remarks
Interface	Not Available	Interface circuit cannot operate.
Clock Calendar	Available	The same as the main power supply operation.
Alarm Interrupt	Available	You cannot use the interrupt output function.
Timer Interrupt	Available	You cannot use the interrupt output function.
Time Update Interrupt	Available	You cannot use the interrupt output function.
Clock Output	Not Available	There is not output from terminal Fout pin.
VBAT Voltage Drop Detection	Available	The same as the main power supply operation.
Temperature Compensation	Available	This function is Available when VBAT supply voltage is more than 2.0V

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3. Application I/II/III Schematics

3.1 Application I: Not Use a Backup Circuit

VDD connects to VBAT directly. In this case, VDD supplies power to RTC. Set the VDETOFF bit in the register 0x18 VDETOFF = 1.

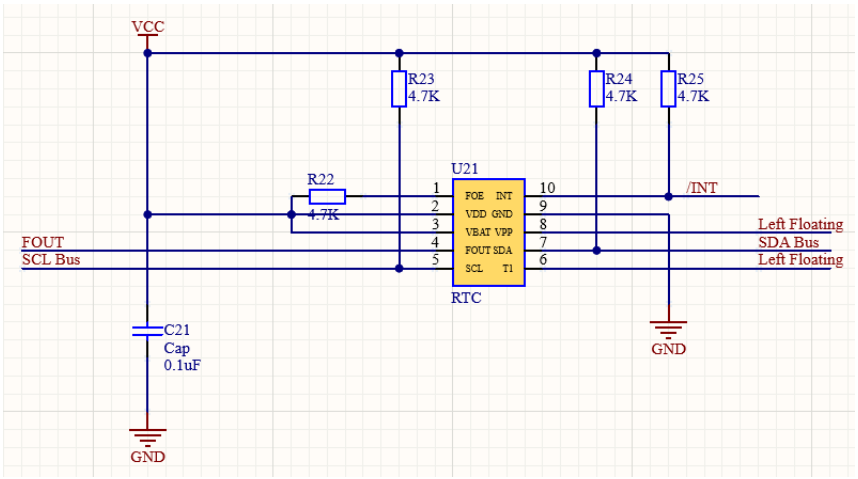

Figure 1. Application I schematic

3.2 Application II: Use a Coin Cell Battery as Backup

Turn on the VDD detector application:

1) Set VDETOFF = 0, SWOFF = 0 in Reg 0x18, R15 = 100Ω (min).
2) Diodes D11 & D12 are required, of which Vf is about 0.2V
3) Diodes BAT54WSQ-7-F is recommended for D11/D12
4) The recommended Cap C14 is 1uF

PS: the maximum duration of leakage current from VBAT to VDD is 1 second when VDD = 0V

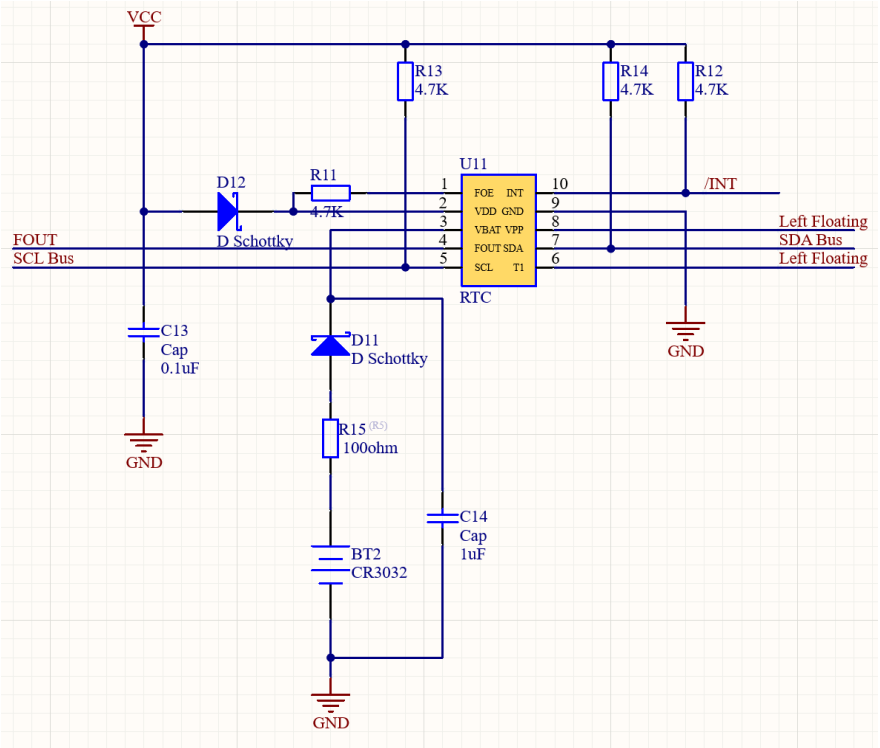

Figure 2. Application II Schematic

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3.3 Application III: Use a Rechargeable Battery or an EDLC as Backup

Turn on the VDD detector application:

1) Set VDETOFF = 0, SWOFF = 0 in Reg 0x18, R35 = 100Ω (min).
2) Diodes D31 is required, of which Vf is about 0.2V
3) Diodes BAT54WSQ-7-F is recommended for D31
4) The recommended Cap C34 is 1uF

PS: the maximum duration of leakage current from VBAT to VDD is 1 second when VDD = 0V

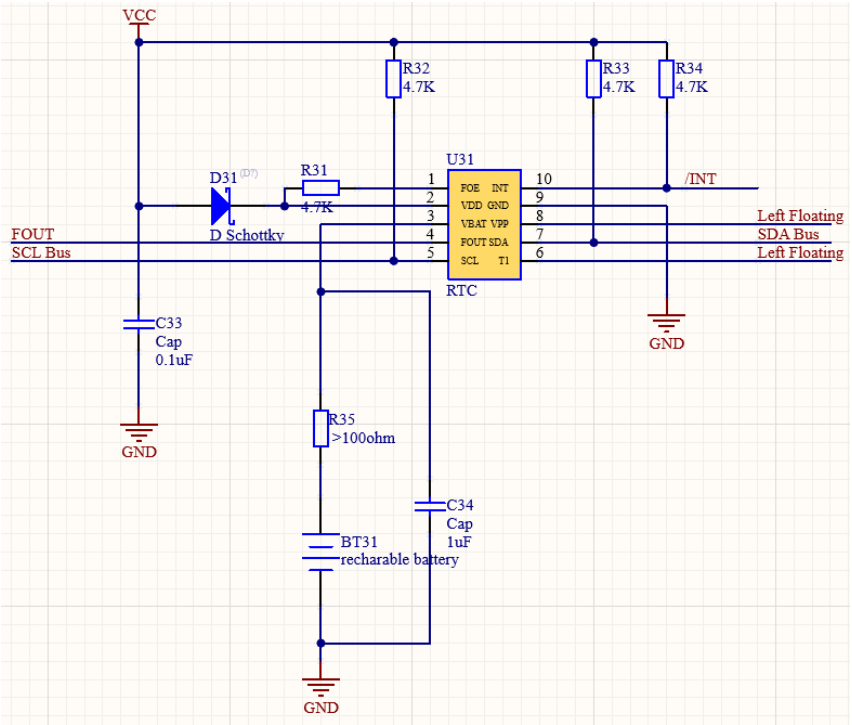

Figure 3. Application III Schematic

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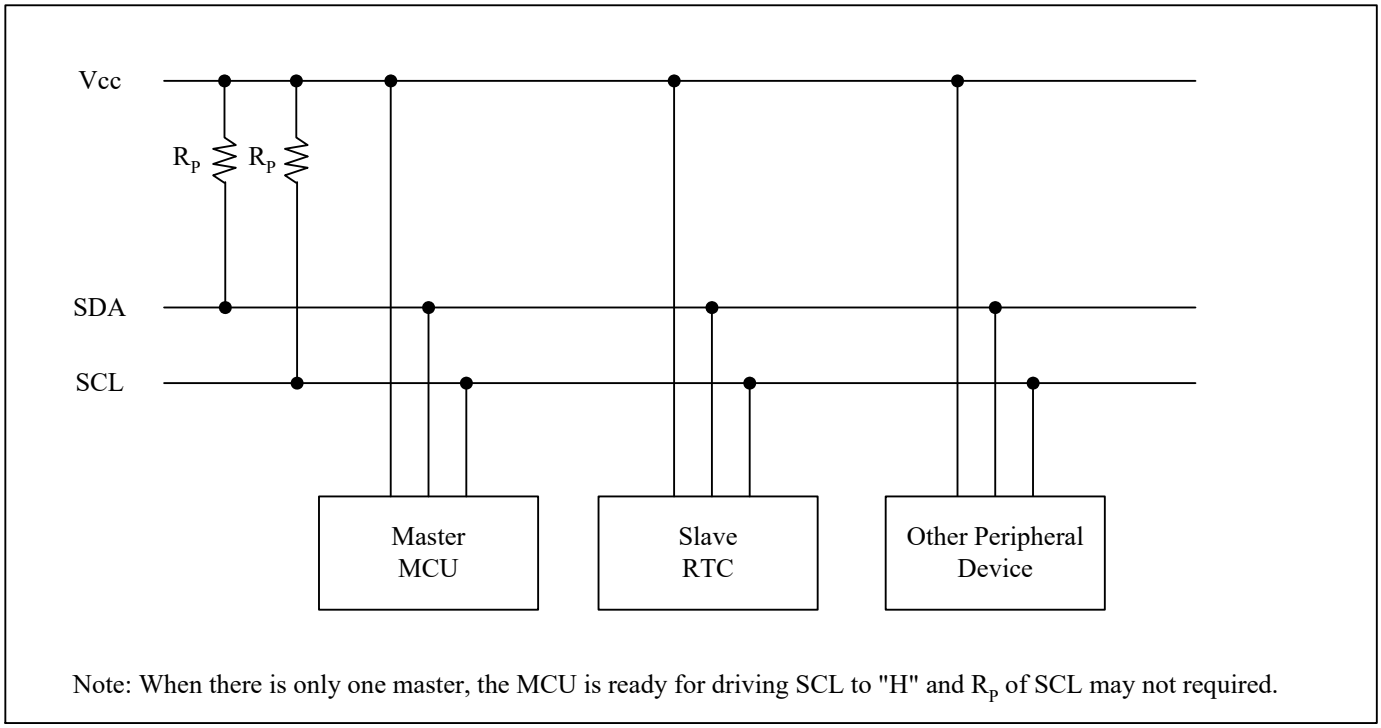
4. I2C Bus Interface

4.1 Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

4.2 System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VCC line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_P of SCL may not required.

Figure 4. System configuration

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Starting and Stopping I2C Bus Communications

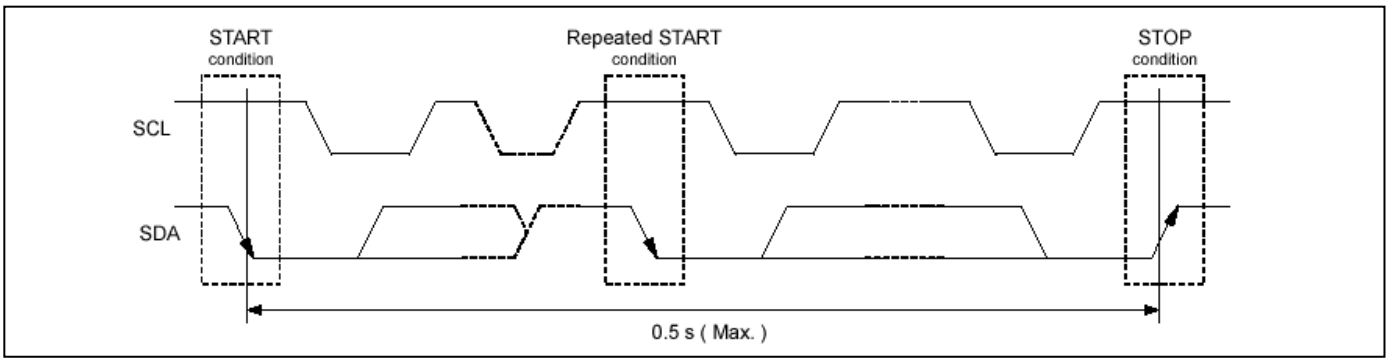


Figure 5. Starting and stopping on I²C bus

1) START Condition, Repeated START Condition, and STOP Condition

a) START Condition

SDA level changes from high to low while SCL is at high level

b) STOP Condition

SDA level changes from low to high while SCL is at high level

c) Repeated START Condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

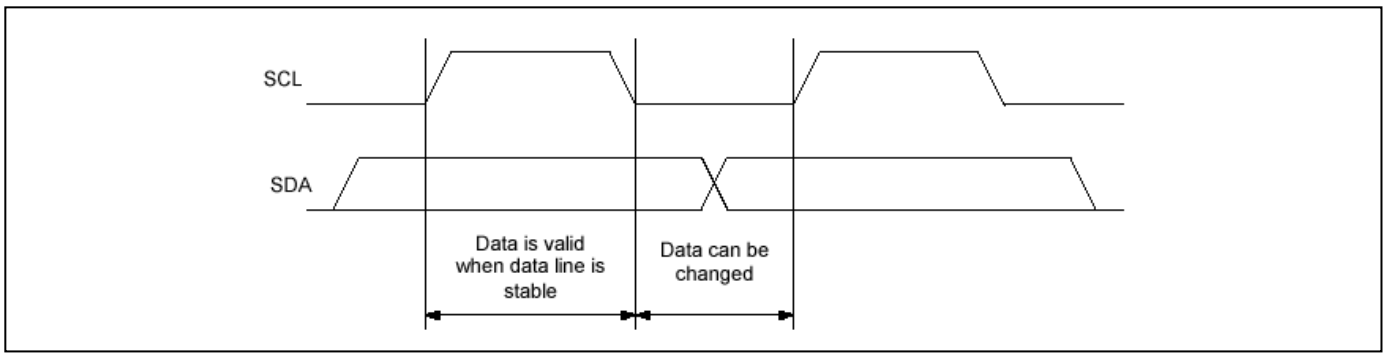
a) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.

The receiver (receiving side) captures data while the SCL line is at high level.



***Note:** with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

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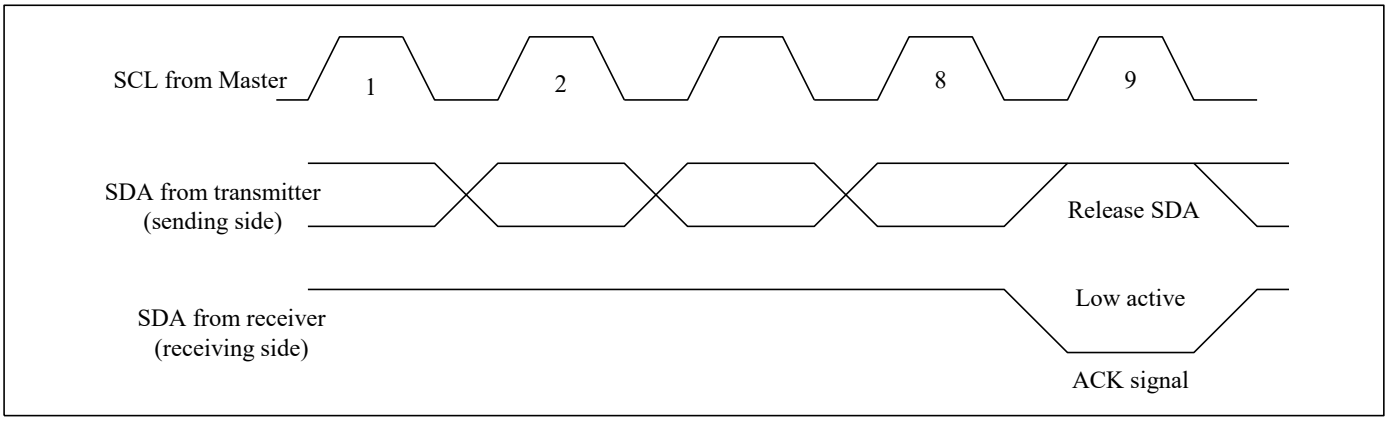
b) Data Acknowledge Response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

4.3 Slave Address

The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. See table for the details.

An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	61 h	0	1	1	0	0	0	0	1 (= Read)
Write	60 h								0 (= Write)

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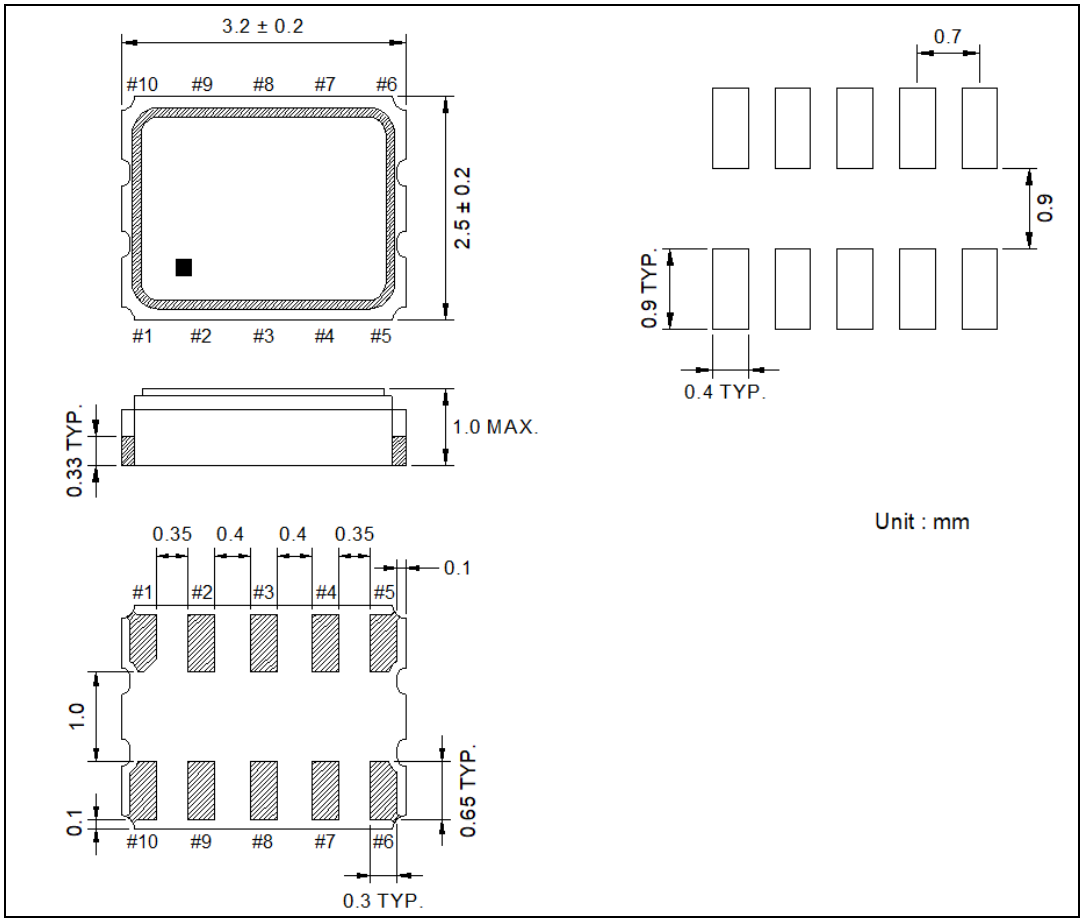
Packaging Mechanical



For latest package info.
Please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Numbers	Package Code	Package Description
RT3A3241N3	Ceramic 3225	Temperature compensated RTC Module in 3225 ceramic package -40°C to +85°C +/-3.5ppm
RT3A3240N3	Ceramic 3225	Temperature compensated RTC Module in 3225 ceramic package -40°C to +85°C +/-5ppm
RT3A3241Q3	Ceramic 3225	Automotive grade temperature compensated RTC Module in 3225 ceramic package -40°C to +85°C +/-3.5ppm
RT3A3240Q2	Ceramic 3225	Automotive grade temperature compensated RTC Module in 3225 ceramic package -40°C to +105°C +/-8ppm
RT3A3240Q1	Ceramic 3225	Automotive grade temperature compensated RTC Module in 3225 ceramic package -40°C to +125°C +/-10ppm

Notes:
1. Q = Automotive Compliant
2. ***Pb-free**
3. ***RoHS Compliant**
4. ***HF-Halogen Free**
5. ***REACH Compliant**
6. ***AEC-Q104 Compliant**
7. ***MSL: Level 1**

*** Please contact Diodes for availability.**

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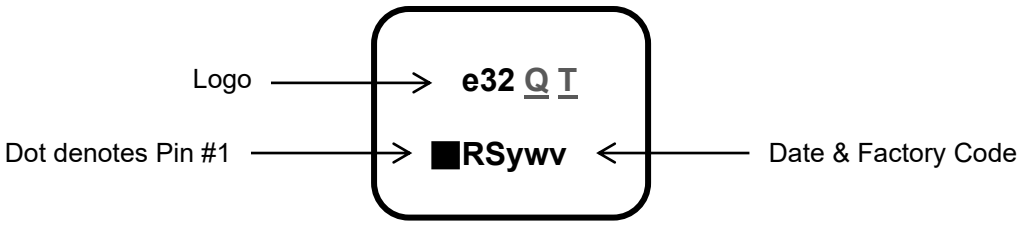
Marking

Part Numbers	Marking Detail
RT3A3241N3	e32N3 ■R1ywv
RT3A3240N3	e32N3 ■R0ywv
RT3A3241Q3	e32Q3 ■R1ywv
RT3A3240Q2	e32Q2 ■R0ywv
RT3A3240Q1	e32Q1 ■R0ywv



32: 32.768 kHz

Q:
Q= Automotive
N= Non-Automotive

T: Temperature Range
1= -40~125°C
2= -40~105°C
3= -40~85°C

R: RT Series

S: Serial Number

y: Year Code (last digit of year)

w: Week Code

v: Factory Code

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