Agilex™ 7 F-Series and I-Series Known Issue List

Online Version
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Contents

1. About this Document

This document provides information about known issues affecting the Agilex™ 7 F-Series and I-Series production devices.

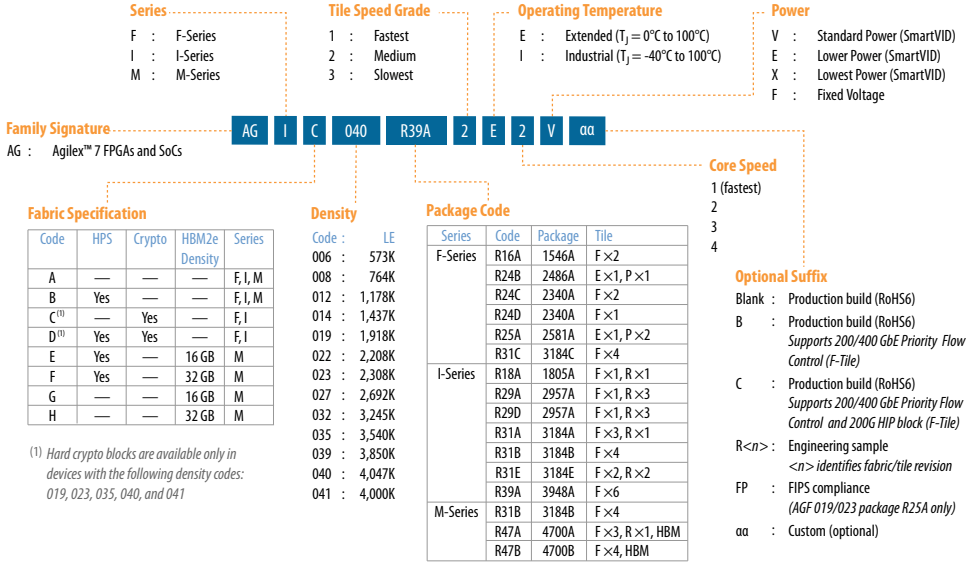
Currently, this document covers the following Ordering Part Numbers (OPNs) of the Agilex 7 F-Series and I-Series production devices:

Table 1. Agilex 7 F-Series and I-Series Production Devices

Agilex 7 F-Series	Agilex 7 I-Series
AGF*x*006*xxxxxxx*	AGI*x*019*xxxxxxx*
AGF*x*008*xxxxxxx*	AGI*x*022*xxxxxxx*
AGF*x*012*xxxxxxx*	AGI*x*023*xxxxxxx*
AGF*x*014*xxxxxxx*	AGI*x*027*xxxxxxx*
AGF*x*019*xxxxxxx*	AGI*x*035*xxxxxxx*
AGF*x*022*xxxxxxx*	AGI*x*040*xxxxxxx*
AGF*x*023*xxxxxxx*	AGI*x*041*xxxxxxx*
AGF*x*027*xxxxxxx*	

Figure 1. Agilex 7 Ordering Part Number (OPN) Decoder

Use this OPN Decoder to determine your device variant.



This document includes:

- Altera®-specific known issues for the Agilex 7 F-Series and I-Series production devices.
- Arm* Cortex*-A53 MPCore processor and CoreSight* errata that applies to the HPS.

For known issues affecting the Agilex 7 F-Series and I-Series ES devices, refer to the *Agilex 7 F-Series and I-Series ES Device Errata and User Guidelines* on the Resource and Documentation Center (RDC) web page.

Related Information

Agilex 7 F-Series and I-Series ES Device Errata and User Guidelines

2. Known Issue List for Agilex 7 Devices

This section lists the known issues for the Agilex 7 production devices. Each listed issue has an associated status that identifies any planned fixes.

Table 2. Device Issues

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
FPGA				
F-Tile				
200G/400G Ethernet Mode Does Not Support Port-Based Priority Flow Control on page 13	Agilex 7 production devices with no suffix (blank) OPN	Agilex 7 production devices with "B" and "C" suffix OPNs	N/A	N/A
The F-Tile Ethernet 200G Hard IP block is de-featured and cannot be used in production devices with OPNs that have no suffix (blank) or "B" suffix on page 14	Agilex 7 production devices with no suffix (blank) or "B" suffix OPNs	Agilex 7 production devices with "C" suffix OPN	N/A	N/A
The Deterministic Latency Feature supports on E200 block Six of Eight FGT Channels on page 15	Agilex 7 production devices with "C" suffix OPN shipped in 2024	Agilex 7 production devices with "C" suffix OPN shipped in 2025 or later	N/A	N/A
FHT TX EOJ Spec Compliance Issue on page 16	Agilex 7 production devices manufactured before 2024	Devices manufactured in 2024 and beyond support improved FHT Transceiver EOJ performance and are fully compliant with published specifications.	N/A	N/A
Requirement for F-Tile Devices which are Powered and Unconfigured on page 17	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
FGT PAM4 Compliance Support on page 18	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	Quartus® Prime Pro Edition software version 25.1.1	N/A	N/A
FGT Transceivers Do Not Support Direct EXTEST JTAG Instruction in Boundary Scan Test on page 19	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile: Unsuccessful TX Equalization on page 20	Agilex 7 production devices	None	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
	(AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)			
Link May Not Downgrade With Corrupt Lanes (F-Tile) on page 22	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
Occasional Equalization Timeout or PCIe Link Training Failure to Achieve Expected Link Speed during Link Disable, Hot Reset, and Speed Change on page 23	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
Link Fault Detection window of the F-Tile Ethernet Hard IP in 10GE-1 or 25GE-1 mode on page 24	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
FHT PMA Transmitter-to-Receiver Internal Serial Loopback operation for error-free BER results on page 25	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile Ethernet Hard IP rst_tx_stats and rst_rx_stats register bits might not function correctly on page 26	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile Ethernet Hard IP force_rf register bit might not function correctly on page 27	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile Ethernet Hard IP tx_pause_request register bit might not function correctly on page 28	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile Ethernet Hard IP PTP statistics might not clear correctly on page 29	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile Ethernet Hard IP unable to achieve 100% throughput with some variants on page 30	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
F-Tile 400G Ethernet Hard IP RX Priority Flow Control Issue on page 31	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
F-Tile Ethernet Hard IP Bidirectional Link Fault Signaling Issue on page 32	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	Quartus Prime Pro Edition software version 25.1.1	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
F-Tile SDI II IP and F-Tile PMA/FEC Direct PHY IP with "SDI" configuration rule are not of production quality on page 33	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
F-Tile HDMI IP and F-Tile PMA/FEC Direct PHY IP with "HDMI" configuration rule are not of production quality on page 34	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
Ethernet Auto-Negotiation and Link Training (AN/LT) designs on F-Tile FGT may not link up when using Quartus Prime Pro Edition software version 25.1.1 and 25.3 on page 35	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
IEEE 802.3-2022 50GBASE-KR compliance testing instability during Link Training (LT) on page 36	Agilex 7 production devices (AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
R-Tile				
Gen3/Gen4 link might be established without successfully performing Transmit Equalization (TX EQ) on page 37	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxx*)	None	N/A	N/A
Link may not downgrade with corrupt lanes on page 39	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxx*)	None	N/A	N/A
Malformed TLP incorrectly flagged as ECRC error on page 40	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxx*)	None	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
Assertion of PERST / warm reset during the Functional Level Reset results in PCIe Link Failure on page 41	Agilex 7 production devices (AGI*x*019R18A*xxxxx*) (AGI*x*023R18A*xxxxx*) (AGI*x*022R29A*xxxxx*) (AGI*x*027R29A*xxxxx*) (AGI*x*022R31A*xxxxx*) (AGI*x*027R31A*xxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	None	N/A	N/A
No Support for Page Request Services in Port 2 and Port 3 of 4x4 Configuration on page 42	Agilex 7 production devices (AGI*x*019R18A*xxxxx*) (AGI*x*023R18A*xxxxx*) (AGI*x*022R29A*xxxxx*) (AGI*x*027R29A*xxxxx*) (AGI*x*022R31A*xxxxx*) (AGI*x*027R31A*xxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	None	N/A	N/A
Multiple Fatal Error Messages on page 43	Agilex 7 production devices (AGI*x*019R18A*xxxxx*) (AGI*x*023R18A*xxxxx*) (AGI*x*022R29A*xxxxx*) (AGI*x*027R29A*xxxxx*) (AGI*x*022R31A*xxxxx*) (AGI*x*027R31A*xxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	None	N/A	N/A
PCIe x4 cores may report Uncorrectable Fatal Error or Malformed TLP on page 44	Agilex 7 production devices (AGI*x*019R18A*xxxxx*) (AGI*x*023R18A*xxxxx*) (AGI*x*022R29A*xxxxx*) (AGI*x*027R29A*xxxxx*) (AGI*x*022R31A*xxxxx*) (AGI*x*027R31A*xxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	None	N/A	N/A
Receiver Errors logged during back-to-back Secondary Bus Resets (SBR) operations when running at Gen 2 speed on page 45	Agilex 7 production devices (AGI*x*019R18A*xxxxx*) (AGI*x*023R18A*xxxxx*) (AGI*x*022R29A*xxxxx*) (AGI*x*027R29A*xxxxx*) (AGI*x*022R31A*xxxxx*) (AGI*x*027R31A*xxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	None	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
R-Tile Digital Temperature Sensor Readings on page 46	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*)	None	N/A	N/A
R-Tile PCIe - LCRC Error/ Malformed TLP on page 47	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxxx*)	Quartus Prime Pro Edition release 24.3.1	N/A	N/A
R-Tile PIPE-Direct - rxdatavalid Signal Unexpected Toggling After P1 to P0 Transition on page 49	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGI*x*041R31*xxxxx*)	Quartus Prime Pro Edition software version 24.2	N/A	N/A
Polling.Active time out during Link Disable-Enable loop tests on page 50	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxx*)	None	N/A	N/A
R-Tile PCIe - Intermittent PCIe Gen4 EQ time out on page 51	Agilex 7 production devices (AGIx019R18A*xxxxx*) (AGIx023R18A*xxxxx*) (AGIx022R29A*xxxxx*) (AGIx027R29A*xxxxx*) (AGIx022R31A*xxxxx*) (AGIx027R31A*xxxxx*) (AGIx041R29*xxxxxx*) (AGIx041R31E*xxxxx*)	Quartus Prime Pro Edition software version 23.4 release Patch 0.07 firmware and Quartus Prime Pro Edition software version 24.1.	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
No response received during read operation on the xcvr_reconfig interface after an FPGA re-configuration on page 52	Agilex 7 production devices (AGI*x*019R18A*xxxxxx*) (AGI*x*023R18A*xxxxxx*) (AGI*x*022R29A*xxxxxx*) (AGI*x*027R29A*xxxxxx*) (AGI*x*022R31A*xxxxxx*) (AGI*x*027R31A*xxxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	Quartus Prime Pro Edition software version 23.3	N/A	N/A
Slow Completion response from Configuration requests targeting R-Tile Endpoint connected to Downstream port with finite Completion Header/ Data credits on page 53	Agilex 7 production devices (AGI*x*019R18A*xxxxxx*) (AGI*x*023R18A*xxxxxx*) (AGI*x*022R29A*xxxxxx*) (AGI*x*027R29A*xxxxxx*) (AGI*x*022R31A*xxxxxx*) (AGI*x*027R31A*xxxxxx*) (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	Quartus Prime Pro Edition software version 24.3.1	N/A	N/A
Bifurcated ports using Independent PERST pins might fail to link up after configuration is complete on page 54	Agilex 7 production devices (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	Quartus Prime Pro Edition software version 24.3	N/A	N/A
Port0 might be stuck in Detect when configuring bifurcated ports using Independent PERST pins on page 55	Agilex 7 production devices (AGI*x*041R29*xxxxxx*) (AGI*x*041R31E*xxxxx*)	Quartus Prime Pro Edition software version 24.3	N/A	N/A
CXL 1.1 version does not support uncorrectable error reporting when receiving two LLCTRL-Init packet on page 56	Agilex 7 production device (AGI*x*019R18A*xxxx*) (AGI*x*023R18A*xxxx*) (AGI*x*022R31A*xxxx*) (AGI*x*027R31A*xxxx*) (AGI*x*022R29A*xxxx*) (AGI*x*027R29A*xxxx*) (AGI*x*041R29D*xxxx*) (AGI*x*041R31E*xxxx*)	None	N/A	N/A
R-tile might report Fatal Error in the Advance Error Reporting (AER) registers when using Address Translation Service (ATS) on page 57	Agilex 7 production device AGI*x*019R18A*xxxxx* AGI*x*023R18A*xxxxx* AGI*x*022R29A*xxxxx* AGI*x*027R29A*xxxxx* AGI*x*022R31A*xxxxx* AGI*x*027R31A*xxxxx* AGI*x*041R29D*xxxxx* AGI*x*041R31E*xxxxx*	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software	N/A	N/A
P-Tile				

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
Root Port Legacy Interrupt Status register INTx is stuck HIGH on page 58	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
TLP Bypass Error Status register may report receiver errors after the PERST is released on page 59	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Register Implementation while using the SR-IOV Feature on page 60	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Register Implementation while using the Multi-function Feature on page 61	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
P-Tile: Unsuccessful TX Equalization on page 63	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Link May Not Degrade With Corrupt Lanes (P-Tile) on page 64	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Warm Reset or PERST Assertion Clears the Sticky Registers on page 65	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Multiple Fatal Error Messages on page 66	Agilex 7 production devices (AGFx014R24A*xxxxx*) (AGFx023R25A*xxxxx*) (AGFx027R25A*xxxxx*)	None	N/A	N/A
Configuration and Security				
FPGA Reconfiguration May Cause Device to Halt on page 67	(AGFx012*xxxxxxx*) (AGFx014*xxxxxxx*) (AGFx022*xxxxxxx*) (AGFx027*xxxxxxx*) (AGIx022*xxxxxxx*) (AGIx027*xxxxxxx*)	None	N/A	N/A

continued...

Issue	Affected Devices (OPN)	Planned Fix (OPN)	Document Update	Notification
Secure Device Manager May Disable Physically Unclonable Function on page 68	(AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
Reset Timing Violation for QSPI Flash Specification on page 69	(AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
Hard Processor System				
Write Data Can Appear at an AXI Interface before the Write Address, which can Cause a Deadlock Condition on page 70	(AGF*xxxxxxxxxxx*) (AGI*xxxxxxxxxxx*)	None	N/A	N/A
HPS EMAC Rx interface stuck in unresponsive state on page 71	Agilex 7 production devices with HPS (AG*x*B*xxxxxxxxxxx*) (AG*x*D*xxxxxxxxxxx*) (AG*x*E*xxxxxxxxxxx*) (AG*x*F*xxxxxxxxxxx*)	None	N/A	N/A

2.1. FPGA

2.1.1. F-Tile

2.1.1.1. 200G/400G Ethernet Mode Does Not Support Port-Based Priority Flow Control

Description

In the Agilex 7 FPGAs with F-Tile, the F-Tile Ethernet Hard IP and F-Tile Ethernet Multirate IP do not support port-based priority flow control (PFC) in the 200G/400G mode.

Workaround

None

Status

Table 3. Device Status Table

Device Affected	Planned Fix
Agilex 7 production devices with no suffix (blank) OPN	• B suffix OPNs (for example, AGI*x*0*xx*R*xxxxxxx*B; AGF*x*0*xx*R*xxxxxxx*B) • C suffix OPNs (for example, AGI*x*0*xx*R*xxxxxxx*C; AGF*x*0*xx*R*xxxxxxx*C)

2.1.1.2. The F-Tile Ethernet 200G Hard IP block is de-featured and cannot be used in production devices with OPNs that have no suffix (blank) or "B" suffix

Description

The F-Tile Ethernet 200G Hard IP block is de-featured and cannot be used in production devices with OPNs that have no suffix (blank) or "B" suffix. Starting with the release of Quartus Prime Pro Edition software version 23.4, an error message appears when the block is included in the design.

Workaround/Resolution

If your design requires use of the 200G Hard IP block, use production devices with OPNs that have "C" suffix. If you are using production devices with OPNs that have no suffix (blank) or "B" suffix, and your design includes the 200G Hard IP block, contact the Altera customer support team for additional information.

Status

Table 4. Device Status Table

Devices Affected	Planned Fix
Agilex 7 production devices with no suffix (blank) or "B" suffix OPNs	Agilex 7 production devices with "C" suffix OPN

2.1.1.3. The Deterministic Latency Feature supports on E200 block Six of Eight FGT Channels

Description

The F-Tile 200G Hard IP block is enabled in production devices with OPNs with a “C” suffix. However, the optional Deterministic Latency feature of the 200G Hard IP block is only supported in six of eight FGT channels. These six channels are FGT Quad 0 channel 1, FGT Quad 0 channel 3, or any FGT Quad 1 channel. The Deterministic Latency feature of the 200G Hard IP block is not guaranteed to function properly on FGT Quad 0 channel 0 and FGT Quad 0 channel 2.

Workaround

If your design requires using the 200G Hard IP block without the Deterministic Latency feature for the 200G Hard IP block, then use any production devices with OPNs with a "C" suffix.

If your design requires the use of the 200G Hard IP block and only requires Deterministic Latency support for the 200G Hard IP block on FGT Quad 0 channel 1, Quad 0 channel 3, or any FGT Quad 1 channel, then use any production devices with OPNs that have a “C” suffix.

If your design requires the use of the 200G Hard IP block and also requires the use of the Deterministic Latency feature for the 200G Hard IP block on any of the FGT channels in Quad 0 or Quad 1, then use any production device with OPNs that have a “C” suffix and is delivered starting in Q1’2025.

Status

Table 5. Device Status Table

Devices Affected	Planned Fix
Agilex 7 production devices with "C" suffix OPN shipped in 2024	Agilex 7 production devices with “C” suffix OPN shipped in 2025 or later

2.1.1.4. FHT TX EOJ Spec Compliance Issue

Description

The FHT transmitter does not meet the Even and Odd Jitter compliance specification as detailed in the CEI 4.0/5.0 and IEEE 802.3 standard. The rates affected are 53, 58, 106, and 116 Gbps.

Workaround

None

Status

Table 6. Device Status Table

Devices Affected	Planned Fix
Agilex 7 production devices manufactured before 2024	Devices manufactured in 2024 and beyond support improved FHT Transceiver EOJ performance and are fully compliant with published specifications.

2.1.1.5. Requirement for F-Tile Devices which are Powered and Unconfigured

Description

To prevent F-Tile performance degradation, devices with F-Tile must not remain in a powered-up and unconfigured state for a cumulative time exceeding 12 months.

Workaround

None

Status

Table 7. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.6. FGT PAM4 Compliance Support

Description

The FGT transceiver requires Quartus Prime Pro Edition software version 25.1.1 (or later) for PAM4 electrical specifications compliance.

Workaround

For protocols that require FGT PAM4 usage, please upgrade to Quartus Prime Pro Edition software version 25.1.1 or later release.

Status

Table 8. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	Quartus Prime Pro Edition software version 25.1.1

2.1.1.7. FGT Transceivers Do Not Support Direct EXTEST JTAG Instruction in Boundary Scan Test

Description

Due to a problem with the Boundary Scan circuitry of the FGT transceivers, the `EXTEST` JTAG instruction cannot be executed directly.

Workaround

Altera recommends utilizing the `EXTEST_PULSE`/`EXTEST_TRAIN` JTAG instruction on FGT transceivers. In cases where the `EXTEST` JTAG instruction is still mandatory, you can execute the `SAMPLE`/`PRELOAD` JTAG instruction ahead of each `EXTEST` JTAG instruction.

Status

Table 9. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.8. F-Tile: Unsuccessful TX Equalization

Description

In the F-Tile IP for PCIe*, when a speed change to Gen3/Gen4 speed is attempted for the first time with full **TxEq** enabled, if all phases of equalization do not successfully complete, the link reverts back to the lowest speed that passed equalization. The Equalization results for Gen3 and Gen4 are recorded in the following registers:

- For Gen3: `Link Status 2 Register [4:1]`:
  - [1] Equalization 8.0 GT/s Complete
  - [2] Equalization 8.0 GT/s Phase 1 Successful
  - [3] Equalization 8.0 GT/s Phase 2 Successful
  - [4] Equalization 8.0 GT/s Phase 3 Successful

- For Gen4: `16.0 GT/s Status Register [3:0]`
  - [0] Equalization 16.0 GT/s Complete
  - [1] Equalization 16.0 GT/s Phase 1 Successful
  - [2] Equalization 16.0 GT/s Phase 2 Successful
  - [3] Equalization 16.0 GT/s Phase 3 Successful

If equalization is attempted, the "`Complete`" bit is set for that speed regardless if the other phases of equalization completed successfully. Once the "`Complete`" bit is set, the F-Tile permits a speed change by setting the **Target Link Speed** in the `Link Control 2 Register`. As a result, the link may train to Gen3/Gen4 speeds with sub-optimal transmitter equalization settings.

To confirm if the transmitter equalization procedure completed successfully, use software to read the following registers and ensure that all bits are set:

- For Gen3: `Link Status 2 Register [4:1]`
- For Gen4: `16.0 GT/s Status Register [3:0]`

To re-initiate the equalization procedure, write **1b** to the `Perform Equalization bit [0]` in the `Link Control 3 register`.

Workaround

Use software to check that the link equalization procedure was successfully performed:

- For Gen3: Both `Equalization 8.0 GT/s Phase 3 Successful` bit and `Equalization 8.0 GT/s Complete` bit of the `Link Status 2` register are set to **1b**.
- For Gen4: Both `Equalization 16.0 GT/s Phase 3 Successful` bit and `Equalization 16.0 GT/s Complete` bit of `16.0 GT/s Status Register` are set to **1b**.

If required, re-initiate the link equalization procedure by:

1. Writing **1b** to the `Perform Equalization` bit in the `Link Control 3` register.
2. Followed by a write to the `Target Link Speed` field in the `Link Control 2` register to enable the Link to run at 8.0 GT/s or higher.
3. Followed by a write of **1b** to the `Retrain Link` bit in the `Link Control` register of the Downstream Port.

Status

Table 10. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.9. Link May Not Downgrade With Corrupt Lanes (F-Tile)

Description

When using F-Tile IP for PCIe, if one or more lanes is corrupted (for example: faulty connection in the TX/RX pin) or not connected, the link may not downgrade as expected. For example, if lane 3 and 8 of a x16 link are not connected, the link may downgrade to x2 (active lanes 0-1), instead of x4 (active lanes 12-15).

Ensure that the F-Tile PCIe IP link width is configured according to your board implementation.

Workaround

None

Status

Table 11. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.10. Occasional Equalization Timeout or PCIe Link Training Failure to Achieve Expected Link Speed during Link Disable, Hot Reset, and Speed Change

Description

In the F-tile IP for PCIe, when you perform link disable, hot reset, or speed change (at Gen 4 and Gen 3), in the worst case scenario, an equalization timeout or PCIe link training failure could occur, preventing the link from achieving the expected speed.

Workaround

You should verify the PCIe link speed after link disable, hot reset, or speed change procedure. If the PCIe link speed does not meet the expectation, repeat the link disable, hot reset, or speed change procedure to allow the link to recover at the desired speed.

Status

Table 12. Device Status Table

Device Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.11. Link Fault Detection window of the F-Tile Ethernet Hard IP in 10GE-1 or 25GE-1 mode

Description

The Link Fault Detection window of the F-Tile Ethernet Hard IP in 10GE-1 or 25GE-1 mode is doubled. Both the Local and Remote Fault detection are affected for these modes. As a result of this problem, IEEE 802.3 Clause-46 compliance testing fails due to the detection window being twice as long as the IEEE 802.3 Clause-46 specification calls for. Since the detection window is doubled, the amount of non-Local or non-Remote Fault ordered sets required to clear the fault condition is also doubled. This problem does not affect the normal operation of the MAC and is only seen during compliance testing. The problem only affects the 10GE-1 and 25GE-1 modes of operation.

Workaround

None

Status

Table 13. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.12. FHT PMA Transmitter-to-Receiver Internal Serial Loopback operation for error-free BER results

Description

When using the FHT PMA **Transmitter-to-Receiver Internal Serial Loopback** mode of operation, you must ensure that no signal is being driven onto the receive serial pins of the PMA in order to obtain error-free BER results. If a signal is being driven onto the RX serial pins, the BER testing yields non-zero results.

Workaround

No workaround available.

Status

Table 14. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.13. F-Tile Ethernet Hard IP `rst_tx_stats` and `rst_rx_stats` register bits might not function correctly

Description

When using the F-Tile Ethernet Hard IP, the `rst_tx_stats` and the `rst_rx_stats` register bits might not function correctly and the resultant Ethernet MAC TX statistics and MAC RX statistics might not be cleared correctly.

Workaround

Assert and deassert the register bits multiple times until the appropriate MAC statistics are cleared correctly.

Status

Table 15. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.14. F-Tile Ethernet Hard IP `force_rf` register bit might not function correctly

Description

When using the F-Tile Ethernet Hard IP, the `force_rf` register bit might not function correctly. Asserting the `force_rf` register bit might cause the F-Tile Ethernet Hard IP to start transmitting errored packets.

Workaround

If the link partner starts observing errored packets, then reset the F-Tile Ethernet Hard IP's transmit path via the `soft_tx_rst` register bit or the `i_tx_rst_n` port of the F-Tile Ethernet Hard IP.

Status

Table 16. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.15. F-Tile Ethernet Hard IP `tx_pause_request` register bit might not function correctly

Description

When using the F-Tile Ethernet Hard IP, the `tx_pause_request` register bit might not function correctly.

Workaround

Use the `i_tx_pause_request` port on the F-Tile Ethernet Hard IP.

Status

Table 17. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.16. F-Tile Ethernet Hard IP PTP statistics might not clear correctly

Description

When using the F-Tile Ethernet Hard IP with PTP enabled, the following PTP statistics might be set to 1'b1 instead of 1'b0 when attempting to clear the statistics. If this condition has been encountered, the PTP statistics indicate one additional packet than what was actually transmitted or received.

- `cntr_tx_total_ptp_pkts`
- `cntr_tx_total_1step_ptp_pkts`
- `cntr_tx_total_2step_ptp_pkts`
- `cntr_tx_total_v1_ptp_pkts`
- `cntr_tx_total_v2_ptp_pkts`
- `cntr_rx_total_ptp_ts`

Workaround

Repeatedly clearing the statistics might eventually properly clear the PTP statistics.

Status

Table 18. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.17. F-Tile Ethernet Hard IP unable to achieve 100% throughput with some variants

Description

When using the F-Tile Ethernet Hard IP in the configurations captured in the below table, the IP is unable to achieve 100% throughput by the small amounts shown. This is due to the fact that the hard MAC within the IP is not removing IDLE characters in order to compensate for Alignment Marker (AM) insertion.

Table 19.

Data Rate	FEC Mode	Throughput Loss?	PPM Impact	Throughput Loss as a % of Full Line Rate
10G	NO_FEC/FC_FEC	NO	NO	NO
25G	NO_FEC	NO	NO	NO
25G	FC_FEC	NO	NO	NO
25G	RS_FEC	YES	48.828125	.0048
40G	NO_FEC/RS_FEC	YES	61.03515625	.0061
50G	NO_FEC/RS_FEC	YES	48.828125	.0048
100G	NO_FEC/RS_FEC	YES	61.03515625	.0061
200G	RS_FEC	YES	48.828125	.0048
400G	RS_FEC	YES	48.828125	.0048

Workaround

Potential workarounds to achieve 100% throughput with the IP include overclocking the TX reference clock to compensate for PPM loss, adjusting the `MIN_AVG_IPG` value from 12 to 10, or using a soft MAC IP where applicable.

Status

Table 20. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.1.18. F-Tile 400G Ethernet Hard IP RX Priority Flow Control Issue

Description

When using the F-Tile 400G Ethernet Hard IP with Priority Flow Control (PFC) enabled, the RX MAC might incorrectly turn a priority queue from the XOFF state to the XON state when all of the following conditions are met:

- The RX MAC receives 2 back-to-back PFC frames with no other type of Ethernet frame between them
- The second PFC frame is sent before the quanta of the first PFC frame expires
- The Priority Enable Vector (PEV) of the second PFC frame has some of the same classes enabled as the first PFC frame
- The packet arrangement on the RX MAC MII interface is such that the second PFC frame's PEV and End-of-Packet appear in the same MII clock cycle

Workaround

None.

Status

Table 21. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.1.19. F-Tile Ethernet Hard IP Bidirectional Link Fault Signaling Issue

Description

When using the F-Tile Ethernet Hard IP variant with the `Link fault generation` parameter set to `Bidirectional`, the TX MAC might transmit invalid packets when it stops sending `remote fault` ordered sets during link fault recovery. These packets can have various issues, such as `FCS` or length errors. In certain cases, when encountering this issue, the Ethernet link might fail to recover.

Workaround

In cases where the link does not recover, assert and deassert `i_tx_rstn` or `i_rst_n` ports or the corresponding soft CSR bits.

Status

Table 22. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	Quartus Prime Pro Edition software version 25.1.1

2.1.1.20. F-Tile SDI II IP and F-Tile PMA/FEC Direct PHY IP with "SDI" configuration rule are not of production quality

Description

The F-Tile SDI II IP and F-Tile PMA/FEC Direct PHY IP with "SDI" configuration rule are not completely compliant with the SDI receiver specifications. Do not use these IP cores in a production design, especially when testing with pathological pattern insertion.

These IP cores can be used for hardware evaluation as well as simulation.

Workaround

None.

Status

Table 23. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	This issue is scheduled to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.1.21. F-Tile HDMI IP and F-Tile PMA/FEC Direct PHY IP with "HDMI" configuration rule are not of production quality

Description

The F-Tile HDMI IP and F-Tile PMA/FEC Direct PHY IP with "HDMI" configuration rule are not completely compliant with the HDMI receiver specifications. Do not use these IP cores in a production design.

These IP cores can be used for hardware evaluation as well as simulation.

Workaround

None.

Status

Table 24. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	This issue is scheduled to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.1.22. Ethernet Auto-Negotiation and Link Training (AN/LT) designs on F-Tile FGT may not link up when using Quartus Prime Pro Edition software version 25.1.1 and 25.3

Description

Ethernet AN/LT designs (all data rates) on F-Tile FGT might not link up, due to an Ethernet and AN/LT reset release causing race condition. This issue only exists in Quartus Prime Pro Edition software versions 25.1.1 and 25.3. This issue does not apply to Quartus Prime software release 25.1 or earlier.

Workaround

Contact the Altera customer support team for patch information for Quartus Prime Pro Edition software versions 25.1.1 and 25.3.

Status

Table 25. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.1.23. IEEE 802.3-2022 50GBASE-KR compliance testing instability during Link Training (LT)

Description

F-Tile FGT 50GBASE-KR compliance testing has identified occasional instability during Link Training (LT), which can lead to suboptimal transmitter FFE configuration and reduced performance/BER.

This instability might happen with F-Tile Ethernet AN/LT enabled designs for FGT 50GBASE-KR only. This issue only exists in Quartus Prime Pro Edition software versions 25.1.1 and 25.3. This issue does not apply to Quartus Prime software release 25.1 or earlier.

Workaround

For FGT 50GBASE-KR designs, a reset is required while observing the instability during link training (LT) for recovery. Or perform the Link Training (LT) at nominal temp 25°C and keep the DTR (Dynamic Temperature Range) within 75°C to reduce the instability.

Contact the Altera customer support team for patch information for Quartus Prime Pro Edition software versions 25.1.1 and 25.3.

Status

Table 26. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	This issue is planned to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.2. R-Tile

2.1.2.1. Gen3/Gen4 link might be established without successfully performing Transmit Equalization (TX EQ)

Description

In the R-Tile IP for PCIe configured natively in Gen5, when a speed change to Gen3/Gen4 speed is attempted for the first time with full **TxEq** enabled, if all phases of equalization do not successfully complete, the link reverts back to the lowest speed that passed equalization. The Equalization results for Gen3 and Gen4 are recorded in the following registers:

- For Gen3: `Link Status 2 Register [4:1]`:
  - [1] Equalization 8.0 GT/s Complete
  - [2] Equalization 8.0 GT/s Phase 1 Successful
  - [3] Equalization 8.0 GT/s Phase 2 Successful
  - [4] Equalization 8.0 GT/s Phase 3 Successful

- For Gen4: `16.0 GT/s Status Register [3:0]`:
  - [0] Equalization 16.0 GT/s Complete
  - [1] Equalization 16.0 GT/s Phase 1 Successful
  - [2] Equalization 16.0 GT/s Phase 2 Successful
  - [3] Equalization 16.0 GT/s Phase 3 Successful

If equalization is attempted, the "`Complete`" bit is set for that speed regardless if the other phases of equalization completed successfully. Once the "`Complete`" bit is set, the R-Tile permits a speed change by setting the **Target Link Speed** in the `Link Control 2 Register`. As a result, the link may train to Gen3/Gen4 speeds with sub-optimal transmitter equalization settings.

To confirm if the transmitter equalization procedure completed successfully, use software to read the following registers and ensure that all bits are set:

- For Gen3: `Link Status 2 Register [4:1]`
- For Gen4: `16.0 GT/s Status Register [3:0]`

To re-initiate the equalization procedure, write **1b** to the `Perform Equalization bit [0]` in the `Link Control 3 register`.

Impacted PCIe Hard IP Modes

- Endpoint
- Root Port
- TL Bypass

Workaround

None

Status

Table 27. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxx* • AGI*x*023R18A*xxxxx* • AGI*x*022R29A*xxxxx* • AGI*x*027R29A*xxxxx* • AGI*x*022R31A*xxxxx* • AGI*x*027R31A*xxxxx* • AGI*x*041R29*xxxxxx* • AGI*x*041R31E*xxxxx*	None

2.1.2.2. Link may not downgrade with corrupt lanes

Description

When using R-Tile IP for PCIe, if one or more lanes are corrupted (for example: faulty connection in the TX/RX pin) or not connected, the link may not downgrade as expected. For example, if lane 3 and 8 of a x16 link are not connected, the link may downgrade to x2 (active lanes 0-1), instead of x4 (active lanes 12-15).

Ensure that the R-Tile PCIe IP link width is configured according to your board implementation.

Impacted PCIe Hard IP Modes

- Endpoint

Workaround

None

Status

Table 28. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	None

2.1.2.3. Malformed TLP incorrectly flagged as ECRC error

Description

For all Agilex 7 devices with R-Tile, if a received TLP has TD (TLP Digest) set to 1 without the ECRC data, an ECRC Error may be flagged instead of a Malformed TLP.

You must make sure ECRC data is not 0 when TD is set to 1 to avoid this issue.

Impacted PCIe Hard IP Modes

- Endpoint
- Root Port
- TL Bypass

Workaround

None

Status

Table 29. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxx* • AGI*x*023R18A*xxxxx* • AGI*x*022R29A*xxxxx* • AGI*x*027R29A*xxxxx* • AGI*x*022R31A*xxxxx* • AGI*x*027R31A*xxxxx* • AGI*x*041R29*xxxxxx* • AGI*x*041R31E*xxxxx*	None

2.1.2.4. Assertion of PERST / warm reset during the Functional Level Reset results in PCIe Link Failure

Description

In the R-Tile IP for PCIe, you must avoid the `PERST` assertion during a functional level reset or before a functional level reset is completed since this could impact the link training process. This is also applicable when using the independent `PERST` feature to issue a warm reset (Independent `GPIO PERST` and Independent `PERST` pins). In case this occurs, a cold reset is required to properly complete the link training process.

Impacted PCIe Hard IP Modes

- Endpoint

Workaround

None

Status

Table 30. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	None

2.1.2.5. No Support for Page Request Services in Port 2 and Port 3 of 4x4 Configuration

Description

In the R-Tile IP for PCIe, the Page Request Services (PRS) interface is not supported in Port 2 and Port 3 of 4x4 configuration.

Impacted PCIe Hard IP Modes

- Endpoint

Workaround

None

Status

Table 31. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxx* • AGI*x*023R18A*xxxxx* • AGI*x*022R29A*xxxxx* • AGI*x*027R29A*xxxxx* • AGI*x*022R31A*xxxxx* • AGI*x*027R31A*xxxxx* • AGI*x*041R29*xxxxxx* • AGI*x*041R31E*xxxxx*	None

2.1.2.6. Multiple Fatal Error Messages

Description

When the R-Tile IP for PCIe receives a different scale factor for Flow Control (FC) update than the FC initialization, the IP sends multiple fatal error messages instead of one.

Impacted PCIe Hard IP Modes

- Endpoint
- Root Port
- TL Bypass

Workaround

None

Status

Table 32. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	None

2.1.2.7. PCIe x4 cores may report Uncorrectable Fatal Error or Malformed TLP

Description

In the R-tile IP for PCIe, the 2nd and 3rd PCIe x4 cores (x4core_0 and x4core_1) fail the atomic address alignment check when the Processing Hints is not 0 and the TLP Hints bit is not set. This failure is reflected as Uncorrectable Fatal Error or Malformed TLP. The PCIe x16 core and x8 core are not affected as the Processing Hints is stripped off when TLP Hints bit is not set during an atomic address alignment check.

Impacted PCIe Hard IP Modes

- Endpoint
- Root Port
- TL Bypass

Workaround

You must not send non-zero Processing Hints when TLP Hints bit is not set.

Status

Table 33. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxx* • AGI*x*023R18A*xxxxx* • AGI*x*022R29A*xxxxx* • AGI*x*027R29A*xxxxx* • AGI*x*022R31A*xxxxx* • AGI*x*027R31A*xxxxx* • AGI*x*041R29*xxxxxx* • AGI*x*041R31E*xxxxx*	None

2.1.2.8. Receiver Errors logged during back-to-back Secondary Bus Resets (SBR) operations when running at Gen 2 speed

Description

When running back-to-back Secondary Bus Reset (SBR) operations, receiver errors may be logged under the following conditions for the R-Tile Avalon®-ST FPGA IP for PCIe:

- Configured in Endpoint, Root Port, and TL Bypass modes
- Link down trained at Gen 2 speed

This problem is not observed when link is trained at Gen3/Gen4/Gen5 speeds.

Workaround

None

Status

Table 34. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R31E*xxxxx*	None

2.1.2.9. R-Tile Digital Temperature Sensor Readings

Description

In the R-Tile IP for PCIe, when the Debug Toolkit or the PHY reconfiguration interface (`xcvr_reconfig`) are enabled in the IP Parameter Editor, the temperature readings performed to the R-Tile Digital Thermal Sensor may be invalid.

Impacted Modes

- PCIe IP modes Endpoint
- Root Port
- TL Bypass

Workaround

For a design that requires to perform temperature readings to the R-Tile Digital Thermal Sensor, set to disable the Debug Toolkit and the PHY reconfiguration interface (`xcvr_reconfig`) in the IP Parameter Editor.

Status

Table 35. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxxx* • AGI*x*023R18A*xxxxxx* • AGI*x*022R29A*xxxxxx* • AGI*x*027R29A*xxxxxx* • AGI*x*022R31A*xxxxxx* • AGI*x*027R31A*xxxxxx*	None

2.1.2.10. R-Tile PCIe - LCRC Error/Malformed TLP

Description

You might observe a corrupted TLP packet (Bad LCRC or Malformed TLP) sent by R-Tile.

PCIe IP:

- Malformed TLP case: The incorrect packet is expected to cause the link partner to log an AER Uncorrectable Error.
- Bad LCRC TLP case: The incorrect packet is expected to cause link partner to issue NAK, and log AER Correctable Errors as Bad TLP and Receiver Error. The reply buffer is expected to send the same Bad LCRC TLP and is expected to prevent forward progression of any TLP.

This issue can happen under the following conditions:

- R-Tile configured in PCIe mode
- Max Payload Size (MPS) = 512B
- Selective PCIe TX traffic pattern that result in credit starvation from link partner

Root Cause: The issue caused by a non-optimal IP setting which configures how the IP consumes the data traffic.

The current fix available in the Quartus Prime Pro Edition software version 23.4 release can result in the following:

- Performance degradation (lower throughput) when running traffic with 512B payloads
- Malformed TLP/LCRC error when running 256B payload

However, the latest fix available in the Quartus Prime Pro Edition 24.3.1 software release eliminates the "current fix" issues described above.

Impacted Modes

- PCIe IP modes Endpoint
- Root Port
- TL Bypass

Workaround

Prior to the Quartus Prime Pro Edition software version 23.4 release, if an error is observed, a system cold reset is required for recovery. This issue has been fixed in the Quartus Prime Pro Edition software version 24.3.1 and later.

Status

Table 36. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx*	Fixed in Quartus Prime Pro Edition software version 24.3.1.

Devices Affected	Planned Fix
• AGI*x*027R29A*xxxxx* • AGI*x*022R31A*xxxxx* • AGI*x*027R31A*xxxxx* • AGI*x*041R29*xxxxxxx* • AGI*x*041R31E*xxxxxx*	

2.1.2.11. R-Tile PIPE-Direct - `rxdatavalid` Signal Unexpected Toggling After P1 to P0 Transition

Description

Unexpected toggling might be observed in the `rxdatavalid` signal, when transitioning from a low power state (P1) to normal operation (P0). This might impact symbol lock in the PCS block.

Impacted Modes

- PIPE Direct Mode

Workaround

Link re-training is required.

Status

Table 37. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxxx* • AGIx023R18A*xxxxxx* • AGIx022R29A*xxxxxx* • AGIx027R29A*xxxxxx* • AGIx022R31A*xxxxxx* • AGIx027R31A*xxxxxx* • AGIx041R29*xxxxxxx* • AGIx041R31*xxxxxx*	Quartus Prime Pro Edition software version 24.2

2.1.2.12. Polling.Active time out during Link Disable-Enable loop tests

Description

When running the LTSSM Link disable-enable loop test, you might observe a timeout during the Polling.Active state reported by the link partner. This timeout is reported only when R-Tile is connected with the link partner using port 0. This issue has no functional impact, and the link comes up correctly at L0 at the target width and speed.

Impacted PCIe Hard IP Modes

- Endpoint
- Root Port
- TL Bypass

Workaround

None

Status

Table 38. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxxxx* • AGI*x*023R18A*xxxxxx* • AGI*x*022R29A*xxxxxx* • AGI*x*027R29A*xxxxxx* • AGI*x*022R31A*xxxxxx* • AGI*x*027R31A*xxxxxx* • AGI*x*041R29*xxxxxx*x • AGI*x*041R31E*xxxxx*	None

2.1.2.13. R-Tile PCIe - Intermittent PCIe Gen4 EQ time out

Description

Intermittent Recovery Equalization timeout might occur under the following conditions when R-Tile is configured as Gen5:

- Links up with a Gen4 link partner or
- Links up with a Gen5 link partner with `Equalization bypass to highest rate supported` bit not set in the 32.0 GT/s Capabilities Register of the Physical Layer 32.0 GT/s Extended Capability (link training goes through Gen3 EQ → Gen4 EQ → Gen5 EQ)

The root cause is the non-optimal PHY recipe setting of `save & restore`. The issue is not present when R-Tile is configured as native Gen4 IP.

Impacted modes

- All PCIe modes
- PIPE-Direct mode

Workaround

None.

Status

Table 39. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxxx* • AGIx023R18A*xxxxxx* • AGIx022R29A*xxxxxx* • AGIx027R29A*xxxxxx* • AGIx022R31A*xxxxxx* • AGIx027R31A*xxxxxx* • AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	Quartus Prime Pro Edition software version 23.4 Patch 0.07 firmware, Quartus Prime Pro Edition software version 24.1

2.1.2.14. No response received during read operation on the xcvr_reconfig interface after an FPGA re-configuration

Description

The xcvr_reconfig interface in the R-Tile IP for PCIe requires to have write and read transactions issued in multiples of 8. Not meeting this guideline can cause a lack of response for read operation on the xcvr_reconfig interface after an FPGA re-configuration and it might require a FPGA power cycle in order to recover the access to the xcvr_reconfig interface.

Workaround

The FPGA Application logic must keep track of the number of write and read transactions performed on the xcvr_reconfig interface prior to the FPGA reconfiguration.

The following guideline describes the tracking that needs to be implemented to track the number of transactions prior the FPGA reconfiguration:

1. The FPGA Application logic implements two separate transaction counters, one for read operations and one for write operations.
2. The FPGA Application logic increases this counter for every transaction issued in the xcvr_reconfig interface.
3. Once FPGA Application logic has completed the accesses required on the xcvr_reconfig interface, it must evaluate the counter and confirm it is a multiple of 8.
   - In case additional write operations are required, the FPGA Application logic must perform the additional write operations with a value of 0x0 to the address offset 0x6_0000.
   - In case additional read transactions are required, the FPGA Application logic must perform the additional read operations to the address offset 0x6_0000. For example, if FPGA Application logic performed only one write operation and two read operations on the xcvr_reconfig interface, as soon as those operations are completed, the FPGA Application logic must perform an additional seven dummy write operations and six dummy read operations to the register offset provided above. This ensures the numbers of transaction issued on the xcvr_reconfig interface is always a multiple of eight.

Status

Table 40. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	Quartus Prime Pro Edition software version 23.3

2.1.2.15. Slow Completion response from Configuration requests targeting R-Tile Endpoint connected to Downstream port with finite Completion Header/Data credits

Description

When the R-Tile IP for PCI Express* in Endpoint mode connects to a downstream port with finite completion header/data credits, you might notice a slow completion response from configuration requests targeting R-Tile, even if the link partner advertises enough completion credits.

R-Tile tracks the credits consumed by a completion generated from configuration requests and withholds the completion transmission until the link partner releases credits from previously transmitted completions.

A slow response might occur if the link partner does not frequently update the completion credit due to its internal UpdateFC scheduling mechanism or if the link is fully utilized for other transactions. This slow response might occasionally cause a completion timeout on the requester's end.

Impacted Modes

- PCIe IP in endpoint mode

Workaround

None.

Status

Table 41. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29*xxxxxx* • AGIx041R31*xxxxx*	Quartus Prime Pro Edition software version 24.3.1

2.1.2.16. Bifurcated ports using Independent PERST pins might fail to link up after configuration is complete

Description

When using `Enable Independent PERST` pins to implement bifurcated x8x8 ports in R-Tile Avalon Streaming IP for PCI Express in Endpoint mode, both ports might fail to link up under the following scenarios:

- **Scenario 1:** When FPGA is configured with

  `-refclk0` unavailable, `i_pin_perst0_n` deasserted (`1'b1`) and

  `-refclk1` stable and free running, `i_pin_perst1_n` deasserted (`1'b1`) and

  `-refclk2` stable and free running, `i_pin_perst_n` deasserted (`1'b1`),
  then `Port 0` is expected to be in reset, while `Port 1` fails to link up. Toggling the `i_pin_perst1_n` or `i_pin_perst_n` does not recover the link on `Port 1`. This issue is fixed in Quartus Prime Pro Edition software version 24.3 (Port 0 in reset, Port 1 links up). To allow Port 0 to link up once the `refclk0` becomes available after FPGA configuration is complete, you must toggle `i_pin_perst0_n`. Toggling the `i_pin_perst_n` causes both the links to fail link up and the FPGA must be reconfigured to recover from this state.
- **Scenario 2:** When FPGA is configured with

  `-refclk0` stable and free running, `i_pin_perst0_n` deasserted (`1'b1`) and

  `-refclk1` unavailable, `i_pin_perst1_n` deasserted (`1'b1`) and

  `-refclk2` stable and free running, `i_pin_perst_n` deasserted (`1'b1`),
  then `Port 0` fails to link up, while `Port 1` is expected to be in reset. Toggling the `i_pin_perst0_n` or `i_pin_perst_n` does not recover the link on `Port 0`. This issue is fixed in Quartus Prime Pro Edition software version 24.3 (`Port 0` links up, `Port 1` in reset). To allow `Port 1` to link up once the `refclk1` becomes available after FPGA configuration is complete, you must toggle `i_pin_perst1_n`. Toggling the `i_pin_perst_n` causes both the links to fail link up and the FPGA must be reconfigured to recover from this state.

Impacted Modes

- PCIe IP in endpoint mode

Workaround

None.

Status

Table 42. Device Status Table

Devices Affected	Planned Fix
• AGI*x*041R29*xxxxxx* • AGI*x*041R31E*xxxxx*	Quartus Prime Pro Edition software version 24.3

2.1.2.17. Port0 might be stuck in Detect when configuring bifurcated ports using Independent PERST pins

Description

When using "Enable independent PERST pins" for implementing bifurcated x8x8 ports in R-Tile Avalon Streaming IP for PCI Express in Endpoint mode, if port1's `pin_perst_n` is asserted, port 0 might be stuck in Detect state and fail to link up. This might be observed after FPGA configuration or when `pin_perst_n` is toggled.

Impacted Modes

- PCIe IP modes endpoint

Workaround

None.

Status

Table 43. Device Status Table

Devices Affected	Planned Fix
• AGIx041R29*xxxxxx* • AGIx041R31E*xxxxx*	Quartus Prime Pro Edition software version 24.3

2.1.2.18. CXL 1.1 version does not support uncorrectable error reporting when receiving two LLCTRL-Init packet

Description

CXL 1.1 version does not support uncorrectable error reporting when receiving two LLCTRL-Init packets. This is a simulation model issue that reflects the R-Tile behavior and it is a violation of the CXL 1.1 Spec.

Workaround

None

Status

Table 44. Device Status Table

Devices Affected	Planned Fix
• AGI*x*019R18A*xxxx* • AGI*x*023R18A*xxxx* • AGI*x*022R31A*xxxx* • AGI*x*027R31A*xxxx* • AGI*x*022R29A*xxxx* • AGI*x*027R29A*xxxx* • AGI*x*027R29A*xxxx* • AGI*x*041R29D*xxxx* • AGI*x*041R31E*xxxx*	None

2.1.2.19. R-tile might report Fatal Error in the Advance Error Reporting (AER) registers when using Address Translation Service (ATS)

Description

When using R-Tile Avalon Streaming FPGA IP for PCI Express, if the Address Translation Service feature is enabled, the R-Tile might report Fatal Error in the `Advance Error Reporting (AER)` registers if the ATS completion returned by the host is split.

Workaround

You can work around this problem by performing a read-modify-write to set bit `0x721[2]` (for x16, x8, and x4 controllers) in the PCIe configuration space. You can do this using your PCIe driver or the Hard IP reconfiguration interface. Alternatively, use `setpci` with the following commands:

- `setpci -s B:D.F reg_addr.B //read`
- `setpci -s B:D.F reg_addr.B=data //write`

Status

Table 45. Device Status Table

Devices Affected	Planned Fix
• AGIx019R18A*xxxxx* • AGIx023R18A*xxxxx* • AGIx022R29A*xxxxx* • AGIx027R29A*xxxxx* • AGIx022R31A*xxxxx* • AGIx027R31A*xxxxx* • AGIx041R29D*xxxxx* • AGIx041R31E*xxxxx*	This issue is scheduled to be fixed in a future release of the Quartus Prime Pro Edition software

2.1.3. P-Tile

2.1.3.1. Root Port Legacy Interrupt Status register INTx is stuck HIGH

Description

During root port implementation in the P-Tile IP for PCI Express*, the Root Port Legacy Interrupt status register `INT_status` of the port configuration and status register space (address: `0x10414C[3:0]`) is stuck HIGH (it can be any bit of `INT_status`) when the `AssertINTx` message is received but the `DeassertINTx` is not received. This may occur when a warm reset or `PERST` is issued before the endpoint sends the `DeassertINTx` message. As a result, the root port interrupt handling does not operate correctly.

Subsequent warm reset or `PERST` does not clear the stuck interrupt bits.

Impacted Modes

- P-Tile Avalon Streaming InterfacePCI Express in Root Port mode

Workaround

When using the P-Tile IP for PCI Express in root port mode, Altera recommends you use the MSI/MSI-X interrupt messages.

To avoid this event when using the Root Port Legacy Interrupt, ensure that an `AssertINTx` message is followed by a `DeassertINTx` message before a warm reset or `PERST` is issued. Otherwise, to clear the stuck interrupt bits, you must re-program the device.

Status

Table 46. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.2. TLP Bypass Error Status register may report receiver errors after the PERST is released

Description

During the TLP Bypass implementation using the P-Tile Avalon Streaming InterfacePCI Express, the `tlpbypass_err_status` register of port configuration and status registers space (address: `0x104190[8]`) may report receiver errors after the `PERST` is released. Therefore, if the user logic implements the Advanced Error Reporting (AER) capability based on the `tlpbypass_err_status` register, the correctable error status register of the AER capability indicates receiver errors.

Impacted Modes

- P-Tile Avalon Streaming InterfacePCI Express in TLP Bypass mode

Workaround

While using the P-Tile Avalon Streaming InterfacePCI Express, the user logic must clear the `tlpbypass_err_status` register's receiver error status bit (`0x104190[8]`) of the port configuration and status registers before the `PERST` is released.

Status

Table 47. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.3. Register Implementation while using the SR-IOV Feature

Description

While using the P-Tile IP for PCI Express:

- When the SR-IOV feature is enabled:
  - The PCIe capability link status register (offset `0x082h bits [15:0]`) returns the parent PF link status register values when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, when SR-IOV feature is enabled, this register must be implemented as Reserved and Zero (**RsvdZ**) and accessed by virtual functions.
  - The PCIe device control2 register (offset `0x098h bit [12]`: 10-bit tag requested enable bit) returns the parent PF device control2 register values when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, when SR-IOV feature is enabled, this register must be implemented as Reserved and Preserved (**RsvdP**) and accessed by virtual functions.
  - The PCIe Address Translation Service (ATS) control register (ATS base address + offset `0x006h bit [4:0]`: smallest translation unit (STU) bits) is implemented as read-only (**RO**) register but returns the value of the parent PF when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, this register must be implemented as a read-only (**RO**) register and hard-wired to 0 when accessed by virtual functions.

These issues do not cause functional failure.

Impacted Modes

- P-Tile Avalon Streaming InterfacePCI Express in Endpoint mode
- P-Tile Avalon Memory-Mapped InterfacePCI Express in Endpoint mode

Workaround

Your logic must use the Configuration Intercept Interface (CII) to modify the configuration accesses to these registers.

Status

Table 48. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.4. Register Implementation while using the Multi-function Feature

Description

While using the P-Tile IP for PCI Express:

- When the multi-function feature is enabled, the PCIe device status register (offset `0x07Ah bit [5]`: Transactions pending bit) for each of the virtual functions (VF) is implemented as a Write-1-to-Clear status register (**RW1C**). According to the PCIe Base specification revision 4.0 version 1.0, this register must be implemented as read-only (**RO**) when multi-function feature is enabled.

These issues do not cause functional failure.

Impacted Modes

- P-Tile Avalon Streaming InterfacePCI Express in Endpoint mode
- P-Tile Avalon Memory-Mapped InterfacePCI Express in Endpoint mode

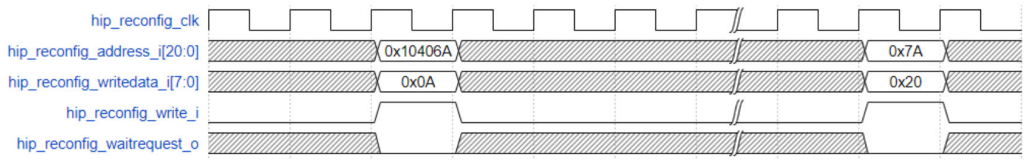
Workaround

The application logic can use Configuration Intercept Interface (CII) or Direct User Avalon Memory-Mapped Interface to modify the configuration accesses to this register.

Using the Direct User Avalon Memory-Mapped Interface:

The application logic must implement a tracking logic for any pending upstream memory read (MRd) completion. After the last pending MRd completion is received, refer to the *P-Tile Avalon Streaming IP for PCI Express User Guide* to clear the Transactions pending bit in the Device Status register. The following sequence is an example for VF3 in PF0.

1. Application logic programs the User Avalon memory-mapped interface Port Configuration Register (Offset 0x10406A, addressing the third byte of the register) with 0x0A (`vf_num[28:18]` = 2, `vf _select[17]` = 1, `vsec[0]` = 0).
2. Application logic sets the `hip_reconfig_addr_i[20:0]` with 0x7A which corresponds to the Device Status register within the VF PCI Express Capability Structure(1) and performs a write 1 operation to the Transaction pending bit [5] by setting the `hip_reconfig_writedata_i[7:0]` to 0x20.



(1) For more details, refer to the PCIe Configuration Registers for Each Virtual Function

Status

Table 49. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.5. P-Tile: Unsuccessful TX Equalization

Description

In the P-Tile IP for PCIe, when a speed change to Gen3/Gen4 speed is attempted for the first time with full **TxEq** enabled, if all phases of equalization do not successfully complete, the link reverts back to the lowest speed that passed equalization. The Equalization results for Gen3 and Gen4 is recorded in the following registers:

- For Gen3: `Link Status 2 Register [4:1]`:
  - [1] Equalization 8.0 GT/s Complete
  - [2] Equalization 8.0 GT/s Phase 1 Successful
  - [3] Equalization 8.0 GT/s Phase 2 Successful
  - [4] Equalization 8.0 GT/s Phase 3 Successful

- For Gen4: `16.0 GT/s Status Register [3:0]`:
  - [0] Equalization 16.0 GT/s Complete
  - [1] Equalization 16.0 GT/s Phase 1 Successful
  - [2] Equalization 16.0 GT/s Phase 2 Successful
  - [3] Equalization 16.0 GT/s Phase 3 Successful

If equalization is attempted, the "`Complete`" bit is set for that speed regardless if the other phases of equalization completed successfully. Once the "`Complete`" bit is set, the P-Tile permits a speed change by setting the **Target Link Speed** in the `Link Control 2 Register`. As a result, the link may train to Gen3/Gen4 speeds with sub-optimal transmitter equalization settings.

To confirm if the transmitter equalization procedure completed successfully, use software to read the following registers and ensure that all bits are set:

- For Gen3: `Link Status 2 Register [4:1]`
- For Gen4: `16.0 GT/s Status Register [3:0]`

To re-initiate the equalization procedure, write **1b** to the `Perform Equalization bit [0]` in the `Link Control 3 register`.

Workaround

None.

Status

Table 50. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.6. Link May Not Degrade With Corrupt Lanes (P-Tile)

Description

When using P-Tile IP for PCIe, if one or more lanes is corrupted (for example: faulty connection in the TX/RX pin) or not connected, the link may not downgrade as expected. For example, if lane 3 and 8 of a x16 link are not connected, the link may downgrade to x2 (active lanes 0-1), instead of x4 (active lanes 12-15).

Ensure that the P-Tile PCIe IP link width is configured according to your board implementation.

Workaround

None.

Status

Table 51. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.7. Warm Reset or PERST Assertion Clears the Sticky Registers

Description

When using P-Tile IP for PCIe, a warm reset or PERST assertion clears the sticky registers of the configuration space.

Impacted Modes

- P-Tile Avalon Streaming Interface IP for PCIe in Endpoint, Root port, and TLP bypass mode
- P-Tile Avalon Memory-Mapped Interface IP for PCIe in Endpoint, and Root port mode

Workaround

You must reconfigure the required sticky registers to the previous state if needed.

Status

Table 52. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.3.8. Multiple Fatal Error Messages

Description

When the P-Tile IP for PCIe receives different scale factor for Flow Control (FC) update than the FC initialization, the IP sends multiple fatal error message instead of one.

Workaround

None.

Status

Table 53. Device Status Table

Devices Affected	Planned Fix
• AGF*x*014R24A*xxxxx* • AGF*x*023R25A*xxxxx* • AGF*x*027R25A*xxxxx*	None

2.1.4. Configuration and Security

2.1.4.1. FPGA Reconfiguration May Cause Device to Halt

Description

During reconfiguration of the Agilex 7 FPGA device that performs a firmware reload, the device may halt if the following conditions are true:

- Attestation or Black Key Provisioning (BKP) is enabled.
- There are no clocks on TCK (JTAG clock) since the last reset.

For example, if you enable Attestation or BKP as well as tie TCK low through a pull-down resistor, as recommended in the Pin Connections Guidelines, the device may halt during the FPGA reconfiguration.

Workaround

To workaround for this issue:

- You must use the Quartus Prime Pro Edition software version 21.3 or later, which includes the required firmware for Attestation or BKP.
- Do not connect the TCK pin to ground. You may leave the TCK pin unconnected.

  Note: The unconnected TCK pin does not affect the device functionality. Recommendation from Pin Connections Guidelines (not mandatory): Connect TCK pin through a 10kΩ pull-up resistor to the `VCCIO_SDM` supply, for additional noise suppression.

Status

Table 54. Device Status Table

Devices Affected	Planned Fix
• AGF*x*012*xxxxxxx* • AGF*x*014*xxxxxxx* • AGF*x*022*xxxxxxx* • AGF*x*027*xxxxxxx* • AGI*x*022*xxxxxxx* • AGI*x*027*xxxxxxx*	None

2.1.4.2. Secure Device Manager May Disable Physically Unclonable Function

Description

When firmware co-signing is enabled, the Secure Device Manager (SDM) may disable the Physically Unclonable Function (PUF) access in the following situation:

- An explicit key cancellation ID of 0 is assigned to any key in the signature chain which is used to co-sign firmware.

Workaround

For PUF access, you can use any other explicit key cancellation IDs (non-zero) in a signature chain that is used to co-sign firmware.

Status

Table 55. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.1.4.3. Reset Timing Violation for QSPI Flash Specification

Description

In Agilex 7 F- and I-Series devices, when the SDM runs the boot ROM firmware, it takes about 800ns to reset the flash memory using the `AS_nRST` reset pin before reading from the flash memory. This might violate the reset timing specification from QSPI flash memory vendors Macronix, Winbond, and ISSI. Due to this issue, the SDM might fail to read the flash memory and might get stalled at the boot ROM phase.

Workaround

Toggle the `nCONFIG` pin to recover from this issue and reconfigure the device.

Status

Table 56. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.2. Hard Processor System

2.2.1. Write Data Can Appear at an AXI Interface before the Write Address, which can Cause a Deadlock Condition

Description:

In the Arm AMBA* AXI* and ACE* Protocol Specification (Arm IHI 0022H.c), the following is described:

A3.3 Relationships between the channels

The AXI protocol requires the following relationships to be maintained:

- A write response must always follow the last write transfer in a write transaction.
- Read data must always follow the read address of the data.
- Channel handshakes must conform to the dependencies of channel handshake signals.

The protocol does not define any other relationship between the channels. The lack of relationship means, for example, that the write data can appear at an interface before the write address for the transaction. This can occur if the write address channel contains more register stages than the write data channel. Similarly, the write data may appear in the same cycle as the address.

There are times when the Agilex 7 device must perform a "fence and drain" operation on the FPGA-to-SDRAM bridge, which means that it blocks all future transactions and completes all current transactions across the AXI bridges. During this operation, the system does not account for the above AXI protocol specification, where the write data can appear at the interface before the write address for the transaction. This can cause corrupt/invalid data to be left in the system, which can cause undefined behavior or system halt.

Workaround:

The solution is to require the AXI initiator (the user logic in the fabric portion of the device) to align the AXI write data channel and the AXI write address channel at the FPGA-to-SDRAM bridge, or where it enters the Platform Designer generated interconnect. You must ensure **WVALID** is not asserted before **AxVALID** is asserted.

Status

Table 57. Device Status Table

Devices Affected	Planned Fix
• AGF*xxxxxxxxxxxx* • AGI*xxxxxxxxxxxx*	None

2.2.2. HPS EMAC Rx interface stuck in unresponsive state

Description

The HPS EMAC RX might become unresponsive for the following network conditions:

- Line Rate: 1Gbps
- Feature: Hardware Timestamp for Precision Time Protocol (PTP) enabled
- Packet Types: Back-to-back (b2b) packets, multicast packets, or any packet with the least significant bit (LSB) set to '1' in the header of the next packet

When receiving network packets with the above conditions, the EMAC interface might become blocked, as indicated by the EMAC DMA Register 5 (Status Register) (`dmagrp_status` at offset 0x1014). The signature of this error is when the following bits are set in the Status Register:

- Bit 19:17: "3'b100: SUSPEND - Suspended: Receive Descriptor Unavailable"
- Bit 22:20: "3'b110: SUSPTX - Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow"
- Bit 25:23: "0 0 0: Error during Rx DMA Write Data Transfer"

The issue occurs when the status of an earlier packet has not yet been forwarded, and bit 0 of the first word of the next packet read from the Rx FIFO has a value of '1'. This sequence causes the internal state machine to hang.

The issue can be triggered by sending User Datagram Protocol (UDP) data packets and PTP traffic with hardware timestamping enabled on the device.

Impact

Under high traffic conditions, this issue can impact the functionality of the EMAC, potentially causing network communication disruptions.

Workaround

To mitigate this issue for 1Gbps line rate, you should use software-based timestamping instead of the hardware timestamp feature. If hardware PTP is required, use 10Mbps or 100Mbps line rate. For other use cases that match this error signature, try using the 10Mbps/100Mbps line rate.

Status

Table 58. Device Status Table

Devices Affected	Planned Fix
Agilex 7 production devices with HPS: • AG*x*B*xxxxxxxxxx* • AG*x*D*xxxxxxxxxx* • AG*x*E*xxxxxxxxxx* • AG*x*F*xxxxxxxxxx*	None

3. Arm Cortex-A53 MPCore and CoreSight Errata

This section lists the Arm Cortex-A53 MPCore and CoreSight errata.

Note: This errata only applies if you are using devices which are enabled with the Hard Processor System (HPS).

Each listed erratum has an associated category number which identifies the degree of the behavior.

The categories are as follows:

- Category 1: Behavior has no workaround and severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.
- Category 2: Behavior contravenes the specified behavior and might limit or severely impair the intended use of the specified features, but does not render the product unusable in all or the majority of applications.
- Category 3: Behavior that was not the originally intended behavior but should not cause any problems in applications.

Note: This device only contains category 2 and category 3 errata.

Table 59. Arm Cortex-A53 MPCore Processor and CoreSight Errata

Errata Listing	Category Number
843819: Memory Locations May be Accessed Speculatively Due to Instruction Fetches When HCR.VM is Set on page 74	Category 2
845719: A Load May Read Incorrect Data on page 75	Category 2
855871: ETM Does Not Report IDLE State When Disabled Using OSLOCK on page 76	Category 2
855872: A Store-Exclusive Instruction Might Pass When it Should Fail on page 77	Category 2
711668: Configuration Extension Register Has Wrong Value Status on page 79	Category 3
720107: Periodic Synchronization Can Be Delayed and Cause Overflow on page 80	Category 3
855873: An Eviction Might Overtake a Cache Clean Operation on page 82	Category 3
853172: ETM May Assert AFREADY Before All Data Has Been Output on page 83	Category 3
836870: Non-Allocating Reads May Prevent a Store Exclusive From Passing on page 84	Category 3
836919: Write of the JMCR in EL0 Does Not Generate an UNDEFINED Exception on page 86	Category 3
845819: Instruction Sequences Containing AES Instructions May Produce Incorrect Results on page 87	Category 3
851672: ETM May Trace an Incorrect Exception Address on page 88	Category 3
851871: ETM May Lose Counter Events While Entering WFx Mode on page 89	Category 3

continued...

Errata Listing	Category Number
852071: Direct Branch Instructions Executed Before a Trace Flush May be Output in an Atom Packet After Flush Acknowledgment on page 90	Category 3
852521: A64 Unconditional Branch May Jump to Incorrect Address on page 91	Category 3
855827: PMU Counter Values May Be Inaccurate When Monitoring Certain Events on page 92	Category 3
855829: Reads of PMEVCNTR<n> are not Masked by HDCR.HPMN on page 94	Category 3
855830: Loads of Mismatched Size May not be Single-Copy Atomic on page 95	Category 3

3.1. 843819: Memory Locations May be Accessed Speculatively Due to Instruction Fetches When HCR.VM is Set

Description

The Armv8 architecture requires that when all associated stages of translation are disabled for the current exception level, software only performs instruction fetches within the same or next translation granule as an instruction which has been or can be fetched due to sequential execution. In the conditions detailed below, this erratum may cause the Cortex-A53 MPCore processor to access other locations speculatively due to instruction fetches.

For this erratum to occur:

- The CPU must be executing at EL3, EL2 or Secure EL1.
- The CPU can be in either AArch32 or AArch64 execution state.
- Address translation is disabled for the current exception level (by clearing the appropriate `SCTLR.M`, `HSCTLR.M` or `SCTLR_ELx.M` bit).
- The `HCR.VM` or `HCR_EL2.VM` bit is set.

Impact

If the above conditions are met, then speculative instruction fetches may be made to memory locations not permitted by the architecture.

Workaround

Because the `HCR.VM` bit default reset value is low, this situation is most likely to occur in power down code, if EL2 or EL3 software disables address translation before the core is powered down. To work around this erratum, software must clear the `HCR.VM` bit before disabling address translation at EL3, EL2 or Secure EL1.

Category

Category 2

3.2. 845719: A Load May Read Incorrect Data

Description

When executing in the AArch32 state at EL0, the Cortex-A53 MPCore processor may read incorrect data if a load is performed to the same offset within a different 4 GB region as a recent previous load in the AArch64 state.

The following sequence must occur for this erratum to be triggered:

Note: This sequence requires execution in both AArch32 and AArch64, therefore at least one exception level change is required.

1. At EL0 or EL1, in the AArch32 or AArch64 state, the CPU executes a load, store, preload or data- or instruction-cache maintenance by MVA instruction.
2. At EL0 or EL1 in the AArch64 state, the CPU executes a load with:

```
VA[63:32] != 32'h00000000
```

3. At EL0 in AArch32 state, the CPU executes a load to the same 4 KB region as the instruction in step 1, with `VA[31:6]` matching the VA from the instruction in step 2.

The erratum does not apply if any of the following occurs between step 1 and step 3 in the sequence:

- A write to any of the following registers:
  - Any `SCTLR`
  - Any `TTBR`
  - Any `TCR`
  - Any `MAIR`
  - `CONTEXTIDR`
- A TLB maintenance instruction is executed, followed by a `DSB`.

This erratum also does not apply if an address translation instruction executes between steps 2 and 3 in the sequence.

Impact

If the above conditions are met, data corruption can occur. The load at EL0 can access data written at EL1 for which it does not have read permissions; however, a load in non-secure state cannot access secure data.

Workaround

If one of the exception conditions listed after the sequence above is applied between steps 2 and 3, this erratum does not occur. Because there must be an exception return from AArch64 to AArch32 between positions 2 and 3 in the above sequence, the recommended workaround is to insert a write of the `CONTEXTIDR_EL1` register into operating system exception return sequences.

Category

Category 2

3.3. 855871: ETM Does Not Report IDLE State When Disabled Using OSLOCK

Description

The OS Lock feature in the Embedded Trace Macrocell (ETM) allows software running on the Cortex-A53 MPCore to disable external debug access and save the register state before powering down the ETM. Software must follow a defined sequence to ensure that the register state is stable and all trace data is output before the system is powered down. Because of this erratum, when the OS Lock mechanism is used, the ETM never indicates to software that it is safe to be powered off. This erratum occurs when:

- The ETM is enabled (`TRCPRGCTLR.EN` = 1).
- The OS Lock feature disables the ETM (`TRCOSLAR.OSLK` = 1).

Impact

When the OS lock feature is enabled and software polls `TRCSTATR.IDLE`, it remains high even after the ETM is disabled and drained of trace data. If the ETM is already disabled by clearing the `TRCPRGCTLR.EN` bit then a software save and restore sequence behaves correctly.

Workaround

To execute the disable sequence properly:

1. Disable the ETM by setting the `TRCOSLAR.OSLK` bit.
2. Save the state of the `TRCPRGCTLR.EN` bit.
3. Clear the `TRCPRGCTLR.EN` bit.

Category

Category 2

3.4. 855872: A Store-Exclusive Instruction Might Pass When it Should Fail

Description

The Cortex-A53 MPCore processor implements an internal exclusive monitor to manage load-exclusive, store-exclusive, and clear-exclusive instructions. Because of this erratum, a load-exclusive instruction to cacheable memory might set the monitor to the exclusive state when the processor does not have exclusive access to the line. A subsequent store-exclusive instruction might pass when it should fail.

This erratum affects all load-exclusive and store-exclusive instructions, including load-acquire exclusive and store-release exclusive instructions.

The conditions that trigger this erratum are listed below:

- A core executes a store to memory that is marked as both inner-writeback and outer-writeback.
- The store is not a store-exclusive (or a store-release exclusive) or a store-release instruction.
- The store is not followed by a `DMB SY` or `DSB`.
- The store misses in the L1 data cache.
- The store does not trigger a linefill. This requires one or more of the following to be true:
  - Core is in read-allocate mode
  - Memory is marked as no-write-allocate
  - Memory is marked as transient
  - Store is a `STNP` instruction
  - Store is triggered by a `DC ZVA` instruction
- The core starts a linefill to the same address as the store. The linefill is started for one of the following:
  - A `PRFM`, `PLD`, or `PLDW` instruction
  - An automatic data prefetch
  - A pagewalk
- The core executes a load-exclusive (or a load-acquire exclusive) instruction to the same address as the store.
- The store data is forwarded to the load-exclusive instruction.
- If a core starts a linefill to the same address as the store, the load-exclusive instruction retires before the linefill is serialized.

Impact

If the above conditions are met then the Cortex-A53 MPCore processor might set the internal exclusive monitor. This behavior is incorrect because the processor is not guaranteed to have exclusive access to the line. If another master executes a load-exclusive instruction to the same address then both masters might gain access to an exclusive region of code at the same time.

Workaround

To work around the issue, avoid the conditions mentioned above. Disabling read-allocate mode by setting `CPUACTLR.RADIS` to 0x3 degrades write-stream performance. Therefore, the preferred workaround is to use an appropriate store-exclusive (or a store-release exclusive) or a store-release instruction or `DMB` instruction.

Category

Category 2

3.5. 711668: Configuration Extension Register Has Wrong Value Status

Description

The Program Trace Macrocell (PTM) implements several read only registers that provide a mechanism for tools using the PTM to determine which features are present in a specific implementation. The `Configuration Code Extension` register (0x7A, address 0x1E8) has an incorrect value of 0x000008EA. The correct value is 0x00C019A2.

Impact

This erratum has no impact on the generation of trace or the configurations that can be enabled. Tools that read this register in order to determine the capabilities of the PTM detect fewer features than are actually present.

The missing bits include:

- Bit[23] - Return stack implemented
- Bit[22] - Timestamp Implemented
- Bit[12] - Reserved, for compatibility with the ETM architecture

Bits[10:3] are incorrect and should indicate 52 external inputs.

Workaround

Tools using the PTM-A9 can read the `peripheral ID` registers (at offsets 0xFE0 to 0xFEC) to determine the version of the PTM-A9 and the features which are implemented, rather than relying on the `Configuration Code Extension` register.

Category

Category 3

3.6. 720107: Periodic Synchronization Can Be Delayed and Cause Overflow

Description

The Program Trace Macrocell (PTM) is required to insert synchronization information into the trace stream at intervals in order to allow a partial trace dump to be decompressed. The synchronization period can be controlled either external to the PTM or by a counter that by default, requests synchronization every 1024 bytes of trace.

Synchronization does not need to be inserted precisely at a regular interval, so allowance is made to delay synchronization if the PTM is required to generate other trace packets, or if there is not sufficient space in the FIFO. To guarantee that some synchronization packets are always inserted regardless of the conditions, a 'forced overflow' mechanism shuts off trace if a new synchronization request occurs before the previous request was satisfied. This forced overflow mechanism is minimally intrusive to the trace stream, but ensures that synchronization is inserted after no more than 2x the requested interval.

Due to this erratum, some specific sequences of instructions prevent the PTM from being able to insert any synchronization into the trace stream while that instruction sequence continues. Typically, there is just a short delay which may not be noticed and the synchronization is inserted once the particular pattern of waypoints changes. It is possible that overflows are generated in the trace regardless of the utilization of the FIFO in the PTM. In this scenario, typically only a single byte of trace (up to 5 waypoints) is lost.

The scenario does not correspond to sustained high rates of trace generation which could genuinely cause the FIFO to become full.

Scenarios that cause this erratum are rare, and are limited to code iterating around a loop many times. The loop would contain several branches and be dependent on memory accesses completing.

This erratum can occur under the following conditions:

1. Tracing is enabled.
2. Branch broadcasting is disabled.
3. Cycle accuracy is disabled.
4. The processor executes tight loops of repeating code, lasting longer than the configured synchronization period.

Impact

This erratum reduces the frequency of periodic synchronization and potentially causes trace overflows where some trace is lost. In the case of an overflow, trace following the overflow can be correctly decompressed. This erratum is more noticeable if the periodic synchronization requests are more frequent.

Workaround

The most appropriate workaround depends on the use case for the trace:

- If the trace buffer is large enough, consider increasing the synchronization period by setting the `ETMSYNCFR` to a higher value.
- If no trace must be lost (and periodic synchronization does not have to be guaranteed), set `bit[0]` of `ETMAUXCR` to disable the forced overflow function. Synchronization is inserted at the earliest opportunity, depending on the executed instruction stream.

Category

Category 3

3.7. 855873: An Eviction Might Overtake a Cache Clean Operation

Description

The Cortex-A53 MPCore processor supports instructions for cache clean operations. To avoid data corruption, the processor must ensure correct ordering between evictions and cache clean operations for the same address.

Because of this erratum, the processor can issue an eviction and an L2 cache clean operation to the interconnect in the wrong order. The processor can also issue transactions that become outstanding in the interconnect at the same time. This situation violates the AXI Coherency Extensions (ACE) protocol specification.

This erratum occurs when the following conditions are met:

1. One or both of the following are true:
   - `L2ACTLR[14]` is set to 1. This setting allows WriteEvict transactions on the ACE interface when the processor evicts data that it holds in the UniqueClean state.
   - `L2ACTLR[3]` is set to 0. This setting allows Evict transactions on the ACE interface when the processor evicts clean data.
2. A CPU executes a cache clean-by-address operation for a line that is present and dirty in the L2 cache.
3. A CPU performs any type of memory access to the same set. Memory access types can include a pagewalk, instruction fetch, cache maintenance operation or data access.
4. An instruction fetch to the same set triggers an L2 cache eviction.
5. A present and dirty cache line that is selected for L2 cache eviction at the same time it is targeted for a cache clean operation.

Impact

Because of this erratum transactions are erroneously reordered in the interconnect, resulting in data corruption.

Workaround

You can work around this issue by changing the cache clean-by-address operations to cache clean-and-invalidate operations. To enable these operations, set `CPUACTLR.ENDCCASCI` to 1.

Category

Category 2

3.8. 853172: ETM May Assert AFREADY Before All Data Has Been Output

Description

When the AFVALID signal on the Advanced Trace Bus (ATB) interface asserts, the ETM immediately outputs all buffered trace. The ETM must assert the AFREADY output one cycle after all trace that was buffered on the cycle in which AFVALID was first asserted.

Because of this erratum, the AFREADY signal may be asserted before all the necessary trace has been output.

Impact

Because of this erratum, the ETM may contain trace data that was generated before the flush request.

Workaround

The system can ensure that all trace has been drained from the ETM by disabling it. You can disable the ETM by clearing the TRCPRGCTLR.EN bit. Next, system software must poll the TRCSTATR.IDLE bit until it reads as 1. This value indicates the ETM is idle and all trace that was generated before the write to TRCPRGCTLR has been output.

Category

Category 3

3.9. 836870: Non-Allocating Reads May Prevent a Store Exclusive From Passing

Description

A Cortex-A53 MPCore processor executing a load and store exclusive instruction in a loop is allowed to repeatedly fail under certain conditions. An example of an allowed condition is when another processor repeatedly writes to the same cache line.

Because of this erratum, a non-allocating load from another processor may cause the store-exclusive instruction to repeatedly fail.

The failure occurs under these conditions:

- One CPU executes a loop containing a load-exclusive and a store-exclusive instruction. The loop continues until the store-exclusive instruction succeeds.
- Another CPU or master in the system repeatedly executes a load to the same L1 data cache index as the store-exclusive instruction.
- The cache line containing the address of the load is present in the L1 cache of the CPU, and is not present in the L2 cache.
- The load does not cause an allocation into the cache of the CPU or the master executing the load. This response results in a snoop arriving at the CPU holding the cache line every time the load is performed.
- The load is repeated at exactly the same frequency as the load- and store-exclusive loop, such that every time around the loop, the snoop arrives at the same time as the store exclusive instruction is executing.

A load can be non-allocating in Cortex-A53 MPCore processor in the following conditions:

- A load instruction executes on a CPU, while the `CPUACTLR.DTAH` bit is not set, with one of the following conditions:
  - The memory address is marked as writeback cacheable, with no read allocate, in the page tables.
  - The memory address is marked as writeback cacheable, transient, in the page tables.
  - The memory address is marked as writeback cacheable, and an `LDNP` non-temporal load instruction is used.
- A read transaction is made on the ACP interface.

Impact

If a CPU or other master is polling a location to determine when the value changes, then it can prevent another CPU from updating that location, causing a software livelock. Most polling routines, however, use memory that can be allocated into their cache. For improved efficiency it is recommended to use a load-exclusive and `WFE` instruction to avoid repeated polling. Because the frequency of the polling loop must match the frequency of the load store-exclusive loop, the conditions that cause this erratum are unlikely. Any other disturbance in the system, such as an interrupt or other bus traffic can easily alter the frequency of either loop sufficiently to break the livelock.

Workaround

If the repeating load is being executed on a Cortex-A53 CPU, then this erratum can be worked around by setting the `CPUACTLR.DTAH` bit. Note this version of the Cortex-A53 MPCore processor sets this bit by default.

If the repeating load is being executed by another master in the system connected to the ACP interface, then the erratum can be worked around by changing the frequency of the polling so that it no longer aligns with the frequency of the load and store exclusive loop.

If the repeating load is being executed by another master in the system connected through the coherent interconnect, then the erratum can be worked around either by ensuring that the other master allocates the line into its cache, or by changing the frequency of the polling so that it no longer aligns with the frequency of the load and store exclusive loop. Note that the Cortex-A53 MPCore processor always allocates the line into either the cache or a temporary buffer, and so does not require any workaround for typical polling loops.

Category

Category 3

3.10. 836919: Write of the JMCR in EL0 Does Not Generate an UNDEFINED Exception

Description

When EL0 is using AArch32 register width and a write is performed in EL0 to the Arm Jazelle® Main Configuration Register (`JMCR`), the write should be UNDEFINED. Because of this erratum, the write is permitted but ignored.

The erratum occurs under the following conditions:

- The processor is executing in AArch32 user mode.
- A write to the `JMCR` is executed, using the instruction `MCR p14,7,<Rt>,c2,c0,0`.

Impact

Rather than treating the `MCR` instruction as UNDEFINED, a write to the `JMCR` is ignored.

Workaround

No available workaround.

Category

Category 3

3.11. 845819: Instruction Sequences Containing AES Instructions May Produce Incorrect Results

Description

When the Cortex-A53 MPCore processor is executing in the AArch64 state, certain sequences of instructions that include AES instructions may cause incorrect results.

There are two code sequences that can cause this erratum in the AArch64 execution state:

- Code sequence 1:
  1. The CPU executes an `AESE` instruction.
  2. The CPU executes a `USQADD` instruction.
     - Both the `Vn` and `Vd` of this instruction must be the same register as `Vd` for the `AES` instruction.
     - The size field for this instruction must be '00', indicating byte-sized elements.
     - The `USQADD` instruction can be in either vector or scalar form.
- Code sequence 2:
  1. The CPU executes a `SUQADD` instruction.
     - The size field for this instruction must be 00, indicating byte-sized elements.
     - The `SUQADD` instruction can be in either vector or scalar form.
  2. The CPU executes an `AESMC` or `AESIMC` instruction.
     - Both the `Vn` and `Vd` of this instruction must be the same register as the `Vd` for the `SUQADD` instruction.

For both these sequences, the two instructions listed must be executed consecutively, with no other instructions or exceptions between them. If either of these sequences is met, the final result of the affected instruction sequence may be incorrect.

Impact

The sequences of instructions described in the conditions above are not expected to occur in real code because they do not perform useful computation. Therefore, there is no impact expected to real systems.

Workaround

Because the code sequences for this erratum are not expected to occur in real code, no workaround is required.

Category

Category 3

3.12. 851672: ETM May Trace an Incorrect Exception Address

Description

The address in an exception packet is the preferred exception return address. Because of this erratum, the address may be equal to the target address of the exception. The trace stream is not corrupted, and decompression can continue after the affected packet.

The following sequence is required for this erratum to occur:

1. The ETM must start tracing instructions because of one of the following:
   a. `ViewInst` starts.
   b. The security state changes indicating trace is now permitted.
   c. The values of the external debug interface (`DBGEN`, `SPIDEN`, `NIDEN`, `SPNIDEN`) change to indicate trace is now permitted.
   d. The CPU exits debug mode.
2. Before the CPU executes any other behavior that causes a trace to be generated, it executes a direct branch instruction, which may or may not be taken.
3. The next instruction is a load or store that causes a data abort or watchpoint exception.

After this sequence, provided certain timing specific conditions are met, the address in the exception packet may be incorrect.

Impact

The trace decompressor may incorrectly infer execution of many instructions from the branch target to the provided address.

Workaround

The trace decompressor can detect that this erratum has occurred by checking if the exception address is in the vector table and identifying if the branch was not expected to be taken to the vector table. A decompressor can infer the correct address of the exception packet. The target of the preceding branch (if the branch was taken), or the next instruction after the branch (if the branch was not-taken) provides the correct address of the exception packet.

Category

Category 3

3.13. 851871: ETM May Lose Counter Events While Entering WFx Mode

Description

If the ETM resources become inactive because of a low-power state, there is a one-cycle window during which the counters and the sequencer may ignore counter-at-zero resources.

The following sequence is required for this erratum to occur:

1. The core executes a `WFI` or `WFE` instruction.
2. The ETM enters a low-power state.
3. In a one-cycle window around this point, either:
   a. A counter in self-reload mode generates a counter-at-zero resource.
   b. A counter in normal mode gets a `RLDEVENT` on the cycle in which it has just transitioned to zero.
4. A counter or sequencer is sensitive to the counter-at-zero resource.

Impact

Counters sensitive to a counter-at-zero resource may not reload or decrement. If the sequencer is sensitive to a counter-at-zero resource, it may not change state, or may change to an incorrect state.

Workaround

The ETM can be prevented from entering low-power mode by setting the `LPOVERRIDE` bit of Trace Event Control 1 (`TRCEVENTCTL1R`) register. This workaround is only needed if there is a counter or sequencer sensitive to a counter-at-zero resource.

Category

Category 3

3.14. 852071: Direct Branch Instructions Executed Before a Trace Flush May be Output in an Atom Packet After Flush Acknowledgment

Description

The Embedded Trace Macrocell (ETMv4) architecture requires that when a trace flush is requested on the AMBA Trace Bus (ATB), a Cortex-A53 MPCore processor must complete any packets that are in the process of being encoded and output them prior to acknowledging the flush request. When trace is enabled, the Cortex-A53 MPCore processor attempts to combine multiple direct branch instructions into a single atom packet. If a direct branch instruction is executed, and an atom packet is in the process of being generated, the processor does not force completion of the packet prior to acknowledging the flush request. This erratum is a violation of the ETMv4 architecture.

The following conditions are required for this erratum to occur:

1. ETM is enabled.
2. Instruction tracing is active.
3. The processor executes one or more direct branch instructions.
4. An atom packet is in the process of being encoded but is not complete.
5. A trace flush is requested on the AMBA ATB.

Impact

When the above conditions occur, the ETM must complete encoding and output the atom packet prior to the trace flush request being acknowledged. Because of this erratum, the atom packet is output after the flush is acknowledged. Therefore, it appears to software monitoring the trace that the direct branch was executed after the requested flush.

Workaround

Enabling the timestamp by setting the `TS` bit in the Trace Configuration (`TRCCONFIGR`) register resolves the erratum because the atom packets complete when timestamp behavior is enabled.

Category

Category 3

3.15. 852521: A64 Unconditional Branch May Jump to Incorrect Address

Description

When executing in AArch64 state with address translation disabled, unconditional immediate branch instructions might jump to an incorrect address.

The following conditions are required for this erratum to occur:

1. The processor is executing in AArch64 state.
2. The `SCTLR_ELx.M` bit for the current exception level is 0.
3. The `HCR_EL2.VM` bit is 0.
4. A `B` or `BL` instruction from the unconditional branch (immediate) encoding class is executed.
5. This branch has an `imm26` field of `0x1FFFFFF`, encoding a branch target of `{pc}+0x7FFFFC`.

Impact

If these conditions are met, then the processor might incorrectly branch to the target `{pc}-0x8000004` instead of `{pc}+0x7FFFFC`.

Workaround

The workaround for this erratum is to avoid the conditions described.

Category

Category 3

3.16. 855827: PMU Counter Values May Be Inaccurate When Monitoring Certain Events

Description

The Cortex-A53 MPCore processor implements a Performance Monitor Unit (PMU). The PMU allows programmers to gather statistics on the operation of the processor during runtime. Because of this erratum, software may read inaccurate PMU counter values when monitoring certain events. Specifically:

- The INST_RETIRED event counts architecturally executed instructions. Because of this erratum, it may count more instructions than were architecturally executed.
- The ST_RETIRED event does not count store-exclusive instructions that fail. Because of this erratum, it does count these instructions.
- The UNALIGNED_LDST_RETIRED event counts loads and stores that fail their alignment check. Because of this erratum, it may also count `LDRD` and `STRD` instructions that pass their alignment check.
- The EXC_TAKEN and EXC_RETURN events are filtered precisely according to the exception level/security state they were executed in. Because of this erratum, they are filtered according to the destination exception level/security state.

This erratum is present when:

- A performance counter is enabled and configured to count an INST_RETIRED , ST_RETIRED, UNALIGNED_LDST_RETIRED, EXC_TAKEN, or EXC_RETURN event.
- The following conditions occur during the event capture:
  - INST_RETIRED: An immediate branch instruction is executed.
  - ST_RETIRED: A store-exclusive instruction is executed and fails.
  - UNALIGNED_LDST_RETIRED: A `LDRD` or `STRD` instruction is executed that is word aligned but not double word aligned.
  - EXC_TAKEN: An exception is taken.
  - EXC_RETURN: An exception return is executed.
- The INST_RETIRED, ST_RETIRED, and UNALIGNED_LDST_RETIRED filter settings for the performance counter are configured so that an event must be counted if it occurs.
- The EXC_TAKEN and EXC_RETURN filter settings are configured to one of the following descriptions:
  - Events must be counted in the original exception level and security state, but must not be counted in the exception level and security state following the exception or the exception return
  - Events must not be counted in the original exception level and security state, but must be counted in the exception level and security state following the exception or the exception return.

Impact

If the erratum conditions are met, the performance counter may erroneously increment or fail to increment. Specifically:

- INST_RETIRED: The counter may erroneously increment by two when only one instruction executes.
- ST_RETIRED: The counter may erroneously increment for the failed store-exclusive instruction.
- UNALIGNED_LDST_RETIRED: The counter erroneously increments for the `LDRD` or `STRD` instruction.
- EXC_TAKEN: The counter may erroneously increment or erroneously fail to increment.
- EXC_RETURN: The counter may erroneously increment or erroneously fail to increment.

Workaround

For the EXC_TAKEN and EXC_RETURN events, you can workaround the erratum by changing the filter settings for the performance counter to monitor the destination exception level and security state instead of the exception level and security state in which the exception or exception return are executed.

There are no workarounds for the other PMU events.

Category

Category 3

3.17. 855829: Reads of PMEVCNTR<n> are not Masked by HDCR.HPMN

Description

Software executing at EL2 can set the `HDCR.HPMN` and `MDCR_EL2.HPMN` fields to restrict non-secure EL0 and EL1 software from accessing a subset of the performance counters. If `n` > `HPMN`, then Performance Counter n `(PMEVCNTR<n>)` register is not accessible to non-secure EL0 or EL1. Because of this erratum, Cortex-A53 reads of inaccessible registers might not return zero as expected, but instead might read the actual contents of the counter registers.

For this erratum to be present:

1. The processor is executing at non-secure EL1 or EL0.
2. `HDCR.HPMN` and `MDCR_EL2.HPMN` are set to a value `n`, where `n` < 6.
3. A read of `PMEVCNTR<n>` and `PMEVCNTR<n>_EL0` is executed.

Impact

If the conditions described above are met, then non-secure EL0 and EL1 software can read the values of performance counters reserved for EL2.

Workaround

Software executing at EL2 can set the `HDCR.TPM` and `MDCR_EL2.TPM` bits. This configuration causes all non-secure EL0 and EL1 accesses to performance monitor registers to trap to EL2. The EL2 software can then emulate accesses as required, and can mask out accesses to reserved registers.

Category

Category 3

3.18. 855830: Loads of Mismatched Size May not be Single-Copy Atomic

Description

The Cortex-A53 MPCore processor supports single-copy atomic load and store accesses as described in the Arm architecture documentation. However, in some unusual code sequences, this erratum can cause the CPU executing a store, and later a load, to the same address but with a different access size to load data that does not meet the requirements of a single-copy atomic load.

For this erratum to be present, a store instruction must execute on one CPU. This instruction can be any halfword, word, or double word store instruction that is not a store release and the address must be aligned to the access size. On a second CPU, the following sequence must occur:

1. A store instruction executes. This store must be a smaller access size than the store on the first CPU, and must address bytes accessed by the first CPU. The address must also be aligned to the access size.
2. The store instruction does not allocate into the cache because of any one of the following conditions:
   - The memory address is marked as transient
   - The write allocate hint in the translation table is not set or the memory is marked as non-cacheable
   - The CPU recently executed a stream of stores and has subsequently dynamically switched into a no-write allocate mode
3. A load instruction executes. The load must be a larger access size than the store from the same CPU, and at least some bytes of the load must be to the same address as the store. The address must also be aligned to the access size.

The Arm architecture requires that the load is single-copy atomic. However, in the conditions described, the load may observe a combination of the two stores, indicating that the store on the initial CPU was serialized first. If the load is repeated, it might only see the data from the first CPU's store, indicating that the store on the first CPU was serialized second.

Impact

Concurrent, unordered stores are uncommon in multi-threaded code. In the ISO/IEC 9899:2011 (C11) standard, they are restricted to the family of relaxed atomics. Using different size load and store instructions to access the same data is also uncommon. For these reasons, the majority of multi-threaded software does not meet the conditions for this erratum.

Workaround

Most multi-threaded software does not satisfy the conditions of this erratum and therefore, does not require a workaround. If a workaround is required, then replace the store on the second CPU with a store-release instruction.

Category

Category 3

4. Agilex 7 F-Series and I-Series User Guidelines

This guideline section is applicable to the following Ordering Part Numbers (OPNs):

Table 60. Agilex 7 F-Series and I-Series Devices

Agilex 7 F-Series and I-Series Devices
AGF*xxxxxxxx* AGI*xxxxxxxx*

Currently, there is no specific user guideline.

5. Document Revision History for the Agilex 7 F-Series and I-Series Known Issue List

Document Version	Changes
2025.09.29	Added the following F-Tile known issues: • Ethernet Auto-Negotiation and Link Training (AN/LT) designs on F-Tile FGT may not link up when using Quartus Prime Pro Edition software version 25.1.1 and 25.3 on page 35 • IEEE 802.3-2022 50GBASE-KR compliance testing instability during Link Training (LT) on page 36
2025.09.04	Updated the following F-Tile known issue: • FGT PAM4 Compliance Support
2025.08.11	Made the following changes: • Added the following known issues for the F-Tile devices: — F-Tile 400G Ethernet Hard IP RX Priority Flow Control Issue — F-Tile Ethernet Hard IP Bidirectional Link Fault Signaling Issue — F-Tile SDI II IP and F-Tile PMA/FEC Direct PHY IP with "SDI" configuration rule are not of production quality — F-Tile HDMI IP and F-Tile PMA/FEC Direct PHY IP with "HDMI" configuration rule are not of production quality • Added the following known issue for the R-Tile devices: — R-Tile might report Fatal Error in the Advance Error Reporting (AER) registers when using Address Translation Services (ATS) • Added the following known issue for Configuration and Security: — Reset Timing Violation for QSPI Flash Specification • Added the following known issue for the Hard Processor System: — HPS EMAC Rx interface stuck in unresponsive state • Updated the following F-Tile known issues: — FGT PAM4 Compliance Support — Occasional Equalization Timeout or PCIe Link Training Failure to Achieve Expected Link Speed during Link Disable, Host Reset, and Speed Change • Updated the following R-Tile known issues: — R-Tile PCIe - Intermittent PCIe Gen4 EQ time out — Bifurcated ports using Independent PERST pins might fail to link up after configuration is complete — Port0 might be stuck in Detect when configuring bifurcated ports using Independent PERST pins
2025.03.13	Added the following known issues for the F-Tile devices: • F-Tile Ethernet Hard IP unable to achieve 100% throughput with some variants Added the following known issues for the R-Tile devices: • Bifurcated ports using Independent PERST pins might fail to link up after configuration is complete • Port0 might be stuck in Detect when configuring bifurcated ports using Independent PERST pins • CXL 1.1 version does not support uncorrectable error reporting when receiving two LLCTRL-Init packet Updated the OPNs for the following known issues:

continued...

Document Version	Changes
	• Gen3/Gen4 link might be established without successfully performing Transmit Equalization (TX EQ) • Link may not downgrade with corrupt lanes • Malformed TLP incorrectly flagged as ECRC error • Assertion of PERST / warm reset during the Functional Level Reset results in PCIe Link Failure • No Support for Page Request Services in Port 2 and Port 3 of 4x4 Configuration • Multiple Fatal Error Messages • PCIe x4 cores may report Uncorrectable Fatal Error or Malformed TLP • Receiver Errors logged during back-to-back Secondary Bus Resets (SBR) operations when running at Gen 2 speed • R-Tile PCIe - LCRC Error/Malformed TLP • R-Tile PIPE-Direct - `rxdatavalid` Signal Unexpected Toggling After P1 to P0 Transition • Polling.Active time out during Link Disable-Enable loop tests • R-Tile PCIe - Intermittent PCIe Gen4 EQ time out • No response received during read operation on the `xcvr_reconfig` interface after an FPGA re-configuration • Slow Completion response from Configuration requests targeting R-Tile Endpoint connected to Downstream port with finite Completion Header/Data credits
2025.01.28	Added the following known issues for the F-Tile devices: • F-Tile Ethernet Hard IP `rst_tx_stats` and `rst_rx_stats` register bits might not function correctly • F-Tile Ethernet Hard IP `force_rf` register bit might not function correctly • F-Tile Ethernet Hard IP `tx_pause_request` register bit might not function correctly • F-Tile Ethernet Hard IP PTP statistics might not clear correctly
2025.01.10	Made the following changes: • Added the following known issues for the F-Tile devices: — 200G/400G Ethernet Mode Does Not Support Port-Based Priority Flow Control — The F-Tile 200G Hard IP block is de-featured and cannot be used in production devices with OPNs that have no suffix (blank) or "B" suffix — The Deterministic Latency Feature supports on E200 block Six of Eight FGT Channels — Requirement for F-Tile Devices which are Powered and Unconfigured Known Issue List — F-Tile FHT TX EOJ Spec Compliance Issue — FGT PAM4 Bounding Solution — FGT Transceivers Do Not Support Direct EXTEST JTAG Instruction in Boundary Scan Test — F-Tile: Unsuccessful TX Equalization — Link May Not Downgrade With Corrupt Lanes (F-Tile) — Intermittent Equalization Timeout of Speed Degrade during Link Disable, Hot Reset, and Speed Change — Link Fault Detection window of the F-Tile Ethernet Hard IP in 10GE-1 or 25GE-1 mode — FHT PMA Transmitter-to-Receiver Internal Serial Loopback operation for error-free BER results

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Document Version	Changes
	• Added the following known issues for the R-Tile devices: — Gen3/Gen4 link may be established without successfully performing Transmit Equalization (TX EQ) — Link may not downgrade with corrupt lanes (R-Tile) — Malformed TLP incorrectly flagged as ECRC error — Assertion of PERST/warm reset during the Functional Level Reset results in Link Failure — No Support for Page Request Services in Port 2 and Port 3 of 4x4 Configuration — Multiple Fatal Error Messages — x4 cores may report Uncorrectable Fatal Error or Malformed TLP — Receiver Errors logged during back-to-back Secondary Bus Resets (SBR) operations when running at Gen 2 speed — R-Tile Digital Temperature Sensor Readings — R-Tile PCIe - LCRC Error/Malformed TLP — R-Tile PIPE-Direct - rxdatavalid Signal Unexpected Toggling After P1 to P0 Transition — Polling.Active time out during Link Disable-Enable loop tests • Added the following known issues for the P-Tile devices: — Root Port Legacy Interrupt Status register INTx is stuck HIGH — TLP Bypass Error Status register may report received errors after the PERST is released — Register Implementation while using the SR-IOV Feature — Register Implementation while using the Multi-function Feature — P-Tile: Unsuccessful TX Equalization — Link May Not Degrade With Corrupt Lanes (P-Tile) — Warm Reset or PERST Assertion Clears the Sticky Registers — Multiple Fatal Error Messages
2023.05.03	• Updated product family name to "Agilex 7". • Made the following updates in *About this Document* : — Updated the Agilex 7 Ordering Part Number (OPN) Decoder figure. — Updated the devices affected list in the Agilex 7 F-Series and I-Series Devices table. • Updated the devices affected list for *FPGA Reconfiguration May Cause Device to Halt*.
2022.07.21	• Added a new erratum: *Write Data Can Appear at an AXI Interface before the Write Address, which can Cause a Deadlock Condition*
2021.10.28	Initial release.