TN_130 FT232H Errata Technical Note

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Version 1.2

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The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT232H devices.
The current revision of the FT232H is **revision C, launched March 2013.**

Use of FTDI devices in life support and/or safety applications is entirely at the user's risk, and the user agrees to defend, indemnify and hold harmless FTDI from any and all damages, claims, suits or expense resulting from such use.

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1 FT232H Revision

FT232H part numbers are listed in **Table 1.** The letter at the end of date code on the device markings identifies the device revision.

The current revision of the FT232H is **revision C, launched March 2013.** At the time of releasing this Technical Note there is one known minor issue with this silicon revision. A workaround is provided for this issue

Part Number	Package
FT232HL	48 Pin LQFP
FT232HQ	48 Pin QFN

Table 1 FT232H Part Numbers

This errata technical note covers the revisions of FT232H listed in **Table 2**.

Revision	Notes
A	First device revision (not released)
B	Second device revision (Released March 2011)
C	Third device revision (Released March 2013)

Table 2 FT232H Revisions

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2 Errata History Table – Functional Issues

Functional Problem	Short description	Errata occurs in device revision
FT232H	Error switching from 245 FIFO mode to MPSSE mode	A,B
FT232H	Incorrect status reported on FT1248 MISO line when SS_n is inactive	B
FT232H	Incorrect status reported on FT1248 MISO line when SS_n is inactive	C

2.1 Errata History Table – Electrical and Timing Specification Deviations.

Deviations	Short description	Errata occurs in device revision
Suspend timer failure (USB Chapter 9 Compliance)	The USB specification requires a maximum time to suspend of 3.125ms. The device takes up to 4ms to suspend.	A
Fault with internal 3V3 regulator.	Device VCC is designed to operate between 3V3 and 5V however with this errata the supply should not be set below 4.3V for correct operation.	A,B

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3 Functional Issues of FT232H

3.1 Revision A

3.1.1 Error switching from 245 FIFO mode to MPSSE mode

Introduction:

The FT232H may switch from one of the EEPROM configurable modes to MPSSE mode during runtime by calling the FT_SetBitMode call in the software application.

Issue:

If the device is configured to be in 245 FIFO mode (external EEPROM) and the application switches the mode to MPSSE, spurious accesses to the RD# or WR lines can cause the MPSSE protocol to corrupt. This only affects the device if 245 FIFO mode is the operational state define in the external EEPROM.

Workaround:

Assuming 245 FIFO mode was not required prior to accessing MPSSE then selecting UART mode in the external EEPROM would prevent the problem.

This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 3.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 3

3.1.2 Incorrect status reported on FT1248 MISO line when SS_n is inactive

Introduction:

The FT232H has an FT1248 mode. This mode uses a MISO line to indicate the status of the device (e.g buffers full / empty)

Issue:

The bug is minor and system will not lose data but the status while SS_n is inactive can indicate that data can be written or read. However when starting a command the status on the MISO line on the clock cycle after the command is not correct.

Workaround:

Ignore the status on the MISO line on the cycle after the command and only look at the ACK status on the data phase of the FT1248. This will correctly reflect the status which was present while SS_n was inactive.

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Package specific:

The effected packages are listed in Table 4.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 4

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3.2 Revision B

3.2.1 Incorrect status reported on FT1248 MISO line when SS_n is inactive

Introduction:

The FT232H has an FT1248 mode. This mode uses a MISO line to indicate the status of the device (e.g buffers full / empty)

Issue:

The bug is minor and system will not lose data but the status while SS_n is inactive can indicate that data can be written or read. However when starting a command the status on the MISO line on the clock cycle after the command is not correct.

Workaround:

Ignore the status on the MISO line on the cycle after the command and only look at the ACK status on the data phase of the FT1248. This will correctly reflect the status which was present while SS_n was inactive.

Package specific:

The effected packages are listed in Table 4.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 5

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3.3 Revision C

3.3.1 Incorrect status reported on FT1248 MISO line when SS_n is inactive

Introduction:

The FT232H has an FT1248 mode. This mode uses a MISO line to indicate the status of the device (e.g buffers full / empty)

Issue:

The bug is minor and system will not lose data but the status while SS_n is inactive can indicate that data can be written or read. However when starting a command the status on the MISO line on the clock cycle after the command is not correct.

Workaround:

Ignore the status on the MISO line on the cycle after the command and only look at the ACK status on the data phase of the FT1248. This will correctly reflect the status which was present while SS_n was inactive.

Package specific:

The effected packages are listed in Table 4.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 6

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4 Electrical and Timing specification deviations of FT232H

4.1 Revision A

4.1.1 Suspend Timer Failure

Introduction:

The FT232H has the ability to be put into suspend by the host to conserve power usage.

Issue:

The USB specification chapter 9 compliance tests require the device to go into suspend within 3.125ms. The device is taking up to 4ms to enter suspend state.

Workaround:

This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 7

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4.1.2 Internal 3V3 Regulator

Introduction:

The FT232H uses an internal regulator to generate 3V3 from a 5V source (VREGIN). The source should be variable from 3V3 to 5V.

Issue:

The supply to the regulator must not drop below 4.3V for the correct 3V3 regulated output to be produced. This only affects self-powered designs where the only board supply is 3V3.

Workaround:

VREGIN must not be supplied below 4.3V. VREGIN can be powered via the USB bus supply with VCCIO, VPLL and VPHY powered with 3.3 volts.

Package specific:

The effected packages are listed in Table 6.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 8

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4.2 Revision B

4.2.1 Internal 3V3 Regulator

Introduction:

The FT232H uses an internal regulator to generate 3V3 from a 5V source (VREGIN). The source should be variable from 3V3 to 5V.

Issue:

The supply to the regulator must not drop below 4.3V for the correct 3V3 regulated output to be produced. This only affects self-powered designs where the only board supply is 3V3.

Workaround:

VREGIN must not be supplied below 4.3V. VREGIN can be powered via the USB bus supply with VCCIO, VPLL and VPHY powered with 3.3 volts.

Package specific:

The effected packages are listed in Table 7.

Package	Applicable (Yes/No)
FT232HL	Y
FT232HQ	Y

Table 9

4.3 Revision C

No known issues at revision C.

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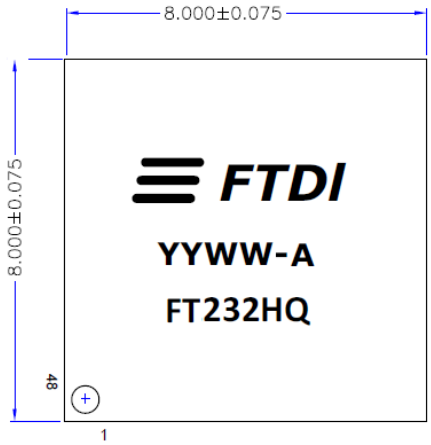
5 FT232H Package Markings

FT232H is available in a RoHS Compliant package, 48 pin LQFP and 48 pin QFN. An example of the markings on the package is shown in Figure 3-1.



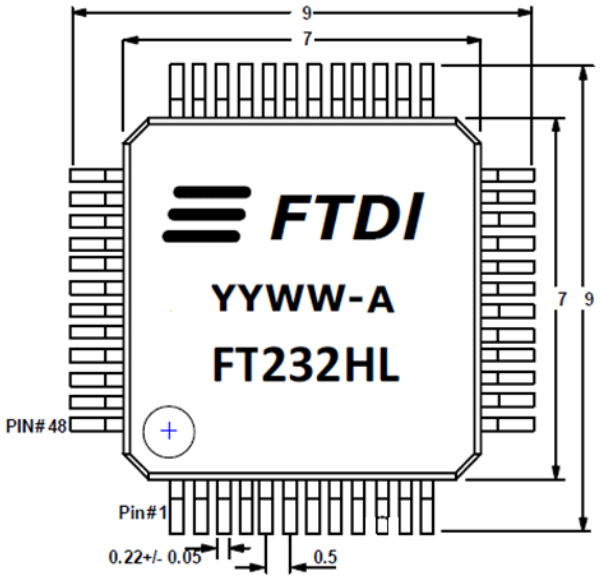
Line 1 – FTDI LOGO

Line 2 – Date code and revision

Line 3 – FTDI Part Number

Dimensions are in mm

Figure 5-1 Package Markings – FT232HQ



Line 1 – FTDI LOGO

Line 2 – Date code and revision

Line 3 – FTDI Part Number

Dimensions are in mm

Figure 5-2 Package Markings – FT232HL

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Appendix C – Revision History

Version 1.0	First Release	16/02/2011
Version 1.1	Update to include 3V3 regulator	28/01/2013
Version 1.2	Update Device to Revision C	15/03/2013

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