Application Note

AN_434

FT602_UVC_Bus_Master_Sample

Version 1.2

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This application note describes the design of an example UVC application that is interfaced to a FTDI FT602 device.

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1 Introduction

1.1 Overview

This document describes the design of an example UVC bus master that is interfaced to a FTDI FT602 device. The example design may be freely adapted by designers and system integrators who work with FTDI FT602 devices. FT602 supports up to 4 UVC channels and the example implements 4 instances of a test pattern generator which may be customised to output QVGA, VGA, HD and F-HD video streams.

1.2 Features

- Supports both FT245 and FT600 (multi-channel) FIFO modes
- Supports 32-bits wide interfaces for interfacing to FT602 devices
- Supports QVGA, VGA, HD and Full HD resolutions in 16-bit YUV format
- Supports up to 4 UVC channels with the total bandwidth up to 320MB per second
- Supports I^2C for sideband configuration
- Supports 100MHz and 66MHz FIFO clock operation
- Supports both Xilinx and Altera FPGAs

2 Design Architecture

2.1 Architecture

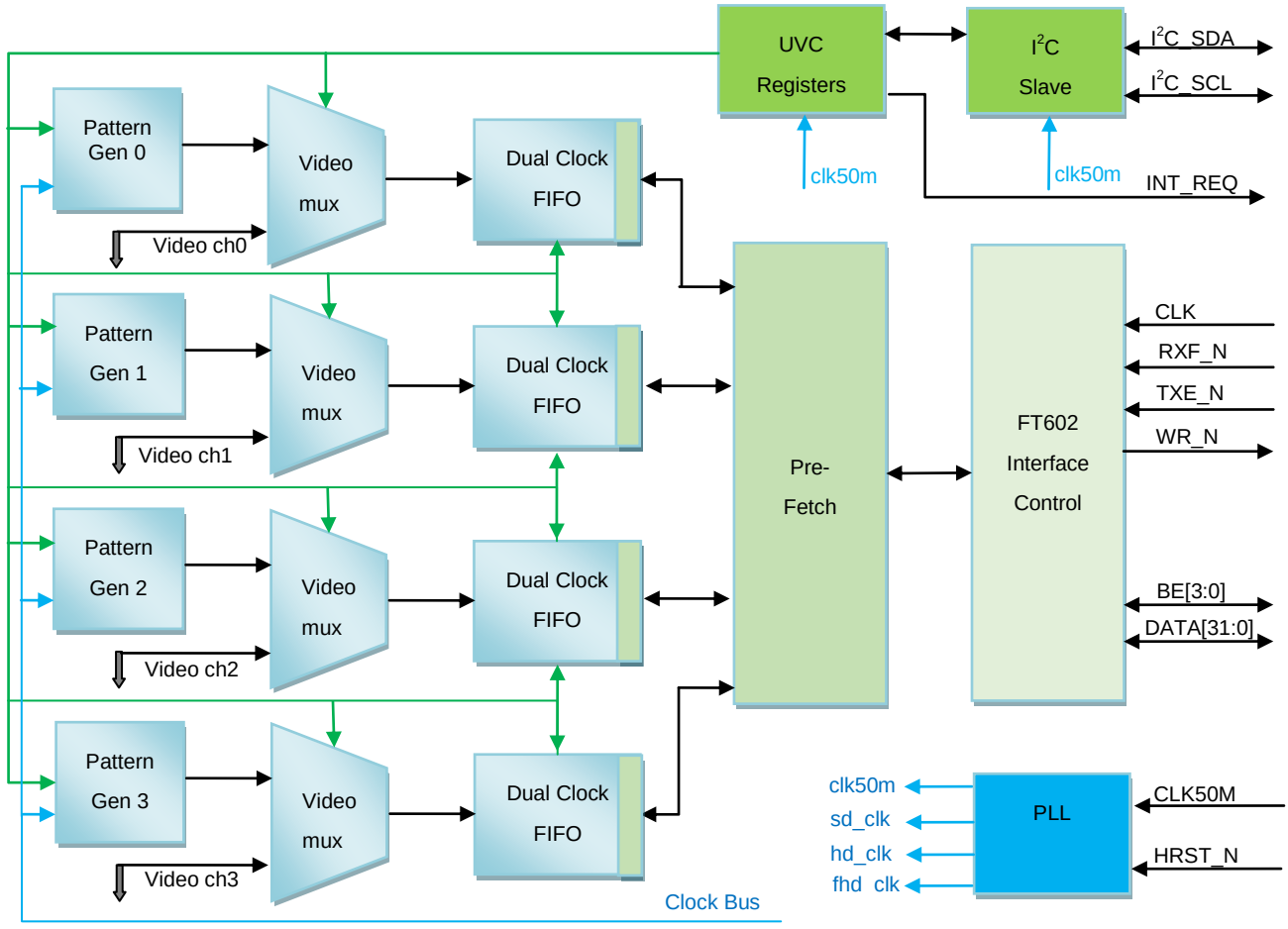


Figure 1 – Architecture

2.2 Pin Out

Name	Width	Type	Active	Description
HRST_N	1	Input	Low	Hard Reset
CLK50M	1	Input		Clock Input
I2C_SCL	1	Inout		I^{2}C Clock
I2C_SDA	1	Inout		I^{2}C Data
INT_REQ	1	Output	High	Interrupt Request
Other Pins	**Refer to FT602 IC Datasheet**			

Table 1 - Pin Out

2.3 Operation Description

The purpose of this sample design is to provide four video input channels to the FT602. Each channel can be configured to QVGA, VGA, HD or Full HD independently with YUV 4:2:2 video formats.

After reset, the device generates 4 VGA 60fps video patterns continuously and stores them into dual-clock FIFOs. The dual clock FIFOs are each 16KB deep. When a FT602 video channel is able to accept data, the corresponding video data is read from the dual clock FIFOs and sent to the FT602. Both FT245 and FT600 FIFO interface modes are supported.

A video frame starts with twelve bytes of header 0x0000_820C, 0xBABE_FACE, 0xBABE_FACE and ends with one terminating byte, 0x55. A frame may be terminated anytime by writing the terminal byte to end frame transmission. The terminal byte signals to FT602 that the frame has ended prematurely or otherwise. FT602 does not transmit the terminal byte to the USB host.

When the dual-clock FIFO overruns, the following conditions are evaluated:

a. If overrun occurred after the frame header is written but before the terminal byte is written, then the FIFO drops all data and continues to discard data until the terminal byte is written into FT602. After this, the FIFO waits for the next start of frame and begins to buffer data and write into the FT602. The discard process is repeated if the FIFO overruns again.

b. If overrun occurred before any frame header is written or after a terminal byte is written but no frame header is written, the FIFO continues to discard data and searches for the next start of frame. This is repeated until FT602 is capable of accepting data.

2.4 I^2C Register Description

1. The I^2C registers have different widths and must be written or read in full.
2. In the following, some registers use a unit of pixel clock. The pixel clock depends on the frame resolution and the selected frame rates. **Table 3 – Pixel Clock** provides the frame resolutions and pixel clock frequency
3. 16 bytes of software defined registers are provided (e.g. scratch) per channel for storing UVC control and command information for storage and retrieval. Customer designs may act on the values written into these locations or provide a response to the USB host via these locations. The IRQ signal may be used to signal the host of change in conditions in the FPGA.

➢ **Convention**

RO: Read Only

RW: Read, Write

Device Address: 0x0D (seven bits address)

Address	Name	Size (Byte)	Type	Description	Default
0x00	Configuration	1	RW	Bit[7:3] : Reserved Bit[2:1]: USB Speed 00: Unknown 01: SuperSpeed 10: High-Speed	0x03

Address	Name	Size (Byte)	Type	Description	Default
				11: Full-Speed Bit[0]: FIFO Interface Select 0: FT245, 1 : FT600	
0x01	FT602 Power Status	1	RW	Bit[7:2]: Reserved Bit[1:0]: FT602 Power Status 00: Active 01: Suspend 1x: Power off	0x00
0x10	Ch0_Control	2	RW	Bit[15:8]:Frame Rate 00-01: 1 Frame per second 02-0xFF: 2-255 frames per second Bit[7]: Pattern Select 0: Moving Pattern 1: Fixed Pattern Bit[6:5]: Four kind of patterns 2'b11: 3 vertical bars 2'b10: 5 vertical bars 2'b01: 7 vertical bars 2'b00: 8 vertical bars Bit[4:0]: Reserved	0x3C00
0x11	Ch0_LSG_LEG	2	RW	Bit[15:8]: Line Start Gap (units of pixel clock) Bit[7:0]: Line End Gap (units of pixel clock)	0x0804
0x12	Ch0_DSG_DEG	2	RW	Bit[15:8]: Data Start Gap (units of pixel clock) Bit[7:0]: Data End Gap (units of pixel clock)	0x0804
0x13	Ch0_H_Blank	2	RW	Number of clock cycle of H Blank (units of pixel clock)	0x0010
0x14	Ch1_Control	2	RW	Bit[15:8]:Frame Rate 00-01: 1 frame per second 02-0xFF: 2-255 frames per second Bit[7]: Pattern Select 0: Moving Pattern 1: Fixed Pattern Bit[6:5]: Four kind of patterns 2'b11: 3 vertical bars	0x3C20

Address	Name	Size (Byte)	Type	Description	Default
				2'b10: 5 vertical bars 2'b01: 7 vertical bars 2'b00: 8 vertical bars Bit[4:0]: Reserved	
0x15	Ch1_LSG_LEG	2	RW	Bit[15:8]: Line Start Gap (units of pixel clock) Bit[7:0]: Line End Gap (units of pixel clock)	0x0804
0x16	Ch1_DSG_DEG	2	RW	Bit[15:8]: Data Start Gap (units of pixel clock) Bit[7:0]: Data End Gap (units of pixel clock)	0x0804
0x17	Ch1_H_Blank	2	RW	Number of clock cycle of H Blank (units of pixel clock)	0x0010
0x18	Ch2_Control	2	RW	Bit[15:8]:Frame Rate 00-01: 1 frame per second 02-0xFF: 2-255 frames per second Bit[7]: Pattern Select 0: Moving Pattern 1: Fixed Pattern Bit[6:5]: Four kind of patterns 2'b11: 3 vertical bars 2'b10: 5 vertical bars 2'b01: 7 vertical bars 2'b00: 8 vertical bars Bit[4:0]: Reserved	0x3C40
0x19	Ch2_LSG_LEG	2	RW	Bit[15:8]: Line Start Gap (units of pixel clock) Bit[7:0]: Line End Gap (units of pixel clock)	0x0804
0x1A	Ch2_DSG_DEG	2	RW	Bit[15:8]: Data Start Gap (units of pixel clock) Bit[7:0]: Data End Gap (units of pixel clock)	0x0804
0x1B	Ch2_H_Blank	2	RW	Number of clock cycle of H Blank (units of pixel clock)	0x0010
0x1C	Ch3_Control	2	RW	Bit[15:8]:Frame Rate 00-01: 1 frame per second 02-0xFF: 2-255 frames per second Bit[7]: Pattern Select	0x3C50

Address	Name	Size (Byte)	Type	Description	Default
				0: Moving Pattern 1: Fixed Pattern Bit[6:5]: Four kind of patterns 2'b11: 3 vertical bars 2'b10: 5 vertical bars 2'b01: 7 vertical bars 2'b00: 8 vertical bars Bit[4:0]: Reserved	
0x1D	Ch3_LSG_LEG	2	RW	Bit[15:8]: Line Start Gap (units of pixel clock) Bit[7:0]: Line End Gap (units of pixel clock)	0x0804
0x1E	Ch3_DSG_DEG	2	RW	Bit[15:8]: Data Start Gap (units of pixel clock) Bit[7:0]: Data End Gap (units of pixel clock)	0x0804
0x1F	Ch3_H_Blank	2	RW	Number of clock cycle of H Blank (units of pixel clock)	0x0010
0x20	Ch0_Low_Mark	2	RW	Water Mark of channel 0	0x0000
0x21	Ch0_High_Mark	2	RW	Buffer size of channel 0	0x0FFF
0x22	Ch1_Low_Mark	2	RW	Water Mark of channel 1	0x0000
0x23	Ch1_High_Mark	2	RW	Buffer size of channel 1	0x0FFF
0x24	Ch2_Low_Mark	2	RW	Water Mark of channel 2	0x0000
0x25	Ch2_High_Mark	2	RW	Buffer size of channel 2	0x0FFF
0x26	Ch3_Low_Mark	2	RW	Water Mark of channel 3	0x0000
0x27	Ch3_High_Mark	2	RW	Buffer size of channel 3	0x0FFF
0x28	Ch0_Frame_Drop	4	RW	Number of discarded frames of channel 0	0x0000_0000
0x29	Ch1_Frame_Drop	4	RW	Number of discarded frames of channel 1	0x0000_0000
0x2A	Ch2_Frame_Drop	4	RW	Number of discarded frames of channel 2	0x0000_0000
0x2B	Ch3_Frame_Drop	4	RW	Number of discarded frames of channel 3	0x0000_0000
0x40-0x5F	UVC Control Channel 0	16	RW	Software Define	X

Address	Name	Size (Byte)	Type	Description	Default
0x60	Ch0_Start_Stream	9	RW	Big Endian Byte 0-1: Video Frame Width Byte 2-3: Video Frame Height Byte 4-7: Clock Frequency (specified in Hz) Byte 8: Resolution index (defined in USB descriptor). 0 : VGA 1 : HD 2 : FHD Others : unused	Byte 0-1: 0x0280 (640) Byte 2-3: 0x01E0 (480) Bytes 4-7: 0x019BFCC0 (27MHz) Byte sequence (0-8): {0x80, 0x02, 0xE0, 0x01, 0x01, 0x9B, 0xFC, 0xC0, 0x00}
0x70-0x8F	UVC Control Channel 1	16	RW	Software Define	X
0x90	Ch1_Start_Stream	9	RW	Big Endian Byte 0-1: Video Frame Width Byte 2-3: Video Frame Height Byte 4-7: Clock Frequency (specified in Hz) Byte 8: Resolution index (defined in USB descriptor). 0 : VGA 1 : HD 2 : FHD Others : unused	Byte 0-1: 0x0280 (640) Byte 2-3: 0x01E0 (480) Bytes 4-7: 0x019BFCC0 (27MHz) Byte sequence (0-8): {0x80, 0x02, 0xE0, 0x01, 0x01, 0x9B, 0xFC, 0xC0, 0x00}
0xA0-0xBF	UVC Control Channel 2	16	RW	Software Define	X
0xC0	Ch2_Start_Stream	9	RW	Big Endian Byte 0-1: Video Frame Width Byte 2-3: Video Frame Height Byte 4-7: Clock Frequency (specified in Hz) Byte 8: Resolution index (defined in USB descriptor). 0 : VGA 1 : HD 2 : FHD Others : unused	Byte 0-1: 0x0280 (640) Byte 2-3: 0x01E0 (480) Bytes 4-7: 0x019BFCC0 (27MHz) Byte sequence (0-8): {0x80, 0x02, 0xE0, 0x01, 0x01, 0x9B, 0xFC, 0xC0, 0x00}
0xD0-0xEF	UVC Control Channel 3	16	RW	Software Define	X

Address	Name	Size (Byte)	Type	Description	Default
0xF0	Ch3_Start_Stream	9	RW	Big Endian Byte 0-1: Video Frame Width Byte 2-3: Video Frame Height Byte 4-7: Clock Frequency (specified in Hz) Byte 8: Resolution index (defined in USB descriptor). 0 : VGA 1 : HD 2 : FHD Others : unused	Byte 0-1: 0x0280 (640) Byte 2-3: 0x01E0 (480) Bytes 4-7: 0x019BFCC0 (27MHz) Byte sequence (0-8): {0x80, 0x02, 0xE0, 0x01, 0x01, 0x9B, 0xFC, 0xC0, 0x00}

Table 2 – Register Description

2.5 Module Description

2.5.1 Module structure

- *ft602_uvc_top.v*
  - *sys_pll.v*
  - *ft602_i2c_slv.v*
  - *ft602_uvc_reg.v*
  - *ft602_uvc_io.v*
  - *ft602_uvc_fsm.v*
  - *ft602_pre_fet.v*
  - *ft602_pch_inp.v:ch0*
    - *ft602_pat_gen.v*
    - *ft602_hdmi_rx.v*
    - *ft602_dclk_fifo.v*
    - *dpsram_4kx36.v*
  - *ft602_pch_inp.v:ch1*
    - *ft602_pat_gen.v*
    - *ft602_hdmi_rx.v*
    - *ft602_dclk_fifo.v*
    - *dpsram_4kx36.v*
  - *ft602_pch_inp.v:ch2*
    - *ft602_pat_gen.v*
    - *ft602_hdmi_rx.v*
    - *ft602_dclk_fifo.v*

- *dpsram_4kx36.v*

- *ft602_pch_inp.v:ch3*
  - *ft602_pat_gen.v*
  - *ft602_hdmi_rx.v*
  - *ft602_dclk_fifo.v*
  - *dpsram_4kx36.v*

2.5.2 Module ft602_uvc_top.v

The top module of the FT602 UVC FPGA application, it contains all sub modules as well as memory, PLL macros used in design. Its interface is identical to the Pin Out (Section 2.2).

2.5.3 Module sys_pll.v

The PLL macro that generates clocks for video emulation, its input clock is 50MHz and output clocks are 27MHz (VGA), 74.25MHz (HD) and 148.5MHz (Full HD).

2.5.4 Module ft602_i2c_slv.v

This simple Slave I^2C module receives parameters from the FT602 to configure the operation of the FPGA such as FIFO modes, pattern generator resolutions, buffer size … The I^2C device address is 0x0D.

2.5.5 Module ft602_uvc_io.v

This module connects signals between ports and internal modules. It also controls the direction of bidirectional IOs DATA and BE.

2.5.6 Module ft602_uvc_fsm.v

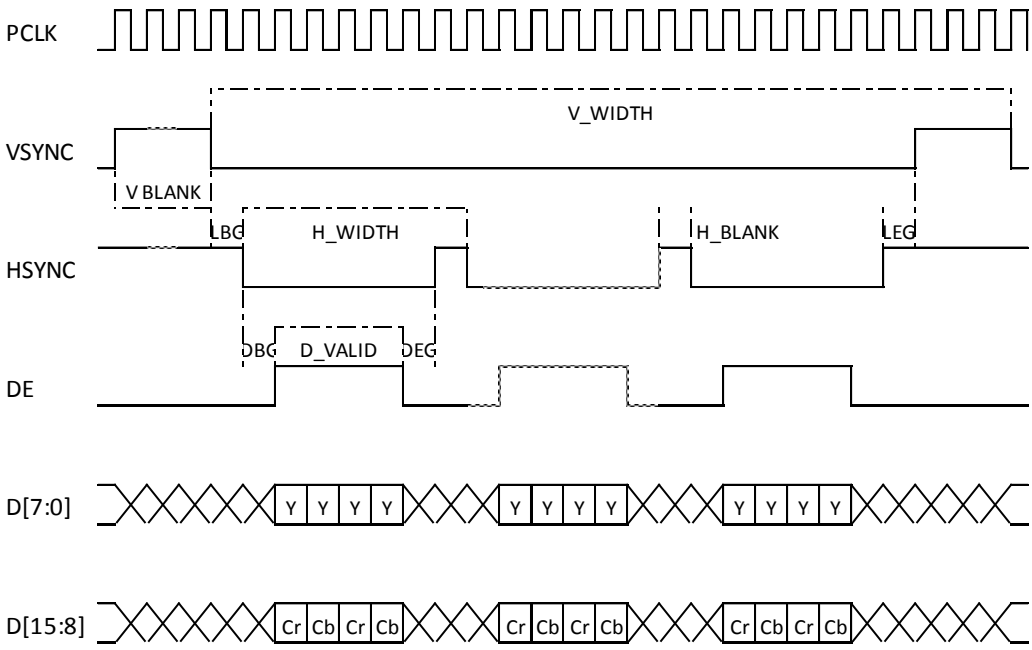
This module controls all operations of the FIFO master. It controls the state machine and round robin of the FT602's 4 channels.

2.5.7 Module ft602_pre_fet.v

This module temporarily stores pre-fetch data that will be sent to IOs in master write mode. It gets data from internal memory to store into registers to optimize the timing of the FPGA.

2.5.8 Module ft602_patt_gen.v

This module generates patterns that emulate the video source with the output as below.



The clock frequency, resolution as well as the blanks and gaps are configurable. Refer to the I2C Register Description for more details.

Note:

(DBG + D_VALID + DEG + H_BLANK) must be smaller than (Pixel Clock / Frame Rate / Number of Lines)

2.5.9 Module ft602_hdmi_rx.v

This module selects the video source between the internal pattern generator and a real video source. For this application, only the internally generated patterns are supported, the real video inputs are tied to 0s. This module also couples two 16-bit pixels to the 32-bit data bus as well as inserting the frame header and the frame terminating byte to the received video frame before storing them into the internal buffer.

2.5.10 Module ft602_dclk_fifo.v

This FIFO converts data from the pixel clock domain to the FT602 clock domain. It also acts as the internal buffer of the design. The maximum capacity is 4kx32 and can be configured to a smaller buffer through the High Mark register. This feature allows user tests with small memories. It also supports a Low Mark register that allows users to slow down the read operation by setting this register then reading data from the FIFO after the volume of data in the FIFO reaches this level.

2.5.11 Module dpsram_4kx36.v

This is the Dual Port SRAM macro. Its capacity is 4096 words depth and 36 bits width, 32 bits for storing data and 4 bits for storing byte enable.

2.6 Operating Mode

Once configured to USB Full Speed or High Speed modes, only QVGA 60fps is generated. When Super Speed is configured, any resolution can be generated but the pixel clock is limited within three frequencies 27MHz, 74.25MHz and 148.5MHz.

Index	USB MODE	Resolution	Pixel Clock
1	High Speed / Full Speed	QVGA	27 MHz
2	Super Speed	VGA	27 MHz
3	Super Speed	HD	74.25 MHz
4	Super Speed	Full HD	148.5 MHz

Table 3 – Pixel Clock

3 Altera FPGA Implementation

The following section describes the FPGA implementation on the Altera Cyclone V GX Starter Kit. The starter kit provides an HSMC connector for the attachment of a UMFT602 development board. KEY0 is the hard reset of design and 4 red LEDs indicate there are frames discarded by FPGA. The video stream for each channel can be disabled or enabled by the dip switches marked as SW3-0.

3.1 System Schematic

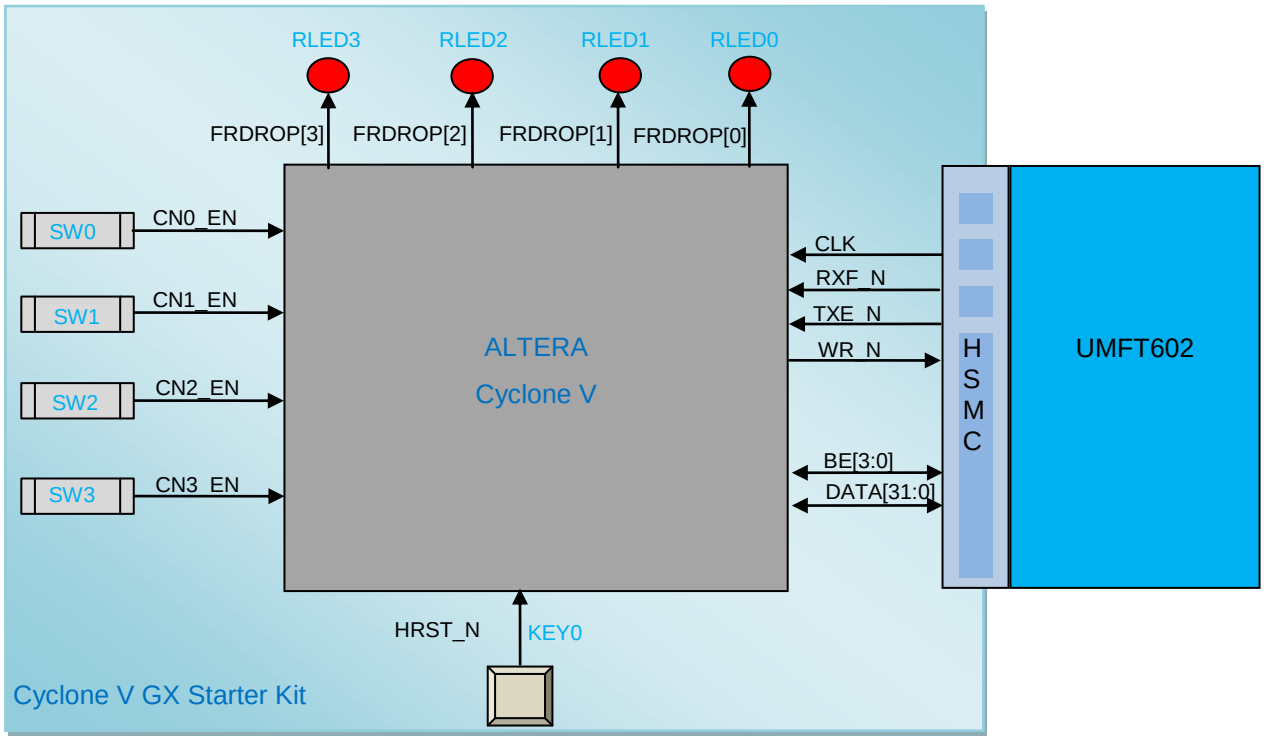


Figure 2 – Altera System Schematic

3.2 Hardware

The image below shows the Altera Cyclone V Starter Kit configuration. The RLEDs connected to FRDROP[3:0] as shown at the bottom. KEY0 is used as HRST_N, SW3-0 are streaming enable, disable switches.

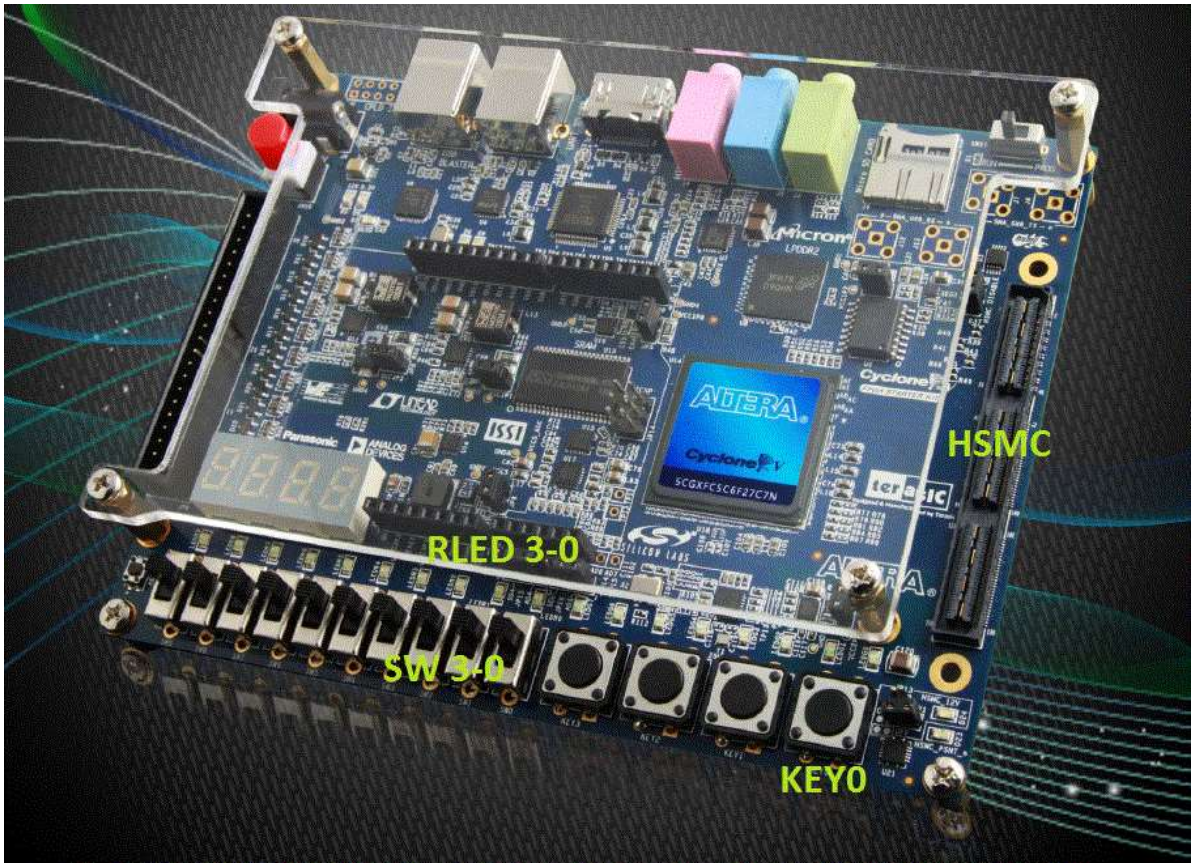


Figure 3 - Altera Cyclone V Development Kit

3.3 FPGA Pin Map

Pin Name	Description	Direction	I/O Standard	Cyclone V GX Pin Number for FT601
CLK	HSMC Connector	Input	2.5V	PIN_N9
RXF_N	HSMC Connector	Input	2.5V	PIN_F18
TXE_N	HSMC Connector	Input	2.5V	PIN_E18
WR_N	HSMC Connector	Output	2.5V	PIN_E15
RESERVE1	HSMC Connector	Output	2.5V	PIN_E13
RESERVE2	HSMC Connector	Output	2.5V	PIN_D13
RESERVE3	HSMC Connector	Output	2.5V	PIN_F16
BE[3]	HSMC Connector	Inout	2.5V	PIN_A9

Pin Name	Description	Direction	I/O Standard	Cyclone V GX Pin Number for FT601
BE[2]	HSMC Connector	Inout	2.5V	PIN_A8
BE[1]	HSMC Connector	Inout	2.5V	PIN_C12
BE[0]	HSMC Connector	Inout	2.5V	PIN_C13
DATA[31]	HSMC Connector	Inout	2.5V	PIN_G17
DATA[30]	HSMC Connector	Inout	2.5V	PIN_G16
DATA[29]	HSMC Connector	Inout	2.5V	PIN_J11
DATA[28]	HSMC Connector	Inout	2.5V	PIN_J12
DATA[27]	HSMC Connector	Inout	2.5V	PIN_J16
DATA[26]	HSMC Connector	Inout	2.5V	PIN_H15
DATA[25]	HSMC Connector	Inout	2.5V	PIN_K11
DATA[24]	HSMC Connector	Inout	2.5V	PIN_L12
DATA[23]	HSMC Connector	Inout	2.5V	PIN_H17
DATA[22]	HSMC Connector	Inout	2.5V	PIN_H18
DATA[21]	HSMC Connector	Inout	2.5V	PIN_L11
DATA[20]	HSMC Connector	Inout	2.5V	PIN_M11
DATA[19]	HSMC Connector	Inout	2.5V	PIN_M12
DATA[18]	HSMC Connector	Inout	2.5V	PIN_N12
DATA[17]	HSMC Connector	Inout	2.5V	PIN_H13
DATA[16]	HSMC Connector	Inout	2.5V	PIN_H14
DATA[15]	HSMC Connector	Inout	2.5V	PIN_C15
DATA[14]	HSMC Connector	Inout	2.5V	PIN_B15
DATA[13]	HSMC Connector	Inout	2.5V	PIN_B19
DATA[12]	HSMC Connector	Inout	2.5V	PIN_C20
DATA[11]	HSMC Connector	Inout	2.5V	PIN_A11
DATA[10]	HSMC Connector	Inout	2.5V	PIN_B10
DATA[9]	HSMC Connector	Inout	2.5V	PIN_B11
DATA[8]	HSMC Connector	Inout	2.5V	PIN_A12
DATA[7]	HSMC Connector	Inout	2.5V	PIN_C10

Pin Name	Description	Direction	I/O Standard	Cyclone V GX Pin Number for FT601
DATA[6]	HSMC Connector	Inout	2.5V	PIN_D10
DATA[5]	HSMC Connector	Inout	2.5V	PIN_B9
DATA[4]	HSMC Connector	Inout	2.5V	PIN_C9
DATA[3]	HSMC Connector	Inout	2.5V	PIN_E11
DATA[2]	HSMC Connector	Inout	2.5V	PIN_E10
DATA[1]	HSMC Connector	Inout	2.5V	PIN_D12
DATA[0]	HSMC Connector	Inout	2.5V	PIN_D11
SRST_N	HSMC Connector	Inout	2.5V	PIN_C23
I2C_SCL	HSMC Connector	Input	2.5V	PIN_A13
I2C_SDA	HSMC Connector	Input	2.5V	PIN_B12
INT_REQ	HSMC Connector	Output	2.5V	PIN_C22
HRST_N	KEY0	Input	2.5V	PIN_P11
DIPSW[0]	SW0	Input	2.5V	PIC_AC9
DIPSW[1]	SW1	Input	2.5V	PIC_AE10
DIPSW[2]	SW2	Input	2.5V	PIC_AD13
DIPSW[3]	SW3	Input	2.5V	PIC_AC8
CLK50M	Clock Input	Input	2.5V	PIN_R20

Table 4 – 5CGXFC5C6F27C6 Device Pin Map

3.4 FPGA Constraints

```
create_clock -period 20.000ns [get_ports CLK50M]
create_clock -period 10.000ns [get_ports CLK]
derive_pll_clocks
derive_clock_uncertainty
set_input_delay -clock [get_clocks CLK] -max 7  [get_ports {RXF_N TXE_N}]
set_input_delay -clock [get_clocks CLK] -max 7  [get_ports {BE[*] DATA[*]}]
set_input_delay -clock [get_clocks CLK] -min 6.5  [get_ports {RXF_N TXE_N}]
set_input_delay -clock [get_clocks CLK] -min 6.5  [get_ports { DATA[*]}]
set_output_delay -clock [get_clocks CLK] -max 1.0 [get_ports {WR_N }]
set_output_delay -clock [get_clocks CLK] -max 1.0 [get_ports {DATA[*]}]
set_output_delay -clock [get_clocks CLK] -min 4.8 [get_ports {WR_N}]
```

```
set_output_delay -clock [get_clocks CLK] -min 4.8 [get_ports {BE[*] DATA[*]}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[2].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[3].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[4].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[2].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[3].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[4].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks {CLK}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks {CLK}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[2].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks {CLK}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[3].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks {CLK}] -to [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[4].gpll~PLL_OUTPUT_COUNTER|divclk}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[0].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{CLK}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[2].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{CLK}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[3].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{CLK}]

set_false_path -from [get_clocks
{i0_sys_pll|sys_pll_inst|altera_pll_i|general[4].gpll~PLL_OUTPUT_COUNTER|divclk}] -to [get_clocks
{CLK}]

set_false_path -from [get_ports {SRST_N HRST_N DIPSW[*] PBUTT[*]}] -to [get_registers *]

set_false_path -from [get_ports {TXE_N}] -to [get_registers *]

set_false_path -from {ft602_uvc_fsm:i3_ft602_uvc_fsm|be_oe_n} -to {DATA[*]};

set_false_path -from {ft602_uvc_fsm:i3_ft602_uvc_fsm|be_oe_n} -to {BE[*]};

set_false_path -from {ft602_uvc_fsm:i3_ft602_uvc_fsm|dt_oe_n} -to {DATA[*]}

set_false_path -to [get_ports {FRDROP[*] LEDR[*] IRQ}]
```

4 Xilinx FPGA Implementation

The following section describes the FPGA implementation on the Spartan-6 SP601 Kit. The starter kit provides FMC connector for the attachment of an UMFT602 board. Push button 0 is the hard reset of design and 4 LEDs indicate there are frames discarded by FPGA. The video stream of each channel can be disabled or enabled by dip switch SW8.

4.1 System Schematic

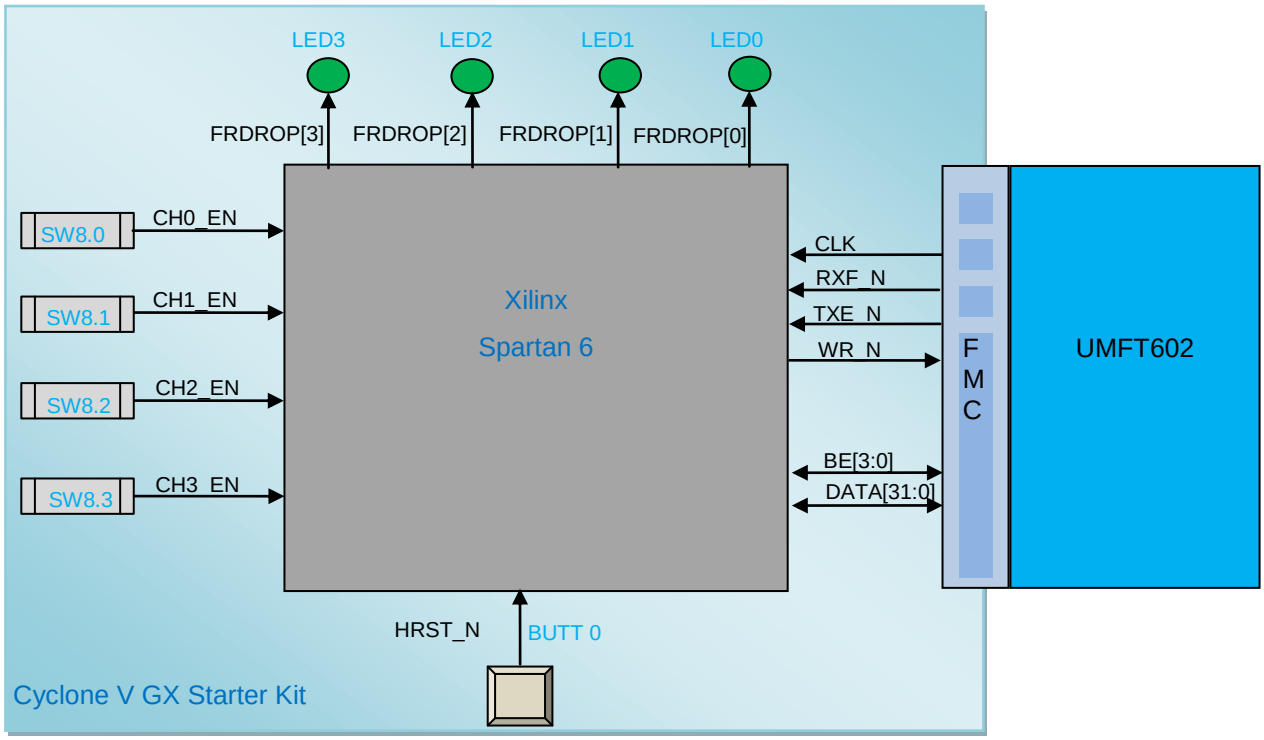


Figure 4 - Xilinx System Schematic

4.2 Hardware

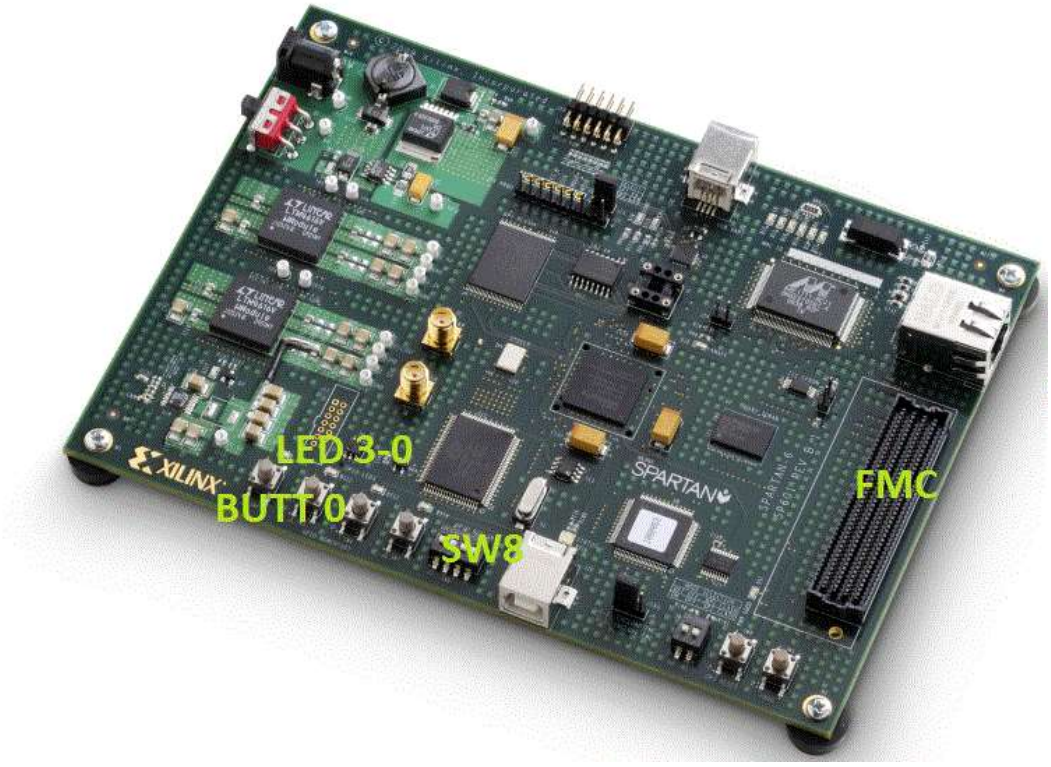


Figure 5 - Xilinx Spartan-6 SP601 Kit

4.3 FPGA Pin Map

Pin Name	Description	Direction	I/O Standard	Spartan-6 Pin Number for FT601
CLK	FMC Connector	Input	2.5V	PIN_R10
RXF_N	FMC Connector	Input	2.5V	PIN_E7
TXE_N	FMC Connector	Input	2.5V	PIN_E8
I2C_SDA	FMC Connector	Input	2.5V	PIN_A2
I2C_SCL	FMC Connector	Input	2.5V	PIN_B2
WR_N	FMC Connector	Output	2.5V	PIN_F11
RD_N	FMC Connector	Output	2.5V	PIN_C9
OE_N	FMC Connector	Output	2.5V	PIN_D9
SIWU_N	FMC Connector	Output	2.5V	PIN_E11

Pin Name	Description	Direction	I/O Standard	Spartan-6 Pin Number for FT601
BE[3]	FMC Connector	Inout	2.5V	PIN_G11
BE[2]	FMC Connector	Inout	2.5V	PIN_F10
BE[1]	FMC Connector	Inout	2.5V	PIN_G9
BE[0]	FMC Connector	Inout	2.5V	PIN_F9
DATA[31]	FMC Connector	Inout	2.5V	PIN_R8
DATA[30]	FMC Connector	Inout	2.5V	PIN_T8
DATA[29]	FMC Connector	Inout	2.5V	PIN_N7
DATA[28]	FMC Connector	Inout	2.5V	PIN_P8
DATA[27]	FMC Connector	Inout	2.5V	PIN_N6
DATA[26]	FMC Connector	Inout	2.5V	PIN_P7
DATA[25]	FMC Connector	Inout	2.5V	PIN_N5
DATA[24]	FMC Connector	Inout	2.5V	PIN_P6
DATA[23]	FMC Connector	Inout	2.5V	PIN_R7
DATA[22]	FMC Connector	Inout	2.5V	PIN_T4
DATA[21]	FMC Connector	Inout	2.5V	PIN_T7
DATA[20]	FMC Connector	Inout	2.5V	PIN_V4
DATA[19]	FMC Connector	Inout	2.5V	PIN_U7
DATA[18]	FMC Connector	Inout	2.5V	PIN_R11
DATA[17]	FMC Connector	Inout	2.5V	PIN_V7
DATA[16]	FMC Connector	Inout	2.5V	PIN_T11
DATA[15]	FMC Connector	Inout	2.5V	PIN_M11
DATA[14]	FMC Connector	Inout	2.5V	PIN_U8
DATA[13]	FMC Connector	Inout	2.5V	PIN_N11
DATA[12]	FMC Connector	Inout	2.5V	PIN_V8
DATA[11]	FMC Connector	Inout	2.5V	PIN_M8
DATA[10]	FMC Connector	Inout	2.5V	PIN_U11
DATA[9]	FMC Connector	Inout	2.5V	PIN_N8
DATA[8]	FMC Connector	Inout	2.5V	PIN_V11

Pin Name	Description	Direction	I/O Standard	Spartan-6 Pin Number for FT601
DATA[7]	FMC Connector	Inout	2.5V	PIN_T6
DATA[6]	FMC Connector	Inout	2.5V	PIN_T12
DATA[5]	FMC Connector	Inout	2.5V	PIN_V6
DATA[4]	FMC Connector	Inout	2.5V	PIN_V12
DATA[3]	FMC Connector	Inout	2.5V	PIN_M10
DATA[2]	FMC Connector	Inout	2.5V	PIN_U15
DATA[1]	FMC Connector	Inout	2.5V	PIN_N9
DATA[0]	FMC Connector	Inout	2.5V	PIN_V15
SRST_N	FMC Connector	Inout	2.5V	PIN_C8
HRST_N	KEY0	Input	2.5V	PIN_P4
CN0_EN	SW0	Input	2.5V	PIN_D14
CN1_EN	SW1	Input	2.5V	PIN_E12
CN2_EN	SW2	Input	2.5V	PIN_F12
CN3_EN	SW3	Input	2.5V	PIN_V13
FRDROP[0]	LED0	Output	2.5V	PIN_E13
FRDROP[1]	LED1	Output	2.5V	PIN_C14
FRDROP[2]	LED2	Output	2.5V	PIN_C4
FRDROP[3]	LED3	Output	2.5V	PIN_A4

Table 5 – XC6SLX16-2CSG324 Device Pin Map

4.4 FPGA Constraints

```
NET "CLK" TNM_NET = "CLK";
TIMESPEC "TS_CLK" = PERIOD "CLK" 10 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
PIN "i0_sys_pll/clkout1_buf.O" TNM_NET = "CLK50";
TIMESPEC "TS_CLK1" = PERIOD "CLK50" 20 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
PIN "i0_sys_pll/clkout3_buf.O" TNM_NET = "CLK150";
TIMESPEC "TS_CLK3" = PERIOD "CLK150" 6.73 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
PIN "i0_sys_pll/clkout4_buf.O" TNM_NET = "CLK75";
TIMESPEC "TS_CLK4" = PERIOD "CLK75" 13.46 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
PIN "i0_sys_pll/clkout5_buf.O" TNM_NET = "CLK27";
TIMESPEC "TS_CLK5" = PERIOD "CLK27" 37.04 ns HIGH 50.00% INPUT_JITTER 800 ps PRIORITY 1;
```

```
PIN "i0_sys_pll/clkout3_buf.O" CLOCK_DEDICATED_ROUTE = FALSE;
PIN "i0_sys_pll/clkout4_buf.O" CLOCK_DEDICATED_ROUTE = FALSE;
PIN "i0_sys_pll/clkout5_buf.O" CLOCK_DEDICATED_ROUTE = FALSE;
NET "DATA<*>"       TNM = "M_FIFO_IO";
NET "BE<*>"         TNM = "M_FIFO_IO";
NET "RXF_N"         TNM = "M_FIFO_I";
NET "TXE_N"         TNM = "M_FIFO_I";
NET "TXE_N"         TNM = "M_FIFO_I1";
NET "WR_N"          TNM = "M_FIFO_O";
NET "RD_N"          TNM = "M_FIFO_O";
NET "OE_N"          TNM = "M_FIFO_O";
NET "FRDROP<*>"      TNM = "LED_O";
INST "i3_ft602_uvc_fsm/odata*"  IOB=TRUE;
INST "i3_ft602_uvc_fsm/wr_n"    IOB=TRUE;
TIMEGRP "M_FIFO_IO" OFFSET = IN 6 ns VALID 6.5 ns BEFORE "CLK" RISING;
TIMEGRP "M_FIFO_I"  OFFSET = IN 6 ns VALID 6.5 ns BEFORE "CLK" RISING;
TIMEGRP "M_FIFO_IO" OFFSET = OUT 9 ns VALID 5.8 ns AFTER "CLK" RISING;
TIMEGRP "M_FIFO_O"  OFFSET = OUT 9 ns VALID 5.8 ns AFTER "CLK" RISING;
NET "i3_ft602_uvc_fsm/be_oe_n*" TPTHRU = "OUT_EN";
NET "i3_ft602_uvc_fsm/dt_oe_n*" TPTHRU = "OUT_EN";
NET "HRST_N" TNM = "IN_TIG";
NET "SRST_N" TNM = "IN_TIG";
TIMESPEC TS_TIG   = FROM "OUT_EN" TO "M_FIFO_IO" TIG;
TIMESPEC TS_TIG   = FROM "IN_TIG" TO FFS TIG;
TIMESPEC TS_TIG   = FROM FFS TO "LED_O" TIG;
TIMESPEC TS_TIG   = FROM "M_FIFO_I1" TO FFS TIG;
```

5 Source Code

The source code to both the Altera and Xilinx projects may be found in the following zip files.

The Altera sample is based on quartus version 16. To use the sample with a newer version of quartus, project needs to be converted. When the project is opened in the new software, a prompt to migrate the project is displayed. Click "Yes" to convert the project.

The Xilinx sample is based on ISE version 14.7. To use with newer versions of ISE, the project needs to be converted first. When the project is opened in the new software, a prompt to migrate the project is displayed. Click "Yes" to convert the project.

5.1 Altera Cyclone V Source Code

	Altera	Remarks
FT602	Cyclone 32	FIFO 32

5.2 Xilinx Spartan-6 Source Code

	Xilinx	Remarks
FT602	Spartan 32	FIFO 32

6 Setup Procedure

Please follow this procedure to get FT602 streaming working on VLC player.

1. Check the R25, R26 and R27 are 0 ohm
2. Check JP3 short 1-2, JP2 short 2-3, JP5 and JP4 remove jumper for UMFT602X module.

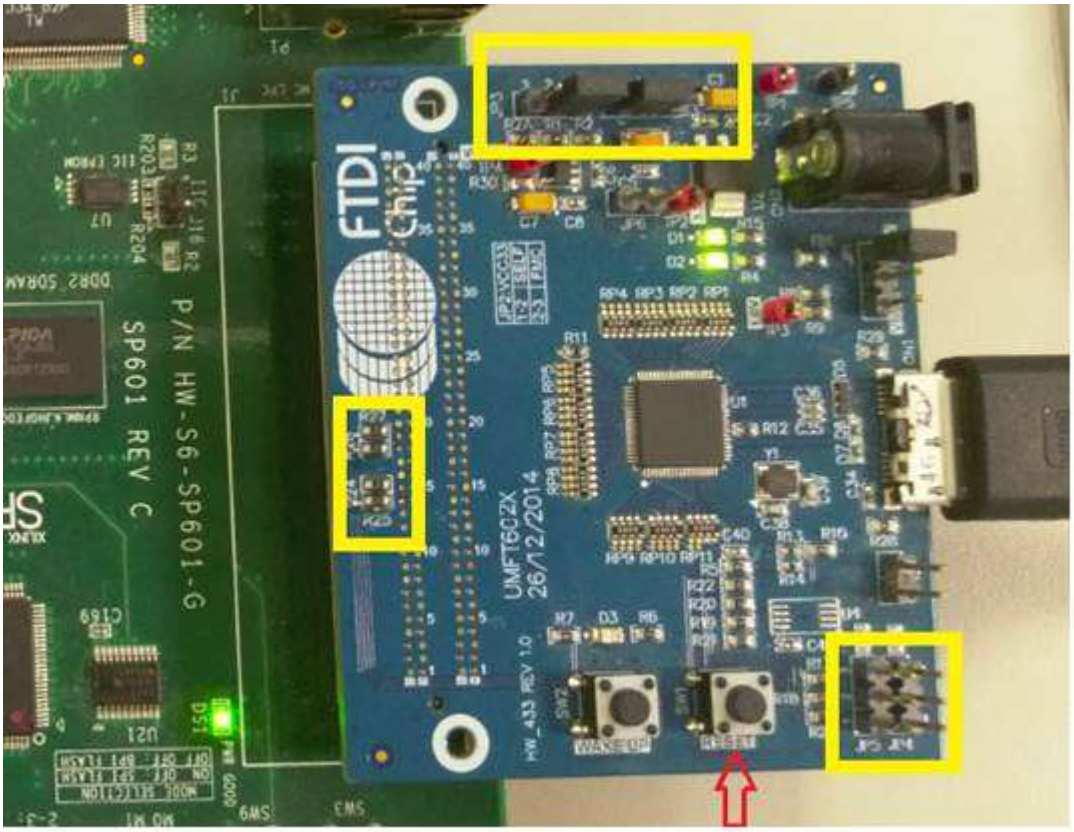


Figure 6 - FT602 Board Setup

3. Plug to USB3.0 host then press "reset" button PC will recognize the "*FTDI Superspeed Video Channel1*" for UVC device.

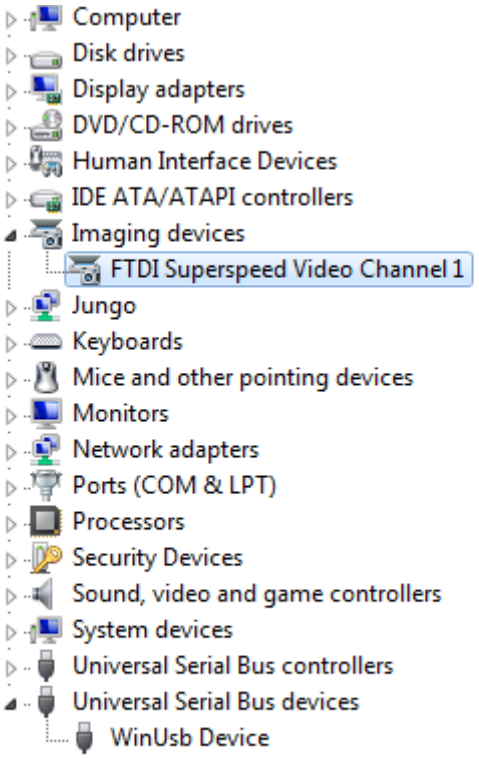


Figure 7 - Device manager shows FT602

4. To update the FPGA image for Xilinx board for UVC streaming, Please refer to AN_376 Xilinx FPGA FIFO Master Programming Guide. Use ft602_uvc_top.bit when prompt for assign new configuration file comes up. And assign ft602_uvc.msc for flashing to PROM.
5. To update the FPGA image for Altera Cyclone board for UVC streaming, please refer to AN_377 Altera FPGA FIFO Master Programming Guide.
6. Press the RESET button of UMFT601X module then plug to USB3.0 HOST.
7. Open VLC player then use the hot key "Ctrl + C" to choose '*FTDI Superspeed Video Channel1'*, then you will see the colour bar on screen.

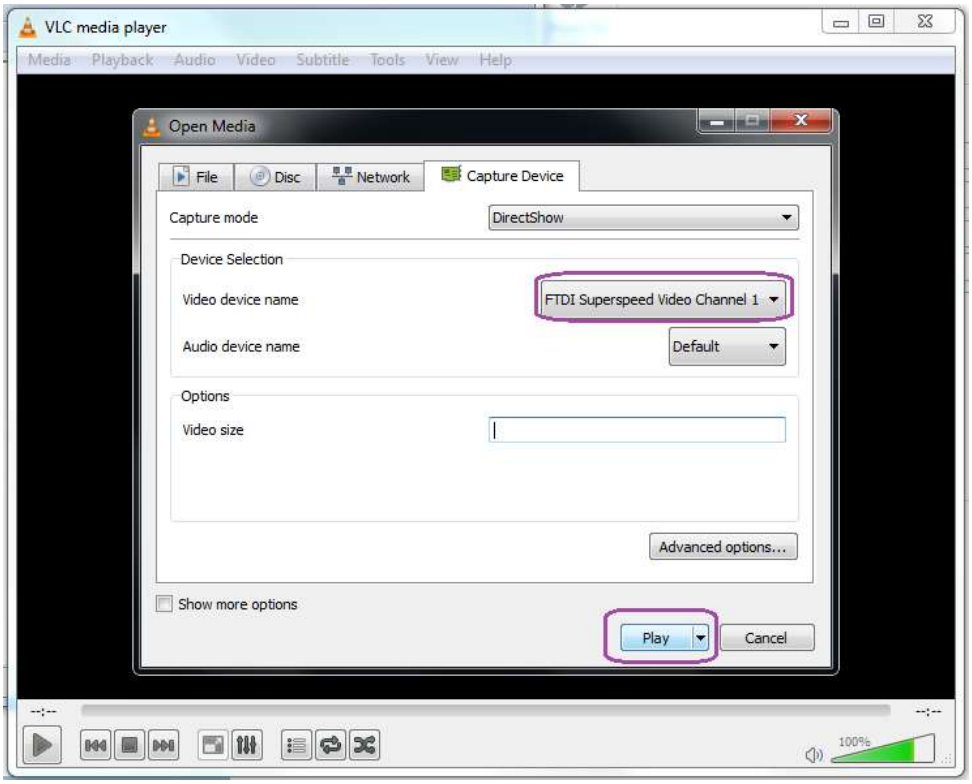


Figure 8 - Device Selection in VLC

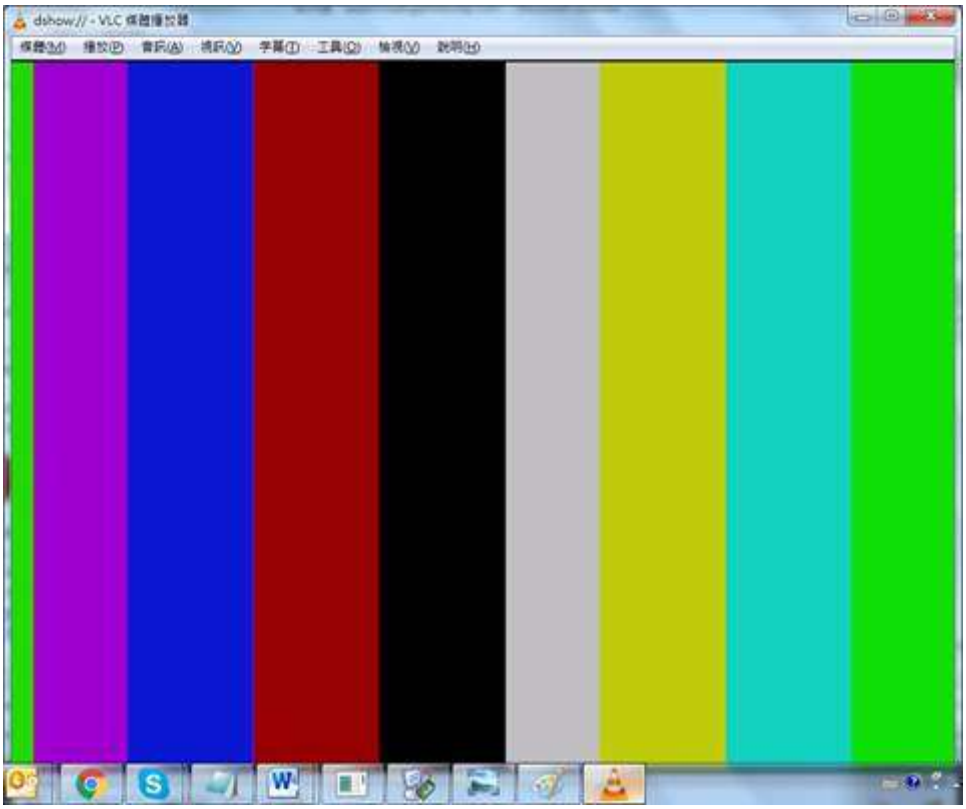


Figure 9 - Colour Bar appears on VLC screen

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A - References

Document References

- FT602 IC Datasheet
- UMFT602x Datasheet
- Altera Cyclone V

Source Code

- Cyclone 32
- Spartan 32

Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

List of Figures

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Appendix C – Revision History

Document Title	:	AN_434 FT602_UVC_Bus_Master_Sample
Document Reference No.	:	FT_001392
Clearance No.	:	FTDI#526
Product Page	:	http://www.ftdichip.com/FTProducts.htm
Document Feedback	:	Send Feedback

Revision	Changes	Date
1.0	Initial Release	2017-04-06
1.1	Updated release (Section 6 – Updated Setup Procedure)	2017-04-18
1.2	Section 3.4 and 4.4 - Updated FPGA constraints Section 5 – Added details about project migration	2017-12-08