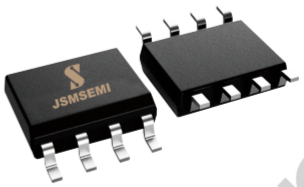
1 Description

IX4426N is power switch driver. It has a matching rise and fall time when charging and discharging the gate of the power switch.

IX4426N has high latch resistance under all conditions in its rated power and voltage range. When noise spikes of up to 5V (either polarity) occur on the ground pin, the IX4426N is not damaged. IX4426N can accept reverse currents up to 500 mA to force back its output without damage or logic confusion. All ports are fully protected by up to 2.0 kV electrostatic discharge (ESD).It can workin the temperature range of -40°C to 125°C .



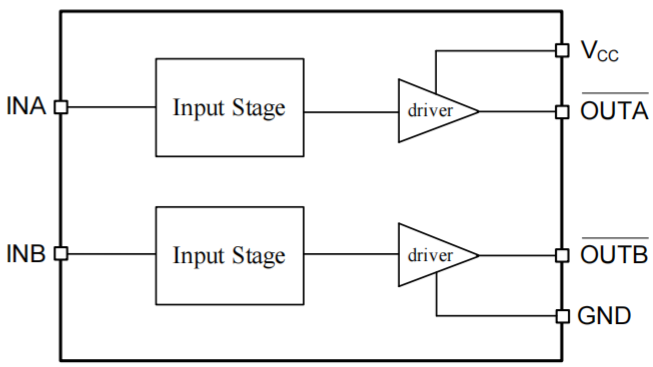
2 Features

- Latch Protection: withstand 0.5 A reverse current
- Ability to Handle Negative Voltages (-10 V) at Inputs
- Low Output Impedance
- Two Independent Gate-Drive Channel
- 2A Peak Output Current
- 4.5 to 25-V Single-Supply Range
- High Ability of driving capacitive load
- Rise/Fall time matching
- Operating Temperature Range of -40 to 125° C
- Turn on/Turn off Delays:
- -- Ton/Toff =25ns/25ns
- The RoSH Standard
- SOIC8 package

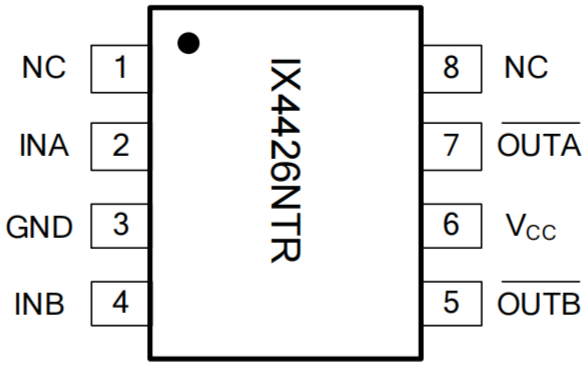
3 Applications

- Switch-Mode Power Supplies
- line drivers
- Pulse transformer driver
- Driving MOSFETs and IGBTs
- Motor drives
- pulse generator
- Switch-Mode Power Supplies
- DC-to-DC Converters
- class D switching amplifier

Pin Configuration



4 Pin Configuration and Functions



8-Pin SOIC8 Package Top View

Pin Functions

PIN	NAME	DESCRIPTION
1	NC	--
2	INA	Input to Channel A
3	GND	Ground: All signals are referenced to this pin.
4	INB	Input to Channel B
5	$\overline{OUTB}$	Output of Channel B
6	VCC	Bias supply input
7	$\overline{OUTA}$	Output of Channel A
8	NC	--

5 Specifications

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

Symbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	—	25	V
V_{IN}	INA, INB voltage	GND-10	V_{CC}+0.3	

5.2 ESD Ratings

Symbol	Definition	MIN	MAX	UNIT
ESD	Human body model (HBM)	—	2000	V
	Charged device model (CDM)	—	500	V

5.3 Power Ratings

Symbol	Definition	MIN	MAX	UNIT
PD	SOIC package power（TA≤70°C）	—	470	mW

5.4 Thermal Information

Symbol	Definition	MIN	MAX	UNIT
T_J	Operating junction temperature	—	+150	°C
T_S	Storage temperature	-45	+150	

5.5 Recommended Operating Conditions

To properly operate, device should be used in the following recommended conditions. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

Symbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	4.5	20	V
T_C	ambient temperature	-40	125	°C

5.6 Electrical Characteristics

TA= 25℃, VCC=15V(unless otherwise noted)

Symbol	Definition	MIN	TYP	MAX	UNIT
V_{IH}	Input signal high threshold	2.4	—	—	V
V_{IL}	Input signal low threshold	—	—	0.8	V
I_{IN}	Input current(0V≤VIN≤VCC)	—	—	200	μA
V_{OH}	High output voltage	VCC–0.025	—	—	V
V_{OL}	Low output voltage	—	—	0.025	V
R_{OH}	Output pullup resistance(VCC=18V,IO=100mA)	—	4.0	8.0	Ω
R_{OL}	Output pulldown resistance(VCC=18V,IO=100mA)	—	2.0	4.0	Ω
I_{PK}	Peak output source current	—	2	—	A
I_{REV}	Reverse current that latch protection can withstand(Working cycle≤2%,t≤300us,VCC=18V)	—	>0.5	—	A
t_R	Rise time(VCC=18V,CLOAD=100pF)	—	—	30	ns
t_F	Fall time(VCC=18V,CLOAD=100pF)	—	—	30	ns
t_{ON}	Turn-on propagation delay(VCC=18V,CLOAD=100pF)	—	—	70	ns
t_{OFF}	Turn-off propagation delay(VCC=18V,CLOAD=100pF)	—	—	70	ns
I_{Q1}	VCC quiescent supply current(V_{INA}=V_{INB}=HIGH)	—	—	1	mA
I_{Q0}	VCC quiescent supply current(V_{INA}=V_{INB}=LOW)	—	—	1	mA

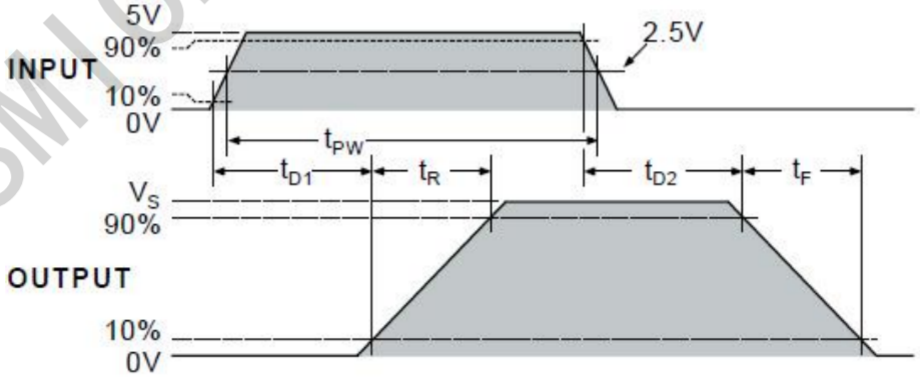
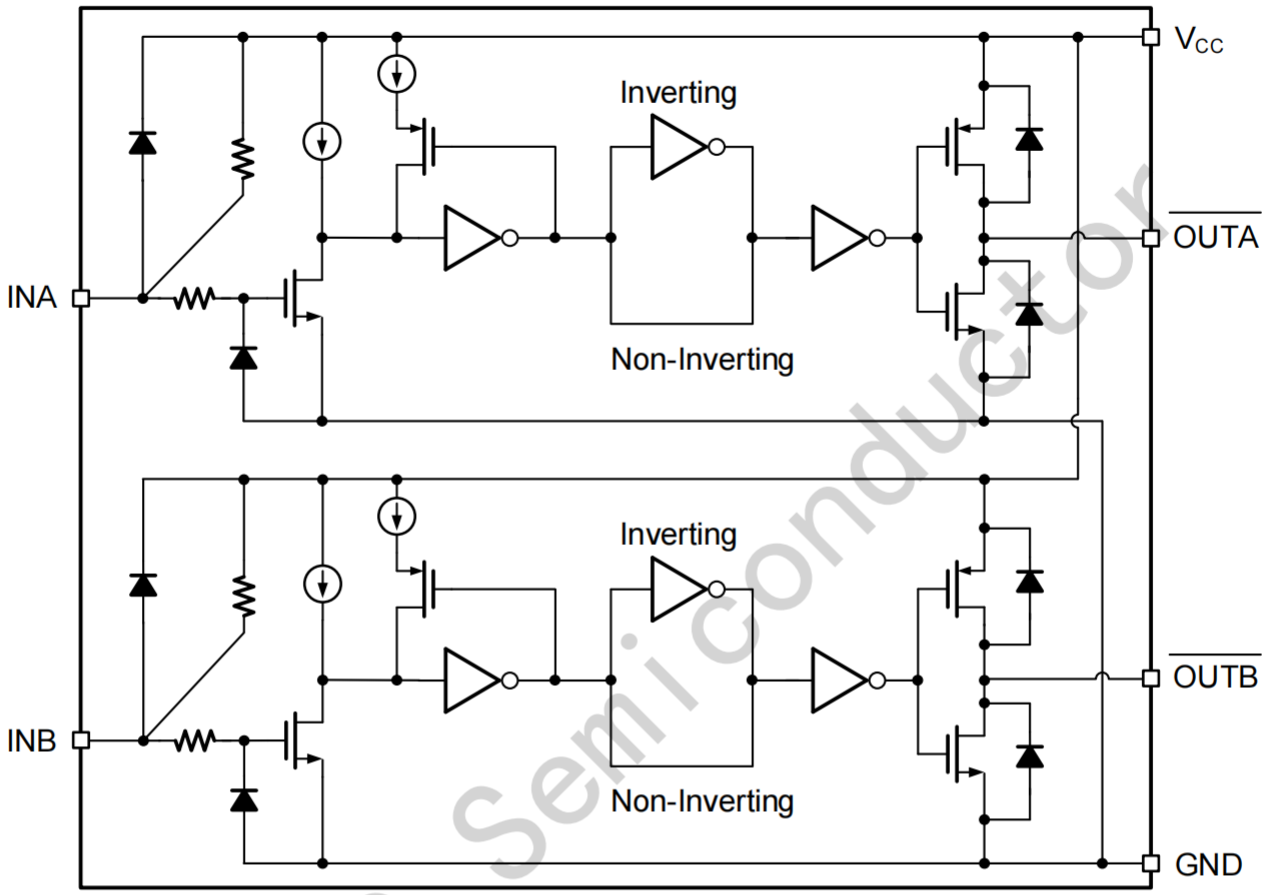


Figure 1 Input-Output waveform(non-inverting)

6 Detailed description

6.1 Functional Block Diagram



6.2 Typical Application

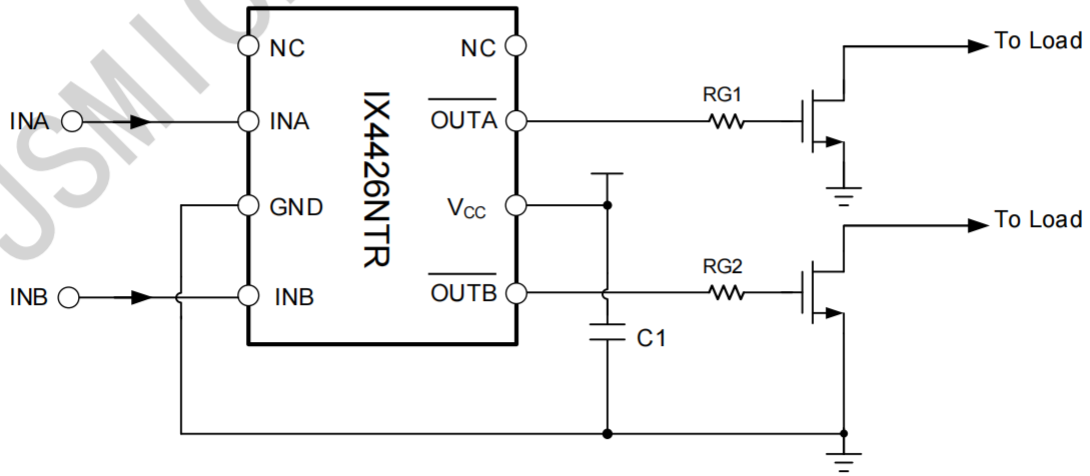


Figure 2 Typical Application Diagram of IX4426N

6.3 Chip working logic

The IX4426N signal input ports (INA, INB) adopt a level trigger mode, which means that the voltage value meets the logical requirements and the chip can operate normally, as shown in Table 7-1.

Input output logic table

INPUT		OUTPUT	
INA	INB	OUTA/	OUTB/
L	L	H	H
H	H	L	L
L	H	H	L
H	L	L	H
Note: H represents high level; L represents low level			

6.4 Signal input port

IX4426N includes two independent signal input ports for receiving control signals from the main control, without mutual interference. These two ports are designed with high reliability, and even if a reverse current of 500mA forcibly returns to their output, it will not cause damage or logical confusion. The signal input port also has the ability to directly process -10V voltage, which can still ensure the safe operation of the chip under the influence of large noise waveforms and increase the stability of the chip. It is not recommended to adjust the input port waveform slope or delay during design to achieve the purpose of adjusting the output waveform. If it is necessary to adjust the rise and fall time of the power end, it is recommended to add additional resistance between the output end and the power end.

The IX4426N signal input port has a pull-up resistance to GND. It is recommended to short circuit this port to GND when not in use.

6.5 Output port

IX4426N has reverse output and input, which can be used to drive P-type or N-type MOSFETs.

Each output port can provide a peak pull-up or pull-down current of 2A, and its high-speed and high current characteristics can be used to drive MOSFETs in high-frequency application design.

7 Application Information

The high-speed and high current characteristics of IX4426N can be used in application scenarios such as high-frequency power supplies. Its typical application is that the PWM output stage power of the main control IC is often insufficient to drive the MOSFET at the power end, so a high-power driver stage chip is needed between the main control IC and the MOSFET to drive the gate voltage of the MOSFET, in order to ensure that the MOSFET operates in a stable state.

7.1 Application suggestions

In high-frequency and high-power application environments, ensuring the stable operation of chips is particularly important. Therefore, the following suggestions are proposed when applying IX4426N:

1) During the switching process, IX4426N will output a peak switching current of 2A, and as the frequency increases, the stability requirements for VCC become more stringent. Therefore, in design, a larger capacitance electrolytic capacitor can be selected to stabilize the VCC voltage, and to cope with high -frequency characteristics, a low ESR/ESL capacitor (ceramic capacitor or chip capacitor) can be selected for parallel use. On a physical level, capacitors should be as close as possible to both ends of VCC and GND.

2) The output port is also a part of the power circuit. In order to ensure the flatness of the output waveform, the output port should be designed as close as possible to the gate of the power MOSFET. In addition, additional resistors can be designed outside of OUT to make the working waveform more stable.

7.2 PCB Layout Guidelines

To achieve optimal performance of high-speed low side door drivers. It is recommended to pay attention to the following points when using:

1) The low ESR/ESL capacitor must be tightly connected to the IC between the VCC and GND pins to support the peak current drawn from the VDD during the mosfet turn on period.

2) Grounding considerations: The primary goal of designing grounding connections is to limit the MOSFET gate charge and discharge circuit to the smallest possible loop area. This method reduces the loop inductance and effectively avoids noise issues on the MOSFET gate.Meanwhile, the gate driver chip should be as close as possible to the MOSFET Star point grounding is a good method to reduce noise coupling from one current circuit to another.The ground point of the driver is connected to other circuit nodes such as the source of the power MOSFET and the ground of the PWM controller. The connection path must be as short as possible to reduce inductance and as wide as possible to reduce resistance.

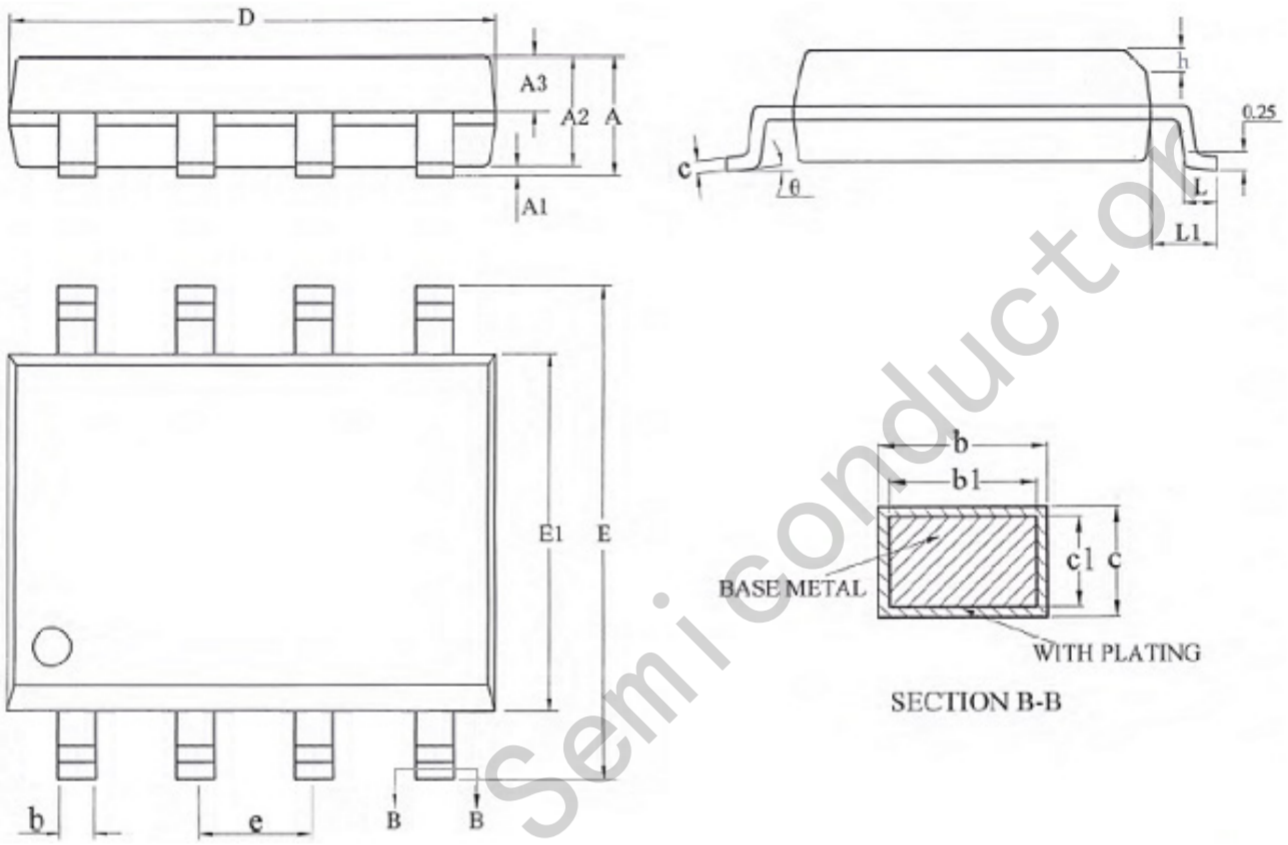
- Use grounding to shield noise. Due to the fact that the rapid rise and fall times of OUT may disrupt the input signal during the transition period, shielding noise through grounding can ensure that the input signal does not receive interference.The grounding ground cannot be a conductive path for any current circuit, and the ground plane must be connected to the star point to establish the ground potential. In addition to shielding noise, a grounding plane can also help dissipate heat.

3) In noisy environments, to prevent output faults caused by noise, unused PINs can be connected to VDD or GND.

4) The power circuit and signal circuit are separated, such as output and input signals.

8 PACKAGING INFORMATION

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°