UMW IRF7304TR

Dual P-Channel MOSFET

1.Description

The SOP-8 has been modified through a customized leadframe for enhanced thermacharacierstics and multip e-dle capabllity making it deal in a varety o powerapplications. With these improvements, multiple devices can be used in an application with dramatically reduced board space.

2.1Features

- $V_{DS\ (V)}$=-20V
- $R_{DS(ON)}$<90mΩ(V_{GS}=-4.5)
- $R_{DS(ON)}$<140mΩ(V_{GS}=-2.7V)

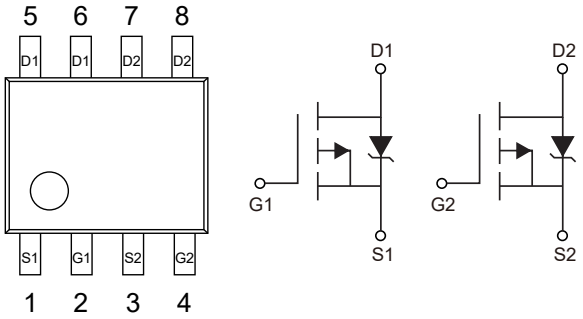
2.2Features

- Generation V Technology
- Ultra Low On-Resistance
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

3.Pinning information

Pin	Symbol	Description
2,4	G	GATE
1,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
10 Sec. Pulsed Drain Current, V_{GS}=-4.5V	T_A=25°C	I_D	-4.7	A
Continuous Drain Current, V_{GS}=-4.5V	T_A=25°C		-4.3	A
Continuous Drain Current, V_{GS}=-4.5V	T_A=70°C		-3.4	A
Pulsed Drain Current ①		I_{DM}	-17	A
Power Dissipation	T_A=25°C	P_D	2	W
Linear Derating Factor			0.016	W/°C

Gate-to-Source Voltage	V_{GS}	±12	V
Peak Diode Recovery dv/dt ②	dv/dt	-5	V/nS
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

5.Thermal resist ance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	°C/W

6.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-250μA, V_{GS}=0V	-20			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	I_D=-1mA,Reference to 25°C		-0.012		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-2.2A ③			90	mΩ
		V_{GS}=-2.7V, I_D=-1.8A ③			140	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.7			V
Forward Transconductance	g_{FS}	V_{DS}=-16V, I_D=-2.2A	4			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=-16V, V_{GS}=0V			-1	μA
		V_{DS}=-16V, V_{GS}=0V, T_J=125°C			-25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-12V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=12V			100	
Total Gate Charge	Q_g	I_D=-2.2A			22	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=-16V, V_{GS}=-4.5V			3.3	
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 12 ③			9	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-10V		8.4		ns
Rise Time	t_r	I_D=-2.2A		26		ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=6Ω		51		ns
Fall Time	t_f	R_D=4.5Ω, See Fig. 10 ③		33		ns
Internal Drain inductance	L_D	Between lead tip		4		nH
Internal Source inductance	L_S	and center of die contact		6		
Input Capacitance	C_{iss}	V_{GS}=0V		610		pF
Output Capacitance	C_{oss}	V_{DS}=-15V		310		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz, See Fig. 5		170		pF

Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-2.5	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-17	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=-1.8A,V_{GS}=0V ③			-1	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=-2.2A		56	84	ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs ③		71	110	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.(See fig.11)

② I_{SD}≤-2.2A, di/dt ≤ -50A/μS, V_{DD}≤ $V_{(BR)DSS}$,T_J≤ 150°C.

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

7.1Typical Characterisitics

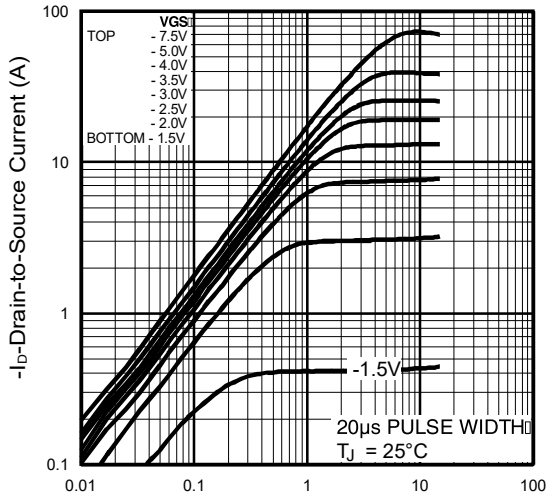


Fig 1. Typical Output Characteristics

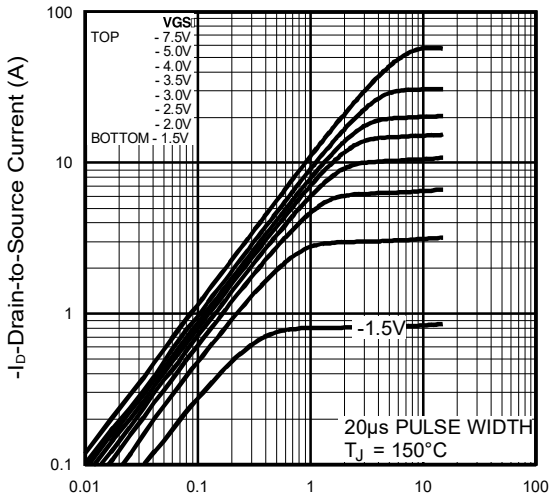


Fig 2. Typical Output Characteristics

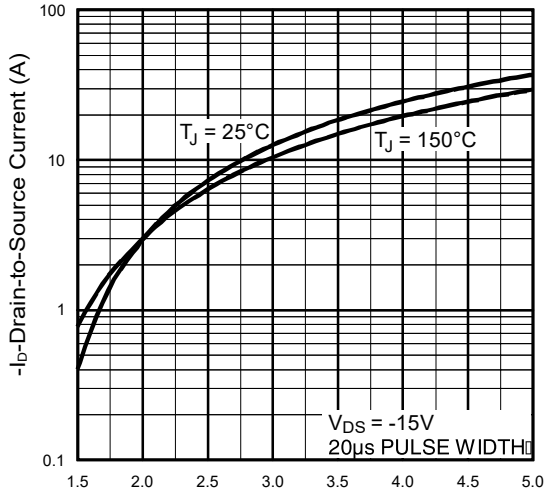


Fig 3. Typical Transfer Characteristics

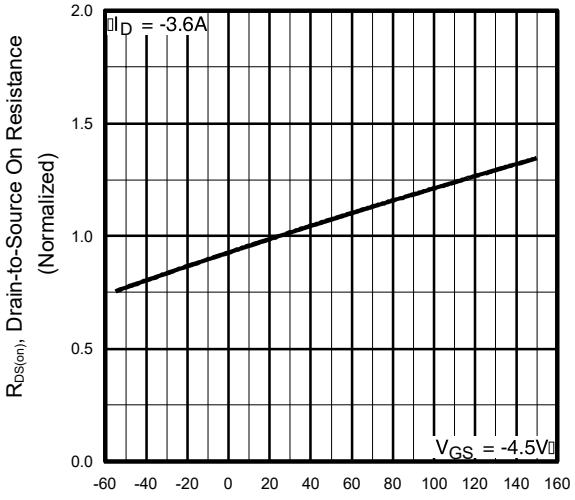
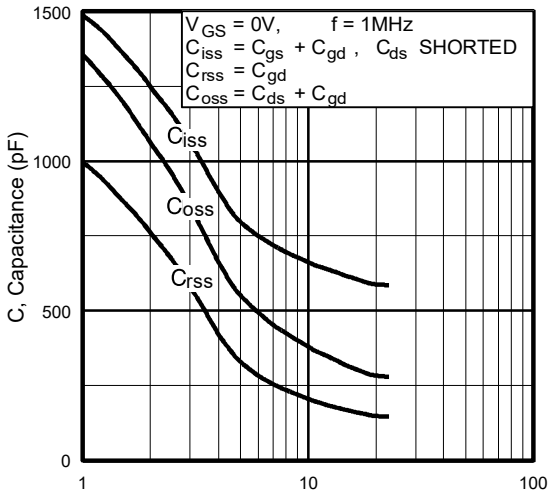


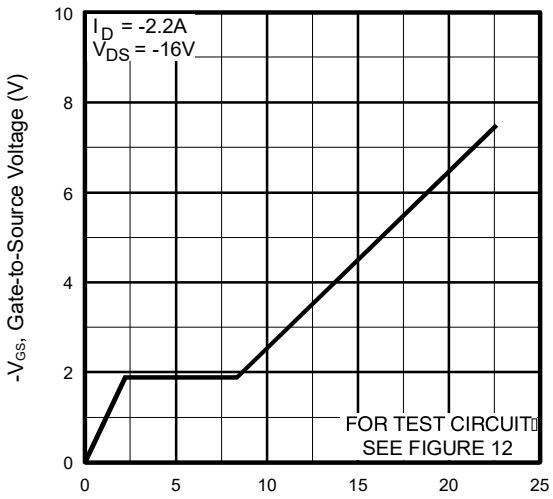
Fig 4. Nomalized On-ResistanceVs. Temperature

7.2Typical Characterisitics



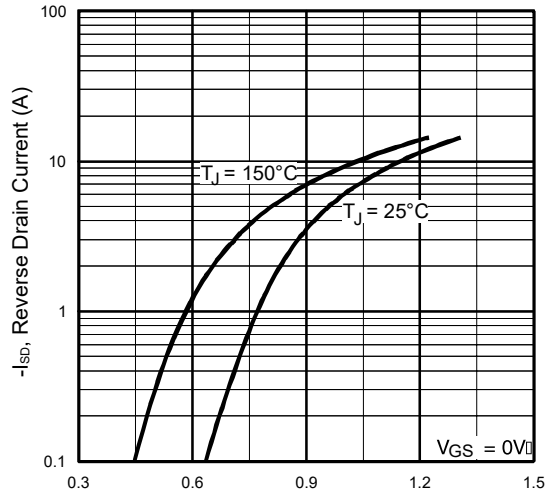
$-V_{DS}$,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



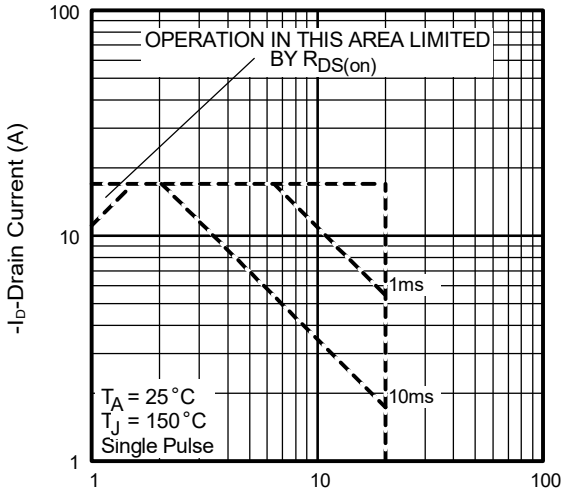
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



$-V_{SD}$, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage



$-V_{DS}$, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

7.3Typical Characterisitics

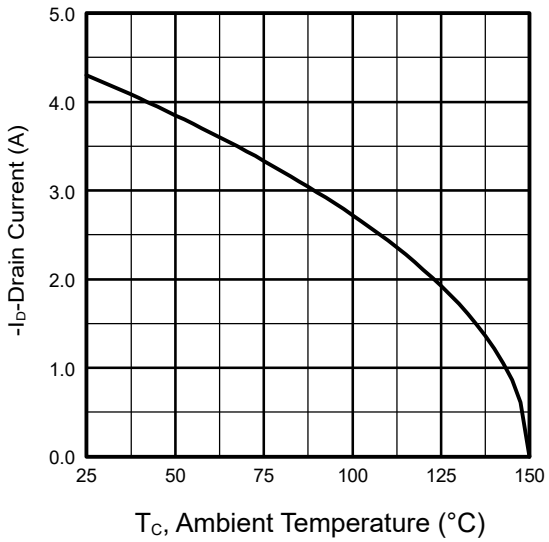


Fig 9. Maximum Drain Current Vs.AmbientTemperature

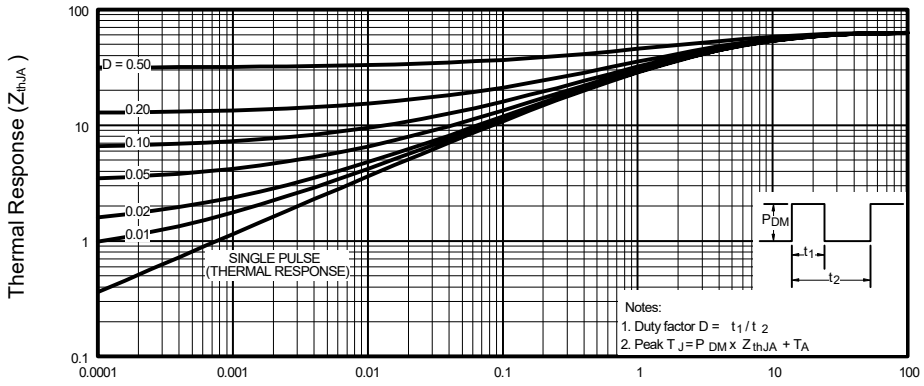


Fig 10. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

7.4Typical Characterisitics

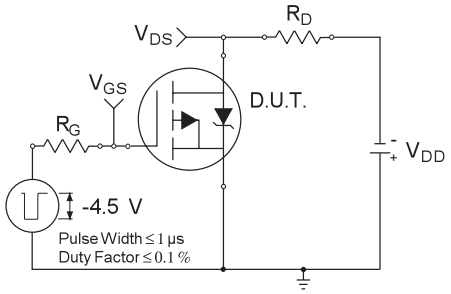


Fig 11a. Switching Time Test Circuit

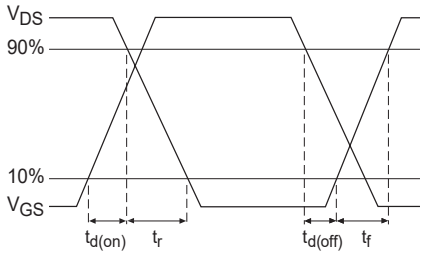


Fig 11b. Switching Time Waveforms

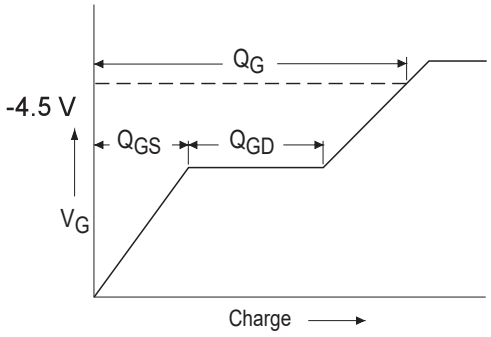


Fig 12a. Basic Gate Charge Wavefomm

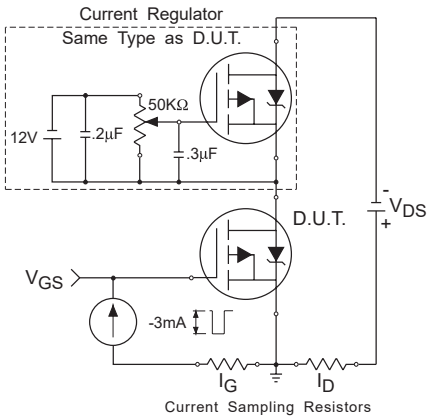


Fig 12b. Gate Charge Test Circuit

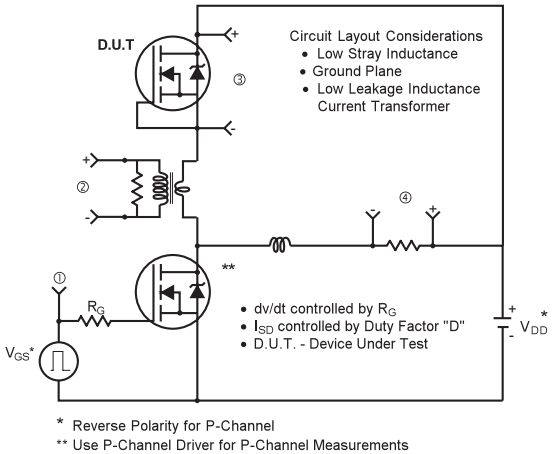
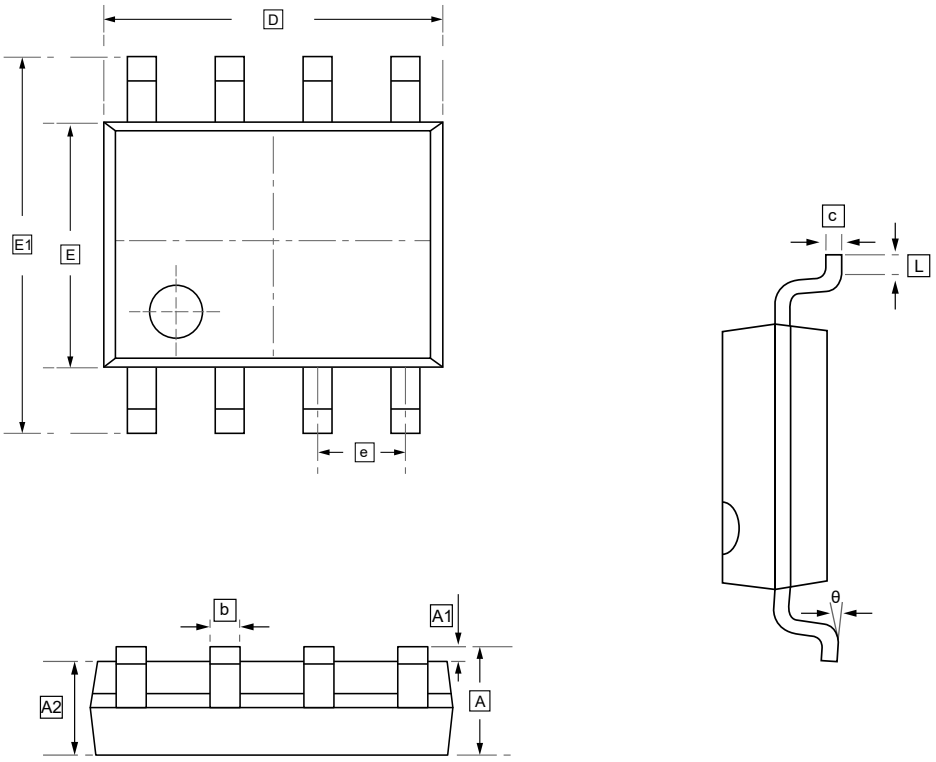


Fig 13. Peak Diode Recovery dv/dt Test Circuit

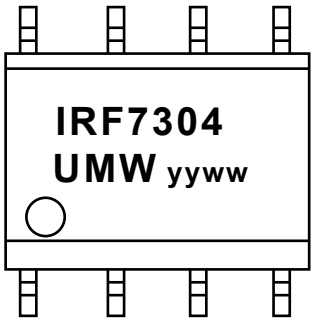
8.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7304TR	SOP-8	3000	Tape and reel

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