

1 Description

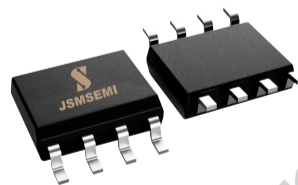
The IRS2103S is a high voltage, high speed power MOSFET drivers with dependent high-and low-

side referenced output channels.

Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction.

The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V. It can work in the temperature range of -40°C to 125°C .



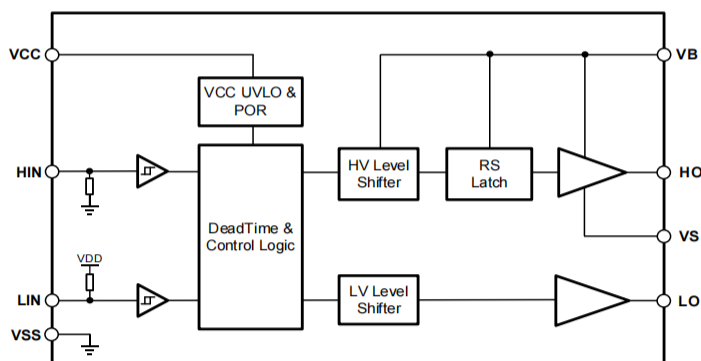
2 Features and Benefits

- Floating channel designed for bootstrap operation
 - Fully operational to +700V
 - 3.3 V, 5V and 15V logic compatible
 - dV/dt noise Immunity ± 50 V/nsec
 - Allowable negative Vs capability = -9V
 - VCC Undervoltage Lockout circuit
 - Undervoltage reset threshold=8.9V
 - Undervoltage set threshold= 8.2V
 - Transmission characteristic
 - turn-on/turn-off Propagation delay
 $T_{on}/T_{off} = 650\text{ns}/130\text{ns}$
 - Delay matching=50ns
 - Cross-conduction prevention logic
 - Deadtime:520ns
 - Wide operating temperature range $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - Output Source/ Sink current 300mA/600mA
 - RoSH compatible
- SOIC8 (S)

3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Functional Block Diagram



4 Function Pin Description

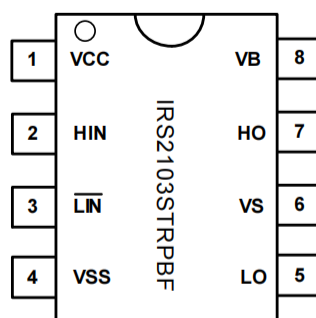


Figure 4-1 8-Pin SOIC8 Top view

Table 4-1 Lead Definitions

Number	Symbol	Description
1	VCC	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase
4	VSS	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

5 Product specifications

5.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	-0.3	725	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	
V _{HO}	High side gate drive output	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and main power supply	-0.3	25	
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input of HIN & LIN	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

5.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	Machine Model	500	—	V

5.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
PD1	Package Power Dissipation @ TA ≤ 25°C	—	625	mW

5.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
R _{thJA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T _J	Junction Temperature	—	150	
T _S	Storage Temperature	-55	150	°C
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	°C/W

5.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	V _S + 10	V _S + 20	V
V _S	High side floating supply return	-9	700	
V _{HO}	High side gate drive output	V _S	V _B	
V _{CC}	Low side and main power supply	10	20	
V _{LO}	Low side gate drive output	0	V _{CC}	
V _{IN}	Logic input of HIN & LIN	0	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note1: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

5.6 Electrical Characteristics

5.6.1 Dynamical electrical characteristics

Valid for temperature range at $T_A=25^\circ\text{C}$, $V_{CC}=V_B=15\text{V}$, $C_L=1\text{nF}$, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	650	820	ns	$V_S=0\text{V}$
t_{OFF}	Turn-off propagation delay	—	130	200	ns	$V_S=700\text{V}$
t_R	Turn-on rise time	—	75	130	ns	
t_F	Turn-off fall time	—	35	70	ns	
DT	Deadtime	400	520	650	ns	
MT	Matching delay ON and OFF	—	—	50	ns	
MDT	Matching delay	—	—	60	ns	

5.6.2 Static electrical characteristics

Valid for temperature range at $T_A=25^\circ\text{C}$, $V_{CC}=V_B=15\text{V}$, $C_L=1\text{nF}$, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—	V	
I_{LK}	Leakage current from VS (600V) to GND	—	—	50	μA	$V_B=V_S=700\text{V}$
I_{QBS}	Quiescent V_B supply current	—	50	100	μA	$V_{IN}=0\text{V}$ or 5V
I_{QCC}	Quiescent VCC supply current	—	120	240	μA	$V_{IN}=0\text{V}$ or 5V
V_{IH}	Logic "1" (\overline{HIN} & \overline{LIN}) input voltage	2.5	—	—	V	$V_{CC}=10\text{V}$ to 20V
V_{IL}	Logic "0" (\overline{HIN} & \overline{LIN}) input voltage	—	—	0.8	V	$V_{CC}=10\text{V}$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	0.1	V	$I_O=0\text{A}$
V_{OL}	Low level output voltage, V_O	—	—	0.1	V	$I_O=0\text{A}$
I_{IN+}	Logic "1" Input bias current	—	5	10	μA	$\overline{HIN}=5\text{V}$, $\overline{LIN}=0\text{V}$
I_{IN-}	Logic "0" Input bias current	—	—	2	μA	$\overline{HIN}=0\text{V}$, $\overline{LIN}=5\text{V}$
I_{O+}	Output high short circuit pulsed current	200	300	—	mA	$V_O=0\text{V}$ $PW \leq 10\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	400	600	—	mA	$V_O=15\text{V}$ $PW \leq 10\mu\text{s}$

6 Function Description

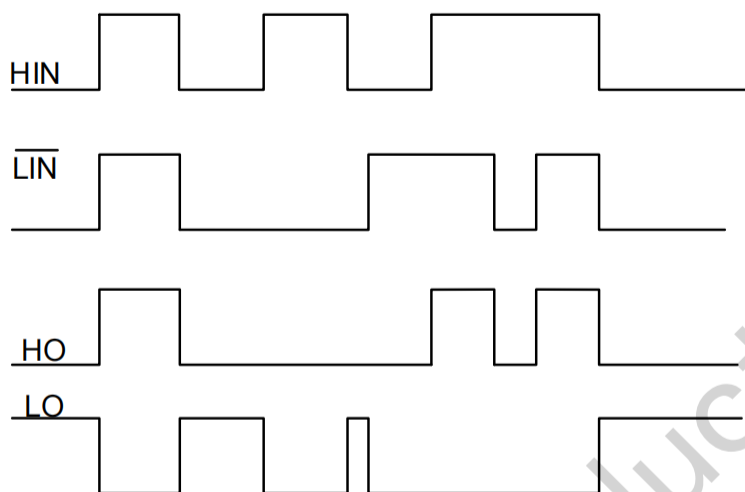


Figure 6. IRS2103S Input and output timing waveform

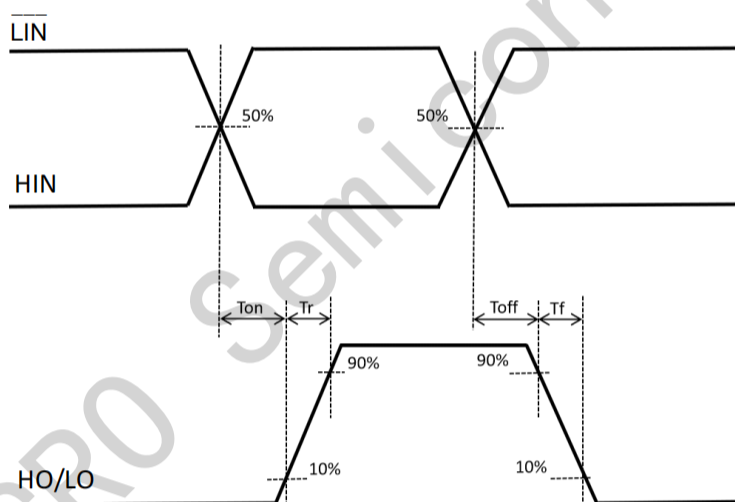


Figure 6. Propagation Time Waveform Definition

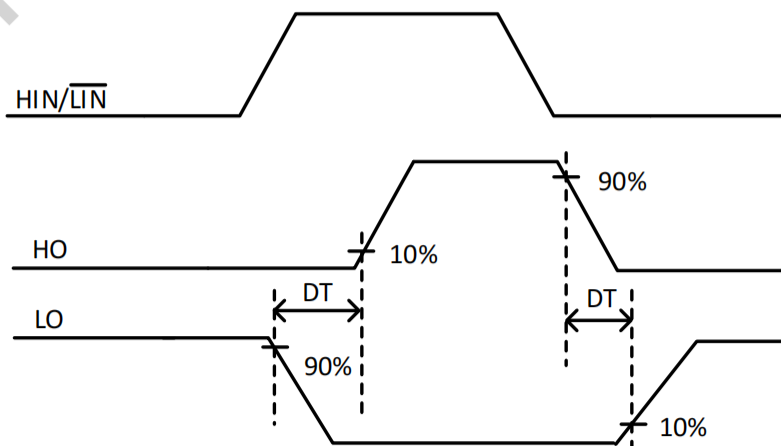


Figure6. Cross Conduction Prevention Delay Time Waveform Definition

7 IRS2103STRPBF Description

7.1 Function Block Diagram

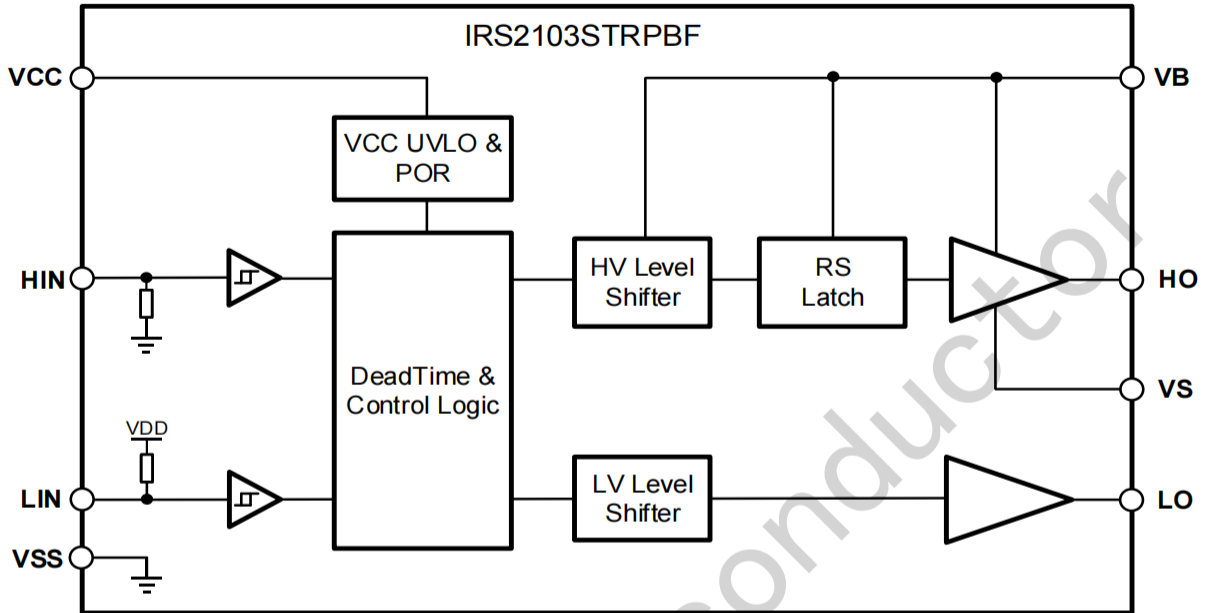


Figure 7-1 Function Block Diagram of IRS2103S

10.2 Typical application circuit

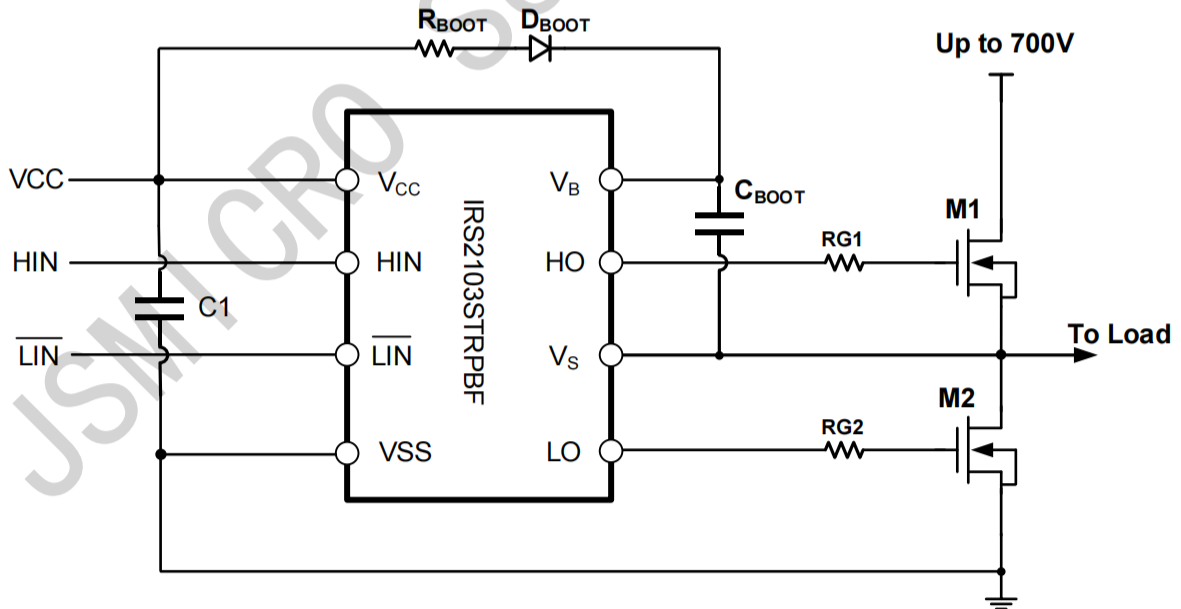
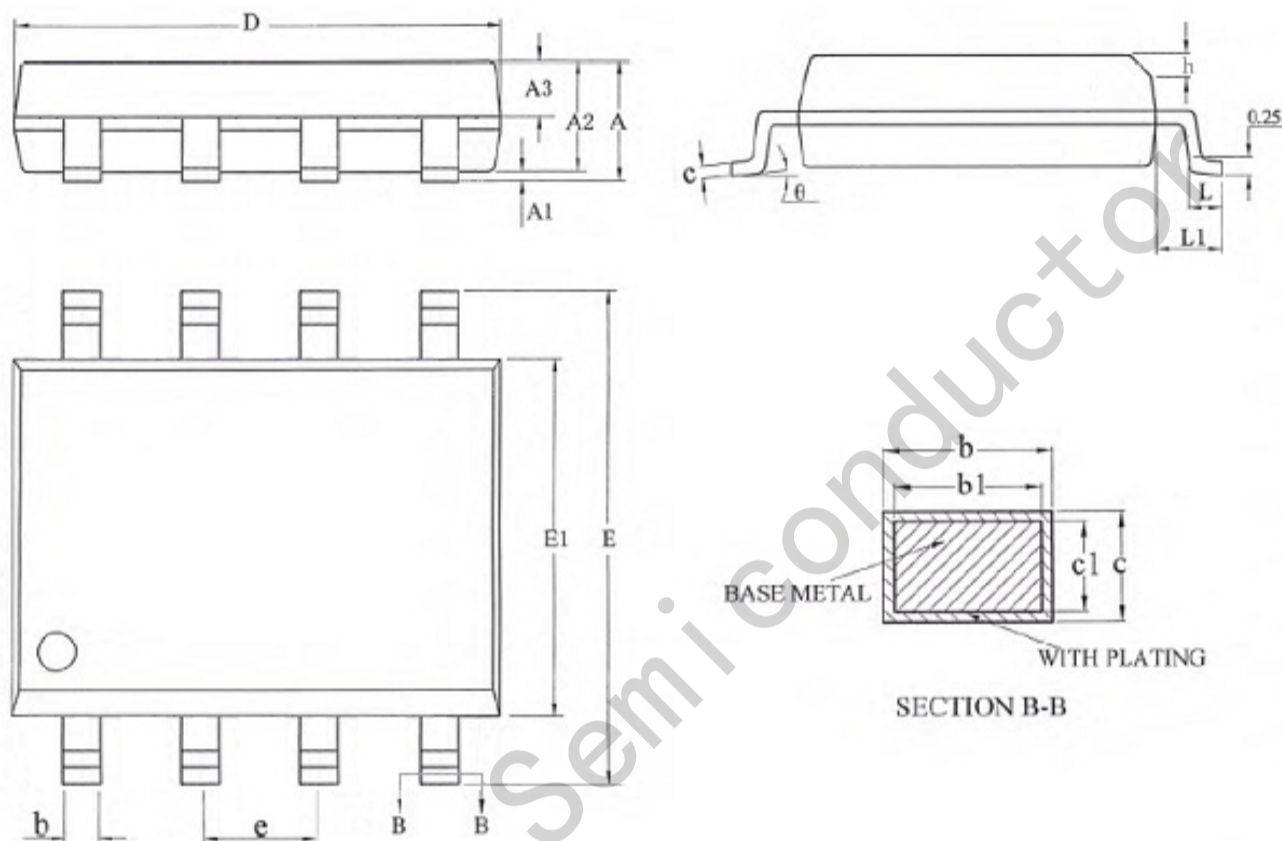


Figure 7-2 Typical application circuit of IRS2103S

8 Package Information

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50		
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°