

CD4076B Types

CMOS 4-Bit D-Type Registers

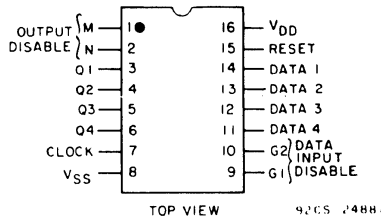
High-Voltage Types (20-Volt Rating)

The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT

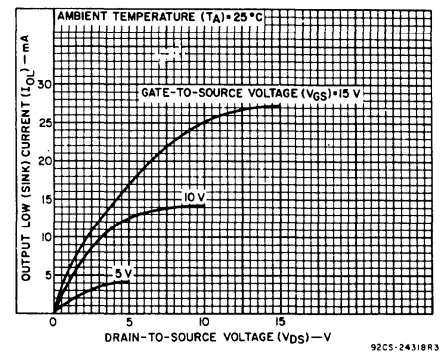
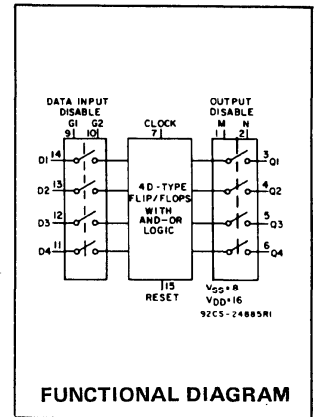


Fig.1 — Typical output low (sink) current characteristics.

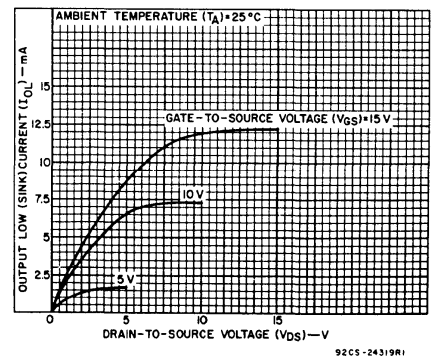


Fig.2 — Minimum output low (sink) current characteristics.

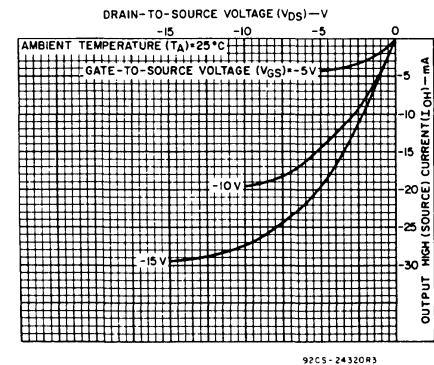


Fig.3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	200 80 60	— — —	ns
Clock Pulse Width, t_W	5 10 15	200 100 80	— — —	ns
Clock Input Frequency, f_{CL}	5 10 15	— dc —	3 6 8	MHz
Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}	5 10 15	— — —	15 5 5	μ s
Reset Pulse Width, t_W	5 10 15	120 50 40	— — —	ns
Data Input Disable Setup Time, t_S	5 10 15	180 100 70	— — —	ns

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	(Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS		-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT		± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)		500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)		Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)		500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)		Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:		
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)		100 mW
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPES D, F, K, H		-55 to $+125^\circ\text{C}$
PACKAGE TYPE E		-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})		-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.		$+265^\circ\text{C}$

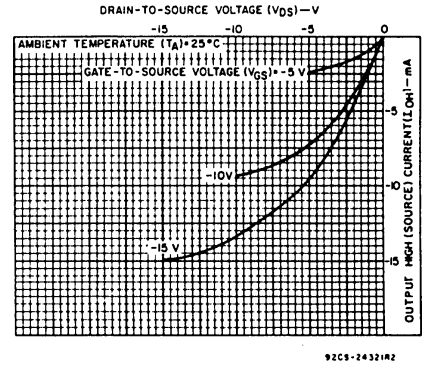
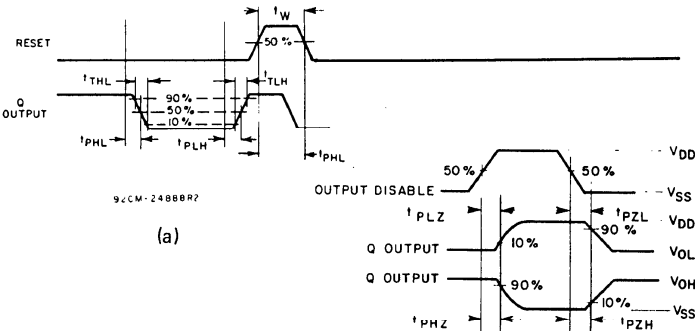
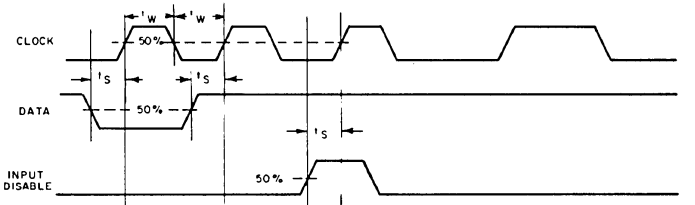


Fig. 4 — Minimum output high (source) current characteristics.



CHAR.	TEST AT	VOLT. VOLT.
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

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(b)

Fig. 5 — Functional waveforms for CD4076B.

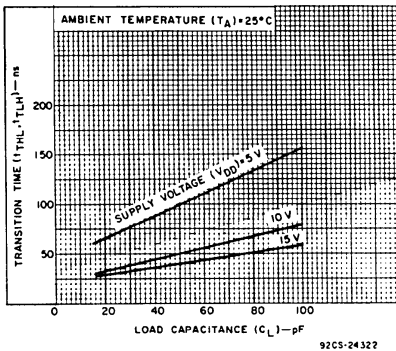


Fig. 7 — Typical transition time vs. load capacitance.

Truth Table						
Reset	Clock	Data Input Disable		Data D	Next State Output Q	
		G1	G2			
1	X	X	X	X	0	NC
0	0	X	X	X	Q	NC
0		1	X	X	Q	NC
0		X	1	X	Q	NC
0		0	0	1	1	
0		0	0	0	0	
0		0	0	0	0	
0	1	X	X	X	Q	NC
0		X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip-flops is not affected.

1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

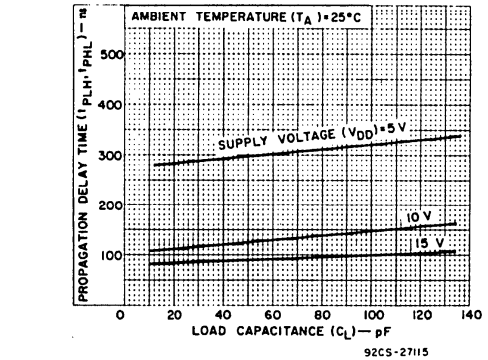


Fig. 6 — Typical propagation delay time vs. load capacitance (clock to Q).

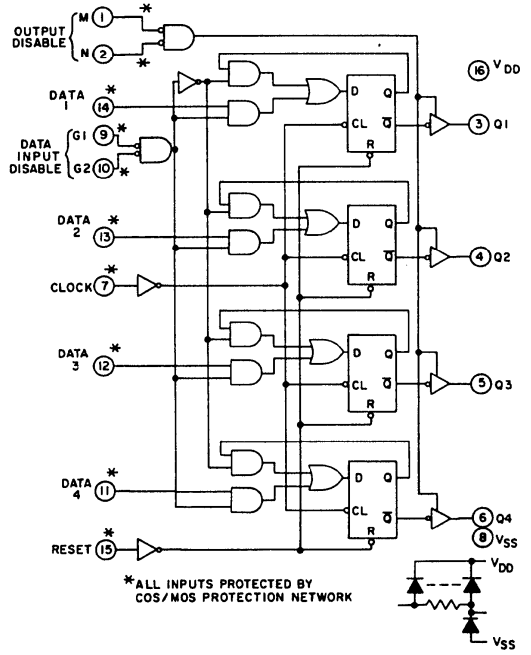


Fig. 8 — CD4076B logic diagram.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$ (Unless otherwise noted)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		V_{DD} V	Min.	Typ.		Max.
Propagation Delay Time: Clock to Q Output, t_{PHL} , t_{PLH}		5	..	300	600	
		10		125	250	
		15		90	180	
Reset, t_{PHL}		5		230	460	ns
		10		100	200	
		15		75	150	
3-State Output 1 or 0 to High Impedance, t_{PHZ} , t_{PLZ}	$R_L = 1 \text{ k}\Omega$	5		150	300	
		10		75	150	
		15		60	120	
3-State High Impedance to 1 or 0 Output, t_{PZH} , t_{PZL}	$R_L = 1 \text{ k}\Omega$	5		150	300	
		10		75	150	
		15		60	120	
Transition Time, t_{THL} , t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6	..	MHz
		10	6	12	..	
		15	8	16	..	
Minimum Clock Pulse Width, t_W		5	..	100	200	ns
		10	..	50	100	
		15	..	40	80	
Maximum Clock Input Rise or Fall Time, t_{rcf} , t_{fcf}		5	15	μs
		10	5	
		15	5	
Minimum Reset Pulse Width, t_W		5	..	60	120	ns
		10	..	25	50	
		15	..	20	40	
Minimum Data Setup Time, t_S		5	..	100	200	ns
		10	..	40	80	
		15	..	30	60	
Minimum Data Input Disable Setup Time, t_S		5	..	90	180	ns
		10	..	50	100	
		15	..	35	70	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

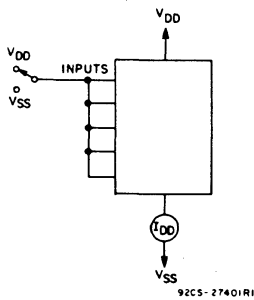


Fig. 11 – Quiescent device current test circuit.

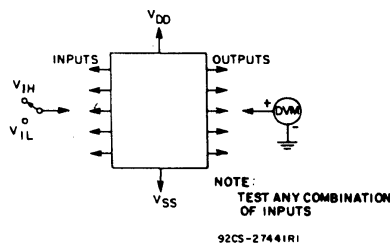


Fig. 12 – Input voltage test circuit.

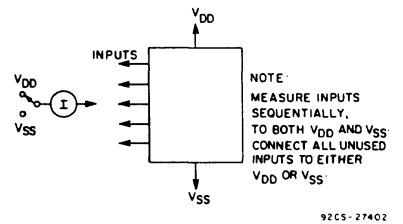


Fig. 13 – Input current test circuit.

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STATIC ELECTRICAL CHARACTERISTICS.

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	-	±10 ⁻⁴	±0,4	μA

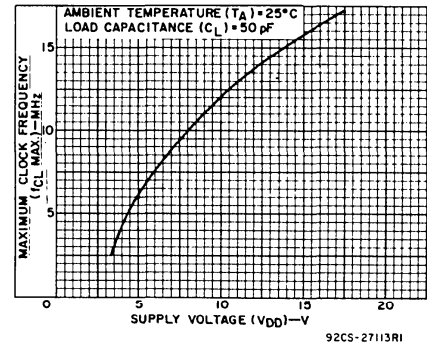


Fig.9 - Typical maximum clock input frequency vs. supply voltage.

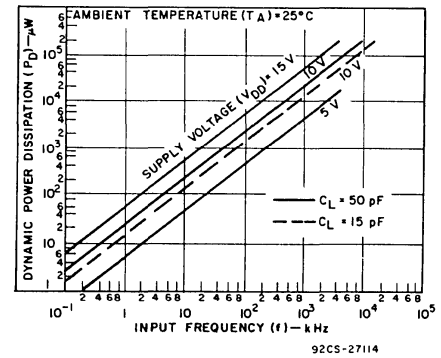
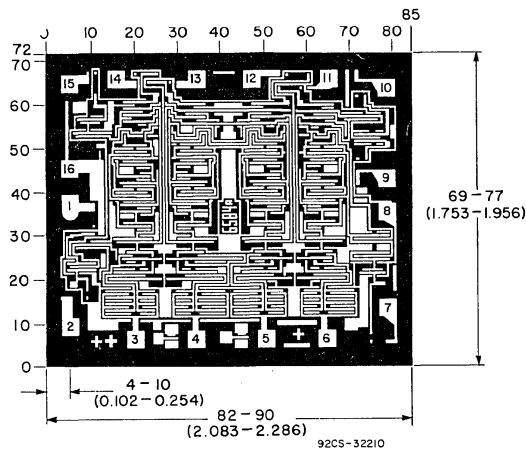


Fig.10 - Typical dynamic power dissipation vs. frequency.



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.